LINEAR APPLICATIONS HANDBOOK

NATIONAL SEMICONDUCTOR

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The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

Many of the application schematics call out the generic family, which, by coincidence, is the military temperature range version of the device. Generally, any device in the generic family will work in the circuit. For example, an amplifier marked LM108 refers to the generic 108 family, and does not imply that only military-grade devices will work. Military (or industrial) grade devices need only be considered when their tighter electrical limits or wider temperature range warrant their use. As a reminder to our users, our numbering system is:

Device No.	Grade	Specified Temperature Range
LM1XX	Military	$-55°C \leq T_A \leq +125°C$
LM2XX	Industrial	$-25°C \leq T_A \leq +85°C$
LM3XX	Commercial	$0°C \leq T_A \leq +70°C$

Because commercial parts are less expensive than military or industrial, these points should be kept in mind when trying to determine the most cost-effective approach to a given design.

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  Micropower: AN71-4
  Microvolt: LB32
  MOS driver: AN41-2, AN41-3, LB12-2
  Op amp voltage comparator: AN4-2, AN71-4, AN72-29
  Preamplifier: LB32
  Power: AN125-9
  Quad array: AN74
  Specifying selected parameters: LB26
  Timers used as: AN97-6
  TTL driver: AN4-2, AN29-15, AN31-3, AN41-2, AN41-3, LB12-2
  Zero crossing: AN31-17, AN41-2, AN41-3, LB6-2, LB12-2
VOLTAGE CONTROLLED OSCILLATOR: AN72-24, AN74-8, AN81-3, AN162
VOLTAGE FOLLOWER
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  Circuit description LH0033: AN48-1
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  Offset adjustment: AN31-4, LB9-2
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  (See Also Followers, Voltage)
VOLTAGE NOISE (See Noise, Voltage)
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VOLTAGE REGULATORS
  (See Also Regulators, Voltage; Positive, Negative, or Switching Voltage Regulator)
  Adjustables: AN178, AN181
  Current: AN103-3, AN110-6, AN127-3
  Dual tracking: AN82, AN103-8, AN103-9, Appendix C
  High current: AN103-3, AN103-5, AN110-4, AN110-5
  High current dual tracking: AN82-4
  High input voltage: AN103-9
  Improving reliability: AN182
  Paralleling: Appendix C
  Power distribution and regulation can be simple, cheap and rugged: Appendix C
  Using audio power amp: AN125-9
  1A, 65V with variable current limit: AN127-9
  ±32.5V dual tracking: AN127-9
VOLTMETER: AN32-2, AN71-6, AN75-4
VOLUME COMPRESSOR/EXPANDER (COMPANDER): AN129-7
VOX PREAMPLIFIER: AN51-8
WEIN BRIDGE OSCILLATOR: AN20-9, AN31-6, AN31-7, AN32-7 AN51-8
WEIN BRIDGE POWER OSCILLATOR: AN125-9
WIND VELOCITY INDICATOR: AN132-8
WINDOW DISCRIMINATOR, MULTIPLE APERTURE: AN31-3
ZENER DIODE
  IC: AN56
  Transistor base-emitter junction: AN71-8
ZENERS (See References, Voltage)
ZERO CROSSING DETECTOR: AN31-17, AN41-2, AN41-3, AN74-5, LB6-2, LB12-2
  Comparators suitable for "two shot": AN87, AN162
ZEROING, AMPLIFIER: AN63-8

Designing Switching Regulators

National Semiconductor
Application Note 2
March 1969

INTRODUCTION

The series pass element in a conventional series regulator operates as a variable resistance which drops an unregulated input voltage down to a fixed output voltage. This element, usually a transistor, must be able to dissipate the voltage difference between the input and output at the load current. The power generated can become excessive, particularly when the input voltage is not well regulated and the difference between the input and output voltages is large.

Switching regulators, on the other hand, are capable of high efficiency operation even with large differences between the input and output voltages. The efficiency is, in fact, negligibly affected by the voltage difference since this type of regulator acts as a continuously-variable power converter.

Switching regulators are, therefore, useful in battery-powered equipment where the required output voltage is considerably lower than the battery voltage. An example of this is a missile with a 30V battery as its only power source, containing a large number of integrated logic circuits which require a 5V supply. Switching regulators are also useful in space vehicles where conservation of power is extremely important. In addition, they are frequently the most economical solution in commercial and industrial applications where the increased efficiency reduces the cost of the series-pass transistors and simplifies heat sinking.

One of the disadvantages of switching regulators is that they are more complex than linear regulators, but this is often a substitution of electrical complexity for the thermal and mechanical complexity of high power linear regulators. Another disadvantage is higher output ripple. However, this can be held to a minimum (about 10 mV) and it is at a high enough frequency so that it can be easily filtered out. Another limitation is that the response to load transients is not always as fast as with linear regulators, but this can be largely overcome by proper design. The rejection of line transients, however, is every bit as good if not better than linear regulators. Lastly, switching regulators throw current transients back into the unregulated supply which are somewhat larger than the maximum load current. These, in some cases, can be troublesome unless adequate filtering is used.

This article will demonstrate the use of a monolithic voltage regulator in a number of switching regulator applications. These include both self-oscillating and synchronously driven regulators in the 0.1A to 5A range. Circuits are shown for both positive and negative regulators with output voltages in the 2V to 30V range. Methods of isolating the integrated circuit from the input voltage are given, permitting input voltages in excess of 100V. Further, current limiting schemes which keep peak currents and dissipation well within safe limits for both over-load and short-circuit conditions are presented. Finally, component selection details peculiar to switching regulators are covered.

SWITCHING REGULATOR OPERATION

The method by which a switching regulator produces a voltage conversion with high efficiency can be explained with the aid of Figure 1. Q_1 is a switch transistor which is turned on and off by a pulse waveform with a given duty cycle, and D_1 is a catch diode which provides a continuous path for the inductor current when Q_1 turns off. The voltage waveform on the collector of Q_1 will be as shown in the figure. The output of the LC filter will be the average value of the switched waveform, V_1. If the voltage drops across the transistor and diode are neglected, the output voltage will be

$$V_{OUT} = V_{IN} \frac{t_{on}}{T}; \qquad (1)$$

and it is independent of the load current. It is obvious from the equation that changes in input voltage can be compensated for by varying the duty cycle of the switched waveform. This is what is done in a switching regulator.

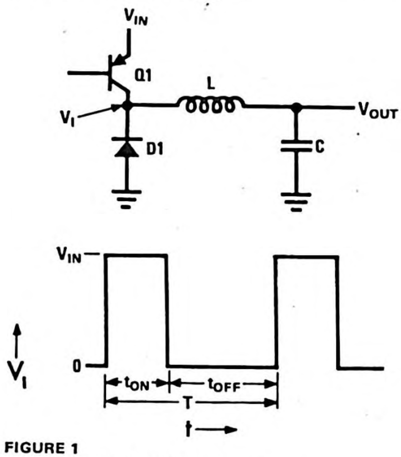


FIGURE 1
Switching Circuit for Voltage Conversion

Figure 2 shows a self-oscillating switching regulator which produces this duty-cycle control. A reference voltage, V_{ref}, equal to the desired output voltage, is supplied to one input of an operational amplifier, A_1. The operational amplifier, in turn, drives the switch transistor. The resistive divider, arranged such that $R_1 >> R_2$, provides a slight amount of positive feedback at high frequencies to make the circuit oscillate. At lower frequencies where the attenuation of the LC filter is less than the attenuation of the resistive divider, there is net negative feedback to the inverting input of the operational amplifier.

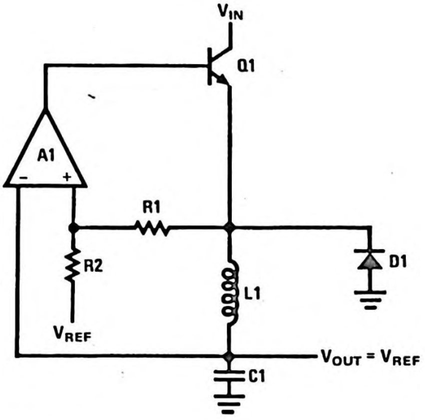


FIGURE 2
Self-oscillating Switching Regulator

In operation, when the circuit is first turned on, the output voltage is less than the reference voltage so the switch transistor is turned on. When this happens, current flow through R_1 raises the voltage on the non-inverting input of the operational amplifier slightly above the reference voltage. The circuit will remain switched on until the output rises to this voltage. The amplifier now goes into the active region, causing the switch to turn off. At this point, the reference voltage seen by the amplifier is *lowered* by feedback through R_1, and the circuit will stay off until the output voltage drops to this lower voltage. Hence, the output voltage oscillates about the reference voltage. The amplitude of this oscillation (or the output ripple) is nearly equal to the voltage fed back through R_1 to R_2 and can be made quite small.

THE LM100

The switching regulator circuits described here use the LM100 integrated voltage regulator as the control element. This device contains, on a single silicon chip, the voltage reference, the operational amplifier and the circuitry for driving a PNP switch transistor. Discrete switch transistors, catch diodes and reactive elements are employed since these components are not easily integrated.

A complete circuit description of the LM100 is given in Application Note AN-1 along with a number of its applications as a linear regulator. However, a brief description will be included here in order to facilitate understanding of the regulator circuits which follow.

Figure 3 shows a schematic diagram of the LM100. The voltage reference portion of the circuit starts with a breakdown diode, D_1, which is supplied by a current source from the unregulated input (one of the collectors of Q_2). The output of the reference diode, which has a positive temperature coefficient of 2.4 mV/°C, is buffered by an emitter follower, Q_4, which increases the temperature coefficient to +4.7 mV/°C. This is further increased to 7 mV/°C by the diode-connected transistor, Q_6. A resistor divider reduces this voltage as well as the temperature coefficient to exactly compensate for the negative temperature coefficient of Q_7, producing a temperature-compensated output of 1.8V.

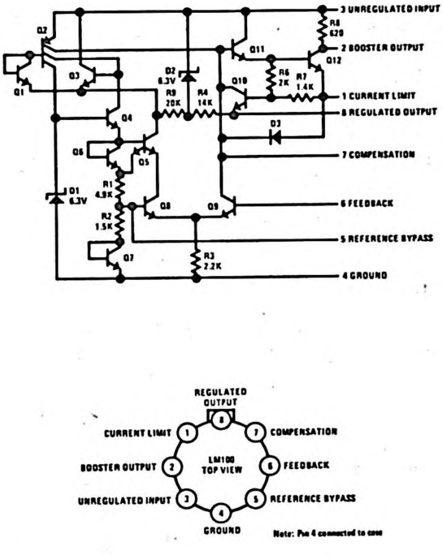

3 UNREGULATED INPUT
R8
620
2 BOOSTER OUTPUT
Q12
Q11
Q2
Q1
Q3
D2
6.3V
R9
20K
R4
14K
Q10
R6
2K
R7
1.4K
1 CURRENT LIMIT
8 REGULATED OUTPUT
D3
Q4
Q6
Q5
7 COMPENSATION
R1
4.9K
D1
6.3V
R2
1.5K
Q8
Q9
6 FEEDBACK
5 REFERENCE BYPASS
Q7
R3
2.2K
4 GROUND
REGULATED OUTPUT
8
CURRENT LIMIT
1
COMPENSATION
7
BOOSTER OUTPUT
2
LM100
TOP VIEW
FEEDBACK
6
UNREGULATED INPUT
3
REFERENCE BYPASS
5
4
GROUND
Note: Pin 4 connected to case

FIGURE 3

Schematic and Connection Diagrams of the LM100 Voltage Regulator

The transistor pair, Q_8 and Q_9, form the input stage of the operational amplifier. The gain of the stage is made high by the use of a current source, one of the collectors of Q_2, as a collector load. The output of this stage drives a compound emitter follower, Q_{11} and Q_{12}. The output of Q_{12} is taken across R_8 to drive the PNP switch transistor. An additional transistor, Q_{10}, is used to limit the output current of Q_{12} to the value required for driving a PNP transistor connected on the booster output. This current is determined by a resistor placed between the current limit and regulated output terminals. The value of the drive current can be determined from Figure 4 which plots the output current as a function of temperature for various current limit resistors.

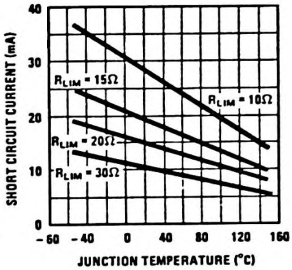


FIGURE 4

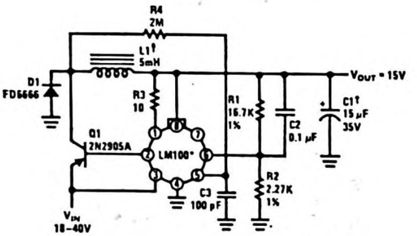
Switched Output Current as a Function of Temperature for Various Values of Current Limit Resistors

As for the remaining details of the circuit, Q_5, Q_3 and Q_1 are part of a bias stabilization circuit for Q_2 to set its collector currents at the desired value. R_9, R_4 and D_2 serve the sole function of starting the regulator. Lastly, D_3 is a clamp diode which keeps Q_9 from saturating when it is switching.

SWITCHING REGULATOR CIRCUITS

Figure 5 demonstrates the use of the LM100 as a switching regulator. Feedback to the inverting input of the operational amplifier (Pin 6 of the LM100) is obtained through a resistive divider which can be used to set the output voltage anywhere in the 2-30V range. R_3 determines the base drive for the switch transistor, Q_1, providing enough drive to saturate it with maximum load current. R_4 works into the 1 kΩ impedance at the reference terminal, producing the positive feedback. C_2 serves to minimize output ripple by causing the full ripple to appear on the feedback terminal. The remaining capacitor, C_3, removes the fast-risetime transients which would otherwise be coupled into Pin 5 through the shunt capacitance of R_4. It must be made small enough so that it does not seriously integrate the waveform at this point.

The circuit shown in Figure 5 is suitable for output currents as high as 500 mA. This limit is set by the output current available from the LM100 to saturate the switch transistor, Q_1. For lower currents, the value of R_3 should be increased so that the base of Q_1 is not driven unnecessarily hard.



*Basing diagram is Top View

†Solid tantalum

†125 turns #22 on Arnold Engineering A262123-2 molybdenum permalloy core.

FIGURE 5

Switching Regulator Using the LM100

The optimum switching frequency for these regulators has been determined to be between 20 kHz and 100 kHz. At lower frequencies, the core becomes unnecessarily large; and at higher frequencies, switching losses in Q_1 and D_1 become excessive. It is important, in this respect, that both Q_1 and D_1 be fast-switching devices to minimize switching losses.

The output ripple of the regulator at the switching frequency is mainly determined by R_4. It should be evident from the description of circuit operation that the peak-to-peak output ripple will be nearly equal to the peak-to-peak voltage fed back to Pin 5 of the LM100. Since the resistance looking into Pin 5 is approximately 1000Ω, this voltage will be

$$\Delta V_{ref} \simeq \frac{1000\,V_{IN}}{R_4} \tag{2}$$

In practice, the ripple will be somewhat larger than this. When the switch transistor shuts off, the current in the inductor will be greater than the load current so the output voltage will continue to rise above the value required to shut off the regulator. An important consideration in choosing the value of the inductor is that it be large enough so that the current through it does not change drastically during the switching cycle. If it does, the switch transistor and catch diode must be able to handle peak currents which are significantly larger than the load current. The change in inductor current can be written as

$$\Delta I_L \simeq \frac{V_{OUT} t_{off}}{L}. \tag{3}$$

In order for the peak current to be about 1.2 times the maximum load current, it is necessary that

$$L_1 = \frac{2.5\,V_{OUT} t_{off}}{I_{OUT\,(max)}}. \tag{4}$$

A value for t_{off} can be estimated from

$$t_{off} = \frac{1}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right), \tag{5}$$

where f is the desired switching frequency and V_{IN} is the nominal input voltage.

The size of the output capacitor can now be determined from

$$C_1 = \left(\frac{V_{OUT}}{2L_1 \Delta V_{OUT}}\right)\left(\frac{V_{IN} - V_{OUT}}{f V_{IN}}\right)^2 \tag{6}$$

where ΔV_{OUT} is the peak-to-peak output ripple and V_{IN} is the nominal input voltage.

It now remains to determine if the component values obtained above give satisfactory load-transient response. The overshoot of the regulator can be determined from

$$\Delta V_{OUT} = \frac{L_1 (\Delta I_L)^2}{C_1 (V_{IN} - V_{OUT})} \tag{7}$$

for increasing loads, and

$$\Delta V_{OUT} = \frac{L_1 (\Delta I_L)^2}{C_1 V_{OUT}} \tag{8}$$

for decreasing loads, where ΔI_L is the load-current transient. The recovery time is

$$t_r = \frac{2L_1 \Delta I_L}{V_{IN} - V_{OUT}} \tag{9}$$

and

$$t_r = \frac{2L_1 \Delta I_L}{V_{OUT}} \tag{10}$$

for increasing and decreasing loads respectively.

In order to improve the load transient response, it is necessary to allow larger peak to average current ratios in the switch transistor and catch diode. Reducing the value of inductance given by Equation (4) by a factor of 2 will reduce the overshoot by 4 times and halve the response time. This, of course, assumes that the output capacitance is doubled to maintain a constant switching frequency.

The above equations outline a design procedure for determining the value for R_4, L_1, and C_1, given the switching frequency and the output ripple. These equations are not exact, but they do provide a starting point for designing a regulator to fit a given application.

As an example, this design method will be applied to a regulator which must deliver 15V at a maximum current of 300 mA from a 28V supply. To start, a 40 kHz switching frequency will be selected along with an output ripple of 14 mV, peak-to-peak.

From (2), R_4 is calculated to be 2 MΩ. In determining L_1, t_{off} is found to be 11.6 μs from (5). Inserting this into (4) gives a value of 1.45 mH for L_1. The value of C_1 obtained from (6) is then 57.5 μF.

In the actual circuit of Figure 5, a standard value of 47 μF is used for C_1; and L_1 is adjusted to 1.7 mH. The switching frequency obtained experimentally on this circuit is 60 kHz and the peak-to-peak output ripple is 20 mV. The fairly-large disagreement between the calculated and experimental values is not alarming since many simplifying assumptions were made in the derivation of the equations. They do, however, provide a convenient method of handling a large number of mutually-dependent variables to arrive at a working circuit.

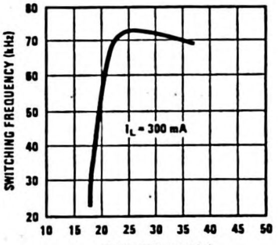


FIGURE 6

Switching Frequency as a Function of Input Voltage

More exact expressions would involve a design procedure which is too cumbersome to be of practical value.

The variation of switching frequency with input voltage and load current is shown in Figures 6 and 7. The sharp rise in frequency at low output currents happens because the output transistor of the LM100 (Q_{12}) begins to supply an appreciable portion of the load current directly.

The efficiency of the regulator over a wide range of input voltages and output currents is given in Figures 8 and 9.

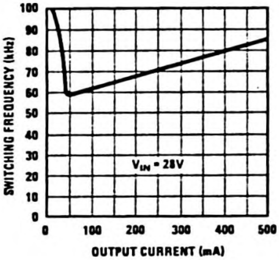


FIGURE 7

Switching Frequency as a Function of Output Current

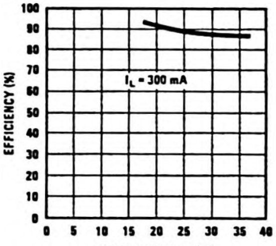


FIGURE 8

Efficiency as a Function of Input Voltage

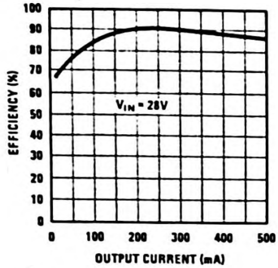
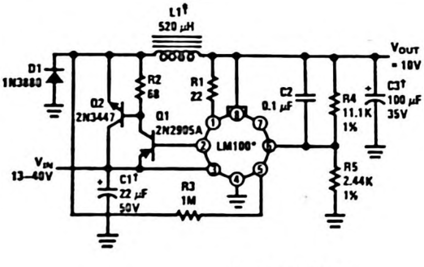


FIGURE 9
Efficiency as a Function of Output Current

HIGHER CURRENT REGULATORS

If output currents greater than about 500 mA are required, it is necessary to add another switch transistor to obtain more current gain. This is illustrated in Figure 10. With the exception of the added NPN power switch, Q_2, this circuit is the same as that described previously.

A photograph of a high-current regulator is shown in Figure 11. It is capable of delivering output currents of 3A continuously with only a small heat sink. Figure 12 shows that the efficiency is better than 80 percent at this level. Output currents to 5A can be obtained at reduced efficiency. However, the case temperature of the power switch and catch diode approach 100°C under this condition, so continuous operation is not recommended unless more heat sink is provided.



*Basing diagram is Top View

†Solid tantalum

‡60 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 10
Switching Regulator for Higher Output Currents

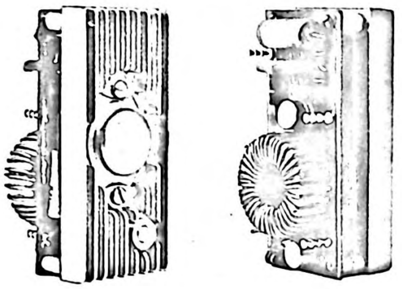


FIGURE 11
High Current Switching Regulator

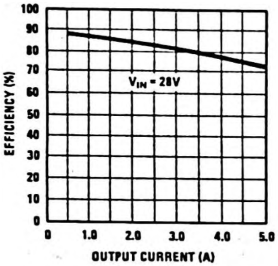


FIGURE 12
Efficiency as a Function of Output Current

Figure 13 shows that the efficiency is not significantly affected by input voltage. In Figure 14 it can be seen that the switching frequency is fairly constant over a wide range of input voltages. Figure 15 shows that the switching frequency increases with increasing load current. The higher dc current through the inductor reduces the incremental inductance causing the frequency to go up. The last graph, Figure 16, illustrates the line regulation of the device. this can be improved by putting a small capacitor (0.01 μF) in series with the positive feedback resistor, R_3, to isolate the reference terminal from the dc input voltage changes.

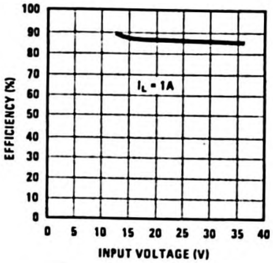


FIGURE 13

Efficiency as a Function of Input Voltage

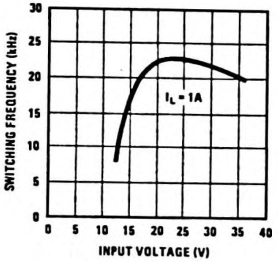


FIGURE 14

Variation of Switching Frequency with Input Voltage

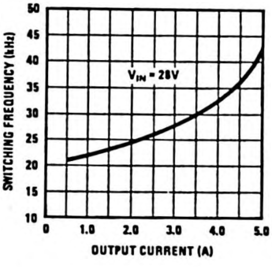


FIGURE 15

Variation of Switching Frequency with Output Current

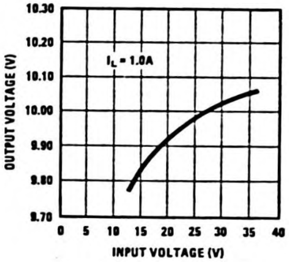


FIGURE 16

Line Regulation

At low output currents the inductor current can drop to zero at some time after the switch transistor turns off. When this happens, ringing occurs on the switching waveform. This is perfectly normal and causes no ill effects.

The use of solid tantalum capacitors for C_1 and C_3 is recommended when the regulator is expected to perform over the full military temperature range. The reason for using 35V capacitors on the output, even though the output voltage is only 10V, is that the 40 mV peak-to-peak ripple on the output would, for example, exceed the ratings of a 100 μF, 15V capacitor.

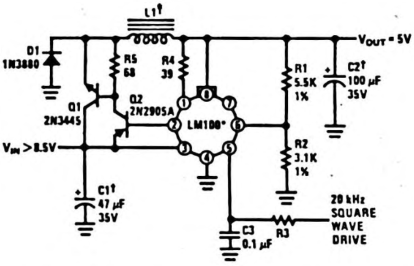
Aluminum electrolytic capacitors have been used successfully over a limited temperature range. And there is basically no reason why wet foil or wet slug tantalums could not be used as long as their equivalent series resistance is low enough so that they behave like capacitors with the high frequency switched-current waveform. It is also important that manufacturer's data be consulted to insure that they can withstand the high frequency ripple.

As was mentioned with the low current regulator, it is necessary to use fast-switching diodes and transistors in these circuits. Ordinary silicon rectifiers or low-frequency power transistors will operate at drastically-reduced efficiencies and will quickly overheat in these circuits.

DRIVEN SWITCHING REGULATOR

When a number of switching regulators are used together in a system it is sometimes desirable to synchronize their operation to more uniformly distribute the switched current waveforms on the input line. Synchronous operation is also wanted when a switching regulator is operated in conjunction with a power converter.

A circuit for synchronizing the switching regulator with a square wave drive signal is shown in Figure 17. In this circuit, positive feedback is not used. Instead, the square wave drive signal is integrated; and the resulting triangular wave (about 40 mV peak-to-peak) is applied to the reference bypass terminal of the LM100. This triangular wave will cause the regulator to switch since its gain is so high that the waveform overdrives it. The duty cycle of the switched waveform is controlled by the voltage on the feedback terminal, Pin 6. If this voltage goes up, the duty cycle will decrease since it is picking off a smaller portion of the triangular wave on Pin 5. By the same token, the duty cycle will decrease if the voltage on Pin 6 drops.



*Basing diagram is Top View

†Solid tantalum

†100 turns #22 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 17
Driven Switching Regulator

This action produces the desired regulation: if the output voltage starts to go up, it will raise the voltage on Pin 6 such that a smaller portion of the triangular wave is picked off. This reduces the duty cycle, counteracting the output voltage increase.

In order for this circuit to work properly, the ripple voltage on Pin 6 should be less than a quarter of the peak-to-peak amplitude of the triangular wave. If this condition is not satisfied, the regulator will try to oscillate at its own frequency. Further, since the resistance looking into Pin 5 is about 1 kΩ, the integrating capacitor, C_3, should have a capacitive reactance of less than 100Ω at the drive frequency. The value of R_3 is determined so that the amplitude of the triangular wave on Pin 5 is about 40 mV.

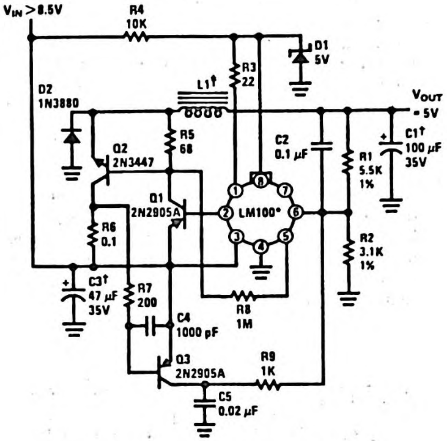
Driven regulators also have other advantages. For one, it is possible to design the LC filter independent of switching frequency considerations. Hence, lower output ripple and better transient response can be realized. A second advantage is the frequency stability. In a self-oscillating regulator, the switching frequency is controlled by a relatively large number of factors. As a result, it is not well determined when normal tolerances are taken into account. With low and medium power regulators, this is not usually a problem since the efficiency does not vary greatly with frequency. However, high power regulators tend to be more frequency sensitive and it is desirable to operate them at constant frequency.

CURRENT LIMITING

In the circuits described previously, the regulator is not protected from overloads or short-circuited output. Providing short-circuit protection is no simple problem, since it is necessary to keep the regulator switching when the output is shorted. Otherwise, the dissipation will become excessive even though the current is limited.

A circuit that does this is shown in Figure 18. The peak current through the switch transistor is sensed by R_6. When the voltage drop across this resistor becomes large enough to turn on Q_3, the output voltage begins to fall since current is being supplied to the feedback terminal of the regulator from the collector of Q_3 so less has to be supplied from the output through R_1. Furthermore, the circuit will continue to oscillate, even with a shorted output, because of positive feedback through R_6 and the relatively-long discharge time constant of C_2.

It is necessary to put a resistor, R_7, in series with the base of Q_3 to insure that excessive current will not be driven into the base. In addition, a capacitor, C_4, must be added across the input of Q_3 so that it does not turn on prematurely on the large current spike (about twice the load current) through the switch transistor caused by pulling the stored charge out of the catch diode. A zener diode bias supply must also be used on the output of the LM100 since the current limiting will not work if the voltage on this point drops below about 1V.


V_IN > 8.5V
R4
10K
D1
5V
R3
22
L1†
D2
1N3880
V_OUT
= 5V
Q2
2N3447
R5
68
C2
0.1 µF
R1
5.5K
1%
C1†
100 µF
35V
Q1
2N2905A
LM100*
R6
0.1
R2
3.1K
1%
C3†
47 µF
35V
R7
200
C4
1000 pF
R8
1M
Q3
2N2905A
R9
1K
C5
0.02 µF

*Basing diagram is Top View

†Solid tantalum

†70 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 18

Switching Regulator with Current Limiting

The current limiting characteristics of this circuit are shown in Figure 19. Figure 20 shows how the average input current actually drops off as the circuit goes into current limiting.

This current limiting scheme protects the switching transistors from overload or short-circuited output. However, the drop-out current and short-circuit current are not well controlled, so it is difficult to prove that the circuit will sustain a continuous short circuit under worst-case conditions. This is particularly true with high current regulators where the required amount of overdesign can become quite expensive.

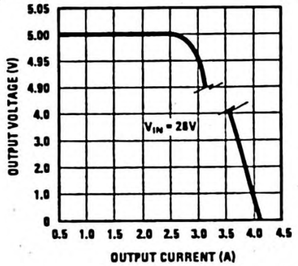


FIGURE 19

Current Limiting Characteristics

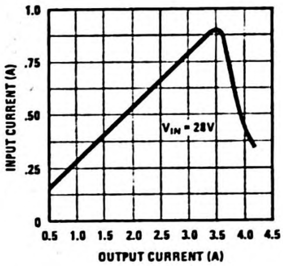
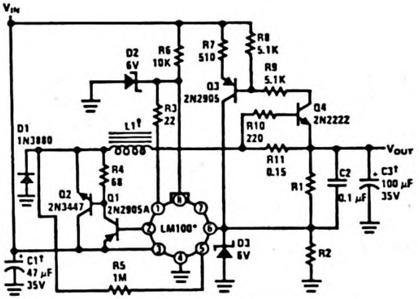


FIGURE 20

Illustrating Drop in Input Current as Regulator Goes Into Limiting

Figure 21 shows a circuit which is more easily designed for continuous short-circuit protection under worst-case conditions. In this circuit, the current-sensing resistor is located in series with the inductor. Therefore, the peak-limiting current can be more precisely determined since the current spike generated by pulling the stored charge out of the catch diode does not flow through the sense resistor.


V_IN
D2
6V
R6
10K
R7
510
R8
5.1K
R9
5.1K
Q3
2N2905
Q4
2N2222
R3
22
L1†
D1
1N3880
R10
220
R11
0.15
V_OUT
R4
68
Q2
2N3447
Q1
2N2905A
LM100*
R1
C2
0.1 µF
C3†
100 µF
35V
D3
6V
R2
C1†
47 µF
35V
R5
1M

*Basing diagram is Top View

†Solid tantalum

†70 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 21

Switching Regulator with Continous Short-Circuit Protection

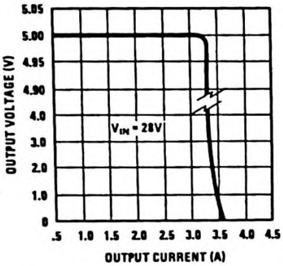


FIGURE 22
Current Limiting Characteristics

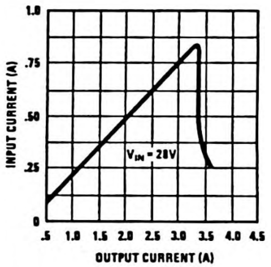


FIGURE 23
Plot of Input Current as Regulator Goes Into Limiting

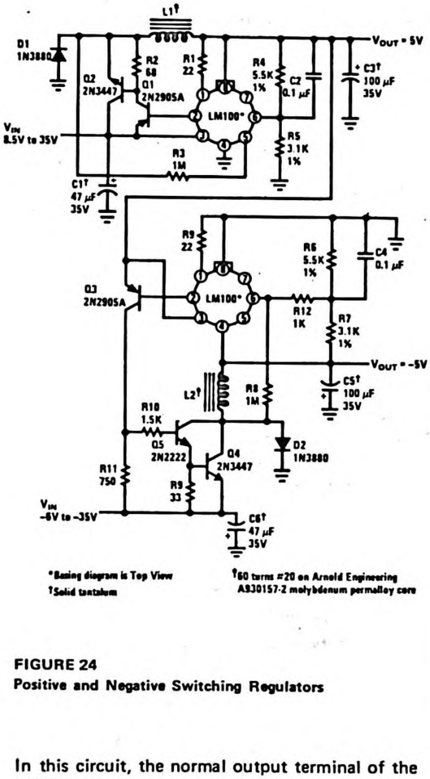
Operation of this circuit is essentially the same as the previous one in that an NPN transistor, Q_4, senses the overcurrent condition and turns on Q_3 which supplies the current-limit signal to the feedback terminal. The zener diode, D_3, is required on the feedback terminal to guarantee that this terminal cannot go more than 0.5V higher than Pin 1. If this does happen, the circuit can latch up and burn out. The performance of this current-limiting scheme is illustrated in Figures 22 and 23.

With this circuit it is not only possible to more accurately determine the limiting current, but as can be seen from Figures 22 and 23, the limiting characteristic is considerably sharper. One disadvantage of this circuit is that the load current flows continuously through the current sense resistor, reducing efficiency. As an example, with a 5V regulated output the efficiency will be reduced by 10 percent at full load.

NEGATIVE REGULATORS

All circuits discussed thus far are for regulators with positive outputs. Although negative regulators can be obtained by floating the unregulated supply and grounding the output, this is not always convenient.

Figure 24 shows a circuit for a negative switching regulator where the unregulated input and regulated output have a common ground. The only limitation of the circuit is that there must be a positive voltage greater than 3V available in order to properly bias the negative regulator.


L1†
D1
1N3880
Q2
2N3447
R2
68
Q1
2N2905A
R1
22
R4
5.5K
1%
C2
0.1 µF
+ C3†
100 µF
35V
V_{OUT} = 5V
V_{IN}
8.5V to 35V
LM100*
1 2 3 4 5 6 7 8
R3
1M
R5
3.1K
1%
C1†
47 µF
35V
R9
22
R6
5.5K
1%
C4
0.1 µF
Q3
2N2905A
LM100*
R12
1K
R7
3.1K
1%
V_{OUT} = -5V
C5†
100 µF
35V
L2†
R8
1M
R10
1.5K
Q5
2N2222
Q4
2N3447
D2
1N3880
R11
750
R9
33
V_{IN}
-6V to -35V
C6†
47 µF
35V

*Basing diagram is Top View
†Solid tantalum

†60 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

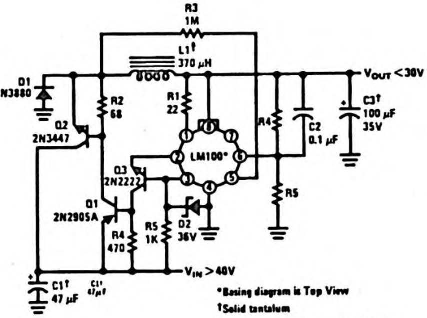
FIGURE 24
Positive and Negative Switching Regulators

In this circuit, the normal output terminal of the LM100 (Pin 8) is grounded and the ground terminal (Pin 4) is connected to the regulated negative output. Hence, as before, it regulates the voltage between the output and ground terminals. The unregulated input terminal (Pin 3) is run from a positive voltage for proper biasing. A PNP booster transistor, Q_3, is connected in the normal manner; and it drives a Darlington-connected NPN switch. Positive feedback is developed by the resistive divider, R_8 and R_{12}.

It is necessary to use a Darlington switch even though the current gain is not needed. The power switch transistor, Q_4, cannot be operated with a fixed base drive: if the base drive is made large enough to insure saturation at maximum load current, it will overstore so badly at lower currents that the output ripple will increase radically. With the extra transistor, however, it is kept out of saturation at lower output currents, eliminating the problem.

HIGH VOLTAGE REGULATORS

With switching regulators, an application can easily arise where the input voltage can be higher than the 40V maximum rating of the LM100, even though the output voltage is within the 30V maximum. As shown in Figure 25, it is possible to isolate the LM100 from the unregulated supply so that it can be used with input voltages limited only by the switch transistors and the catch diode.


R3
1M
L1†
370 μH
V_OUT <30V
D1
1N3880
R2
68
R1
22
C3†
100 μF
35V
Q2
2N3447
R4
C2
0.1 μF
LM100*
Q3
2N2222
R5
Q1
2N2905A
R5
1K
D2
36V
R4
470
V_IN >40V
C1†
47 μF
C1'
47μF

*Basing diagram is Top View

†Solid tantalum

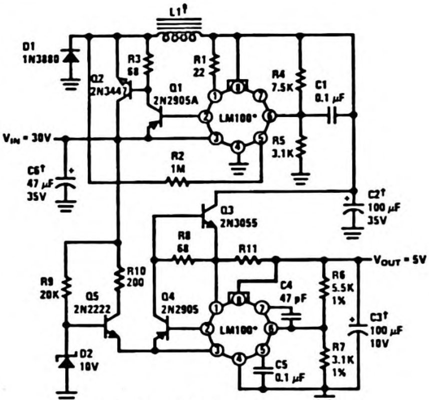
†50 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 25
Switching Regulator for High-voltage Inputs

In this circuit, the voltage seen by the LM100 is maintained at a fixed level within ratings by the zener diode, D_2. The zener voltage must be at least 3V greater than the output voltage. The output of the LM100 is level-shifted up to the input voltage by an additional NPN transistor, Q_3, which is operated common base. This drives the PNP switch driver in the normal manner.

SWITCHING AND LINEAR REGULATOR COMBINATION

In certain applications, the output ripple and load transient response requirements rule out the use of a switching regulator, yet the input-output voltage differential is still high. In this case, a power converter might be used to reduce the input voltage and this reduced voltage would be regulated by a linear regulator. This arrangement, however, is not nearly as efficient as the switching and linear regulator combination shown in Figure 26. The switching regulator not only reduces the input voltage with high efficiency, but it also regulates it. Therefore, the linear regulator operates with a fixed input-output voltage differential which holds dissipation to a minimum.


L1†
D1
1N3880
R3
68
R1
22
Q2
2N3447
Q1
2N2905A
R4
7.5K
C1
0.1 μF
LM100*
V_IN = 30V
R5
3.1K
R2
1M
C6†
47 μF
35V
C2†
100 μF
35V
Q3
2N3055
R8
68
R11
V_OUT = 5V
R9
20K
R10
200
Q5
2N2222
Q4
2N2905
C4
47 pF
R6
5.5K
1%
C3†
100 μF
10V
LM100*
D2
10V
R7
3.1K
1%
C5
0.1 μF

*Basing diagram is Top View

†Solid tantalum

†60 turns #20 on Arnold Engineering A930157-2 molybdenum permalloy core

FIGURE 26
Switching and Linear Regulator Combination for Obtaining Very Low Ripple and Fast Transient Response

In this circuit, the linear regulator is biased by a zener pre-regulator (R_9, D_2 and Q_5) to isolate it from noise on the unregulated supply. This separate bias supply permits the linear pass transistor, Q_3, to operate right down into saturation. The collector of Q_3 is supplied by the output of a switching regulator which is made enough higher than the linear regulator output to allow for the maximum overshoot of the switching regulator plus the saturation of Q_3.

SUMMARY

A number of switching regulator circuits which use a readily-available monolithic voltage regulator as the voltage reference and control circuitry have been described. These regulators are useful over a 2V to 30V range for either positive or negative supplies. Although the discussion was limited to circuits providing maximum output currents from 100 mA to 5A, it is possible to obtain even higher output currents. The output current is, in fact, limited by the discrete components — not by the basic design or the integrated circuit.

The majority of the circuits shown were self-oscillating regulators; however, a method of driving the regulator in synchronism with an external clock signal was given. In addition, circuits which provide overload protection, limiting both the output current as well as the power dissipation, were presented. The performance of the regulator circuits was described in detail, and a design procedure was outlined. Suggestions were also made on the selection of components for switching regulators.

The circuits which have been described here for the LM100 work equally well with the LM200 or the LM300. These devices are identical, except that the LM200 is specified over a –25°C to 85°C temperature range and the LM300 is specified from 0°C to 70°C instead of the –55°C to 125°C temperature range for the LM100.

Drift Compensation Techniques for Integrated DC Amplifiers

National Semiconductor
Application Note 3
November 1967

INTRODUCTION

With DC amplifiers, it is usually possible to substantially improve drift performance by using additional circuitry along with some form of adjustment. In fact, one of the reasons that discrete-component operational amplifiers have better input current specifications than monolithic amplifiers is that current compensation is used. Monolithic circuits cannot incorporate these techniques because it is not possible to select components or make adjustments. These adjustments can, however, be made external to the amplifier. This article will discuss a number of compensation methods which can substantially reduce the input currents of monolithic amplifiers, especially in limited-temperature-range applications.

Bias current compensation reduces offset and drift when the amplifier is operated from high source resistances. With low source resistances, such as a thermocouple, the drift contribution due to bias current can be made quite small. In this case, the offset voltage drift becomes important.

A technique is presented here by which offset voltage drifts better than 0.5 $\mu V/^\circ C$ can be realized. The compensation technique involves only a single room-temperature balance adjustment. Therefore, chopper-stabilized performance can be realized, with low source resistances, in a fairly-simple amplifier without tedious cut-and-try compensation methods.

BIAS CURRENT COMPENSATION

The simplest and most effective way of compensating for bias currents is shown in Figure 1. Here, the offset produced by the bias current on the inverting input is cancelled by the offset voltage produced across the variable resistor, R_3. The main advantage of this scheme, besides its simplicity, is that the bias currents of the two input transistors tend to track well over temperature so that low drift is also achieved. The disadvantage of the method is that a given compensation setting works only with fixed feedback resistors, and the compensation must be readjusted if the equivalent parallel resistance of R_1 and R_2 is changed.

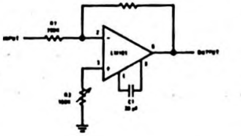


FIGURE 1. Summing Amplifier with Bias-Current Compensation for Fixed Source Resistances.

Figure 2 shows a similar circuit for a non-inverting amplifier. The offset voltage produced across the DC resistance of the source due to the input current is cancelled by the drop across R_3. For proper adjustment range, R_3 should have a maximum value about three times the source resistance and the equivalent parallel resistance of R_1 and R_2 should be less than one-third the input source resistance.

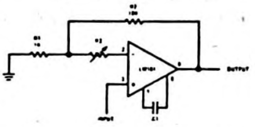


FIGURE 2. Non-Inverting Amplifier with Bias-Current Compensation for Fixed Source Resistances.

This circuit has the same advantages as that in Figure 1, however, it can only be used when the input source has a fixed DC resistance. In many applications, such as long-interval integrators, sample-and-hold circuits, switched-gain amplifiers or voltage followers operating from unknown source, the source impedance is not defined. In these cases other compensation schemes must be used.

Figure 3 gives a compensation technique which does not depend upon having a fixed source resistance. A current is injected into the input terminal from the base of a PNP transistor. Since NPN input transistors are used on the integrated amplifier,* the base current of the PNP balances out the base current of the NPN. Further, since a silicon-planar PNP transistor has approximately the same current-gain versus temperature characteristic as the integrated transistors, an improvement in temperature drift will also be realized.† However, perfect

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*This is true for all monolithic operational amplifiers presently available.

†If the operational amplifier uses a Darlington input stage, however, the drift compensation will not be nearly as good.

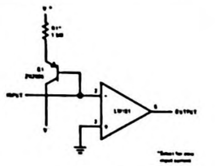

FIGURE 3. Summing Amplifier with Bias-Current Compensation.

compensation should not be expected because of unit-to-unit variations in the temperature characteristics of both the PNP transistor and the integrated circuit.

Although the circuit in Figure 3 works well for the summing amplifier connection, it does have limitations in other applications, It could, for example, be used for the voltage follower configuration by connecting the base of the PNP to the non-inverting input. However, this would reduce the input impedance (to about 150 MΩ) because the current supplied by the PNP will vary with the input voltage level.

If this characteristic is objectionable, the more-complicated circuit shown in Figure 4 can be used.

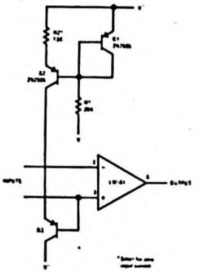

FIGURE 4. Bias-Current Compensation for Non-Inverting Amplifier Operated Over Large Common Mode Range.

The emitter of the PNP transistor is fed from a current source so that the compensating current does not vary with input-voltage level. The design of the current source is such as to give it about the same characteristics as those on the input stage of the better monolithic amplifiers‡ to give closer compensation with changes in temperature and supply voltage. The circuit makes use of the emitter base voltage differential between two transistors operated at different collector currents.[1,2] Although it is recommended in the references that these transistors be well matched, it is not really necessary since the devices are operated at much different collector currents.

Figure 5 shows another compensation scheme for the voltage follower connection. This circuit is much simpler than that shown in Figure 4, but the temperature compensation is not quite as good. The compensating current is obtained through a resistor connected across a diode which is bootstrapped to the output. The diode acts as a regulator so that the compensating current does not change appreciably with signal level, giving input impedances about 1000 MΩ. The negative temperature coefficient of the diode voltage also provides some temperature compensation.

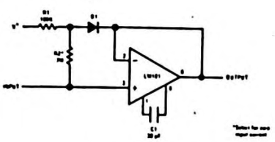

FIGURE 5. Voltage Follower with Bias-Current Compensation.

All the circuits discussed thus far have been tailored for particular applications. Figure 6 shows a completely-general scheme wherein both inputs are current compensated over the full common mode range as well as against power supply and temperature variations. This circuit is suitable for use either as a summing amplifier or as a non-inverting amplifier. It is not required that the DC impedance seen by both inputs be equal, although lower drift can be expected if they are.

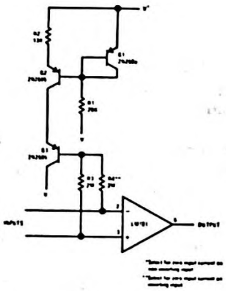

FIGURE 6. Bias-Current Compensation for Differential Inputs.

As was mentioned earlier, all the bias compensation circuits require adjustment. With the circuits in Figures 1 and 2, this is merely a matter of adjusting the potentiometer for zero output with zero input. It is not so simple with the other circuits, however. For one, it is difficult to use potentiometers because a very wide range of resistance values are required to accommodate expected unit-to-unit variations. Resistor selection must therefore be used. Test circuits for selecting bias compensation resistors are given in Figure 7.

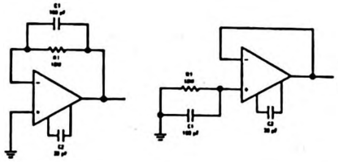

FIGURE 7. Test Circuits for Selecting Bias-Compensation Resistors.

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‡The 709 and the LM101.

OFFSET VOLTAGE COMPENSATION

The highly predictable behavior of the emitter-base voltage of transistors has suggested a unique drift compensation method; it is shown in Reference 3 that the offset voltage drift of a differential transistor pair can be reduced by about an order of magnitude by unbalancing the collector currents such that the initial offset voltage is zero. The basis for this comes from the equation for the emitter-base voltage differential of two transistors operating at the same temperature:

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{S2}}{I_{S1}} - \frac{kT}{q} \log_e \frac{I_{C2}}{I_{C1}} \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, I_S is a constant which depends only on how the transistor is made and I_C is the collector current. This equation is derived in Reference 2.

It is worthwhile noting here that these expressions make no assumptions about the current gain of the transistors. It is shown in Reference 5 and 6 that the emitter-base voltage is a function of collector current not emitter current. Therefore, the balance will not be upset by base current (except for interaction with the DC-source resistance).

The first term in Equation (1) is the offset voltage of the two transistors for equal collector currents. It can be seen that this offset voltage is directly proportional to the absolute temperature — a fact which is substantiated by experiment.[4] The second term is the change of offset voltage which arises from operating the transistors at unequal collector currents. For a fixed ratio of collector currents, this is also proportional to absolute temperature. Hence, if the collector currents are unbalanced in a fixed ratio to give a zero emitter-base voltage differential, the temperature drift will also be zero.

Experiment indicates that this is indeed true. Thermal drifts less than 100 µV over the −55°C to +125°C temperature range have been realized consistently. In order to obtain these low drifts, however, it is almost necessary to use a monolithic transistor pair, since a 0.05°C temperature differential will give a 100 µV drift. With a monolithic pair, the physical proximity of the devices as well as the high thermal conductivity of silicon holds this differential to an absolute minimum.

For low drift, the transistors must operate from a low enough source resistance that the voltage drop across the source due to base current (or base current differential if both bases see the same resistance) is insignificant. Furthermore, the transistors must be operated at a low enough collector current that the emitter-contact and base-spreading resistances are negligible, since Equation (1) assumes that they are zero.

A complete amplifier using this principle is shown in Figure 8. A monolithic transistor pair is used as a preamplifier for a conventional operational amplifier. A null potentiometer, which is set for zero output for zero input, unbalances the collector load resistors of the transistor pair such that the collector currents are unbalanced for zero offset. This gives minimum drift. An interesting feature of the circuit is that the performance is relatively unaffected by supply voltage variations: a 1V change in either supply causes an offset voltage change of about 10 µV. This happens because neither term in Equation (1) is affected by the magnitude of the collector currents.

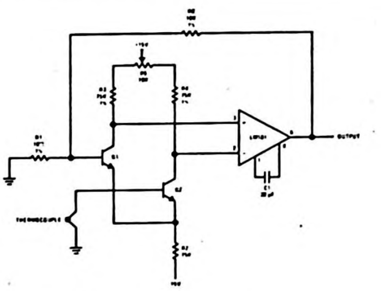

FIGURE 8. Example of a DC Amplifier Using the Drift-Compensation Technique.

In order to get low drift, it is necessary that the gain of the preamplifier be high enough so that the drift of the operational amplifier does not degrade performance. The gain can be determined from the expression for the transconductance of the input transistors:

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT} \qquad (2)$$

The voltage gain is

$$A_V = \frac{\partial V_{OUT}}{\partial V_{IN}} \qquad (3)$$

$$= \frac{\partial I_C}{\partial V_{BE}} R_L \qquad (4)$$

where R_L is the average value of the two collector load resistors on the input stage and I_C is the average of the two collector currents.

Substituting Equation (2), this becomes

$$A_V = \frac{qI_C R_L}{kT} \qquad (5)$$

$$= \frac{qV_{RL}}{kT} \qquad (6)$$

The input referred drift is then

$$\Delta V_{IN} = \frac{\Delta V_{OS} + R_L\, \Delta I_{OS}}{A_V}$$

where ΔV_{OS} is the offset voltage drift of the operational amplifier and ΔI_{OS} is its offset current drift.

Using Equation (7),

$$\Delta V_{IN} = \frac{kT\,(\Delta V_{OS} + R_L \Delta I_{OS})}{qV_{RL}} \qquad (8)$$

With the circuit shown in Figure 8, Equation (8) gives a 25 μV input-referred drift for every 10 mV of offset voltage drift or for every 100 nA of offset current drift. It is obvious from this that the offset current drift is most important if an operational amplifier with bipolar input transistors is used.

Another important consideration is the matching of the collector load resistors on the preamplifier stage. A 0.1-percent imbalance in the load resistors due to thermal mismatches or any other cause will produce a 25 μV shift in offset. This includes the balancing potentiometer which can introduce an error that will depend on how far it is set off mid-point if it has a different temperature coefficient than the resistors.

The most obvious use of this type of low drift amplifier is with thermocouples, magnetometers, current shunts, wire strain gauges or similar signal sources where very low drift is required and the source resistance is low enough that the bias currents do not cause a problem. The 0.5 to 1 μV/°C drift* realized with this relatively simple amplifier over a −55°C to +125°C temperature range compares favorably with the drift figures achieved with chopper amplifiers: 0.4 μV/°C for mechanical choppers, 0.5 μV/°C with photoelectric choppers over a 0°C to 55°C temperature range and 2 μV/°C with field-effect-transistor choppers over a −55°C to +125°C temperature range. In order to give some appreciation of the level of performance, it is interesting to note that no substantial improvement in performance would be realized by operating the amplifier in a temperature-controlled oven. Any improvement would be masked by various thermoelectric effects not directly associated with the amplifier unless extreme care were taken in the choice of input lead material, the method of making connections and the balancing of thermal paths. These factors are, in fact, important when making oven tests to verify the drift of the amplifier since thermoelectric effects can easily produce drift voltages larger than those of the amplifier if they are not properly handled.

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*Drifts of 0.05 μV/°C over a 0-50°C temperature range were reported in Reference 3 using matched discrete transistors in one can.

SUMMARY

A number of compensation circuits designed to increase the DC resolution of monolithic operational amplifiers have been presented. Both current compensation techniques for high impedance levels as well as methods of achieving chopper-stabilized drift performance at low impedance levels have been covered.

Fairly-simple current compensation which requires that the impedance levels be fixed have been described along with compensation which is effective in cases where the source impedance is not well defined. This latter category includes long-interval integrators, sample-and-hold circuits, switched-gain amplifiers or voltage followers which operate from an unknown source. The application of these schemes is generally limited to integrated amplifiers since modular amplifiers almost always incorporate current compensation.

The drift-reduction techniques provide stabilities better than 0.5 μV/°C for low impedance sources, such as thermocouples, current shunts or strain gauges. With a properly designed circuit, compensation depends only on a single room temperature adjustment, so excellent performance can be obtained from a fairly-simple amplifier.

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Monolithic Op Amp — The Universal Linear Component

National Semiconductor
Application Note 4
April 1968

AN-4 Monolithic Op Amp — The Universal Linear Component

INTRODUCTION

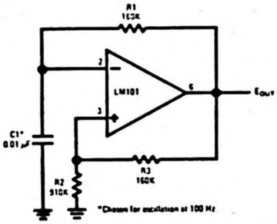
Operational amplifiers are undoubtedly the easiest and best way of performing a wide range of linear functions from simple amplification to complex analog computation. The cost of monolithic amplifiers is now less than $2.00, in large quantities, which makes it attractive to design them into circuits where they would not otherwise be considered. Yet low cost is not the only attraction of monolithic amplifiers. Since all components are simultaneously fabricated on one chip, much higher circuit complexities than can be used with discrete amplifiers are economical. This can be used to give improved performance. Further, there are no insurmountable technical difficulties to temperature stabilizing the amplifier chip, giving chopper-stabilized performance with little added cost.

Operational amplifiers are designed for high gain, low offset voltage and low input current. As a result, dc biasing is considerably simplified in most applications; and they can be used with fairly simple design rules because many potential error terms can be neglected. This article will give examples demonstrating the range of usefulness of operational amplifiers in linear circuit design. The examples are certainly not all-inclusive, and it is hoped that they will stimulate even more ideas from others. A few practical hints on preventing oscillations in operational amplifiers will also be given since this is probably the largest single problem that many engineers have with these devices.

Although the designs presented use the LM101 operational amplifier and the LM102 voltage follower produced by National Semiconductor, most are generally applicable to all monolithic devices if the manufacturer's recommended frequency compensation is used and differences in maximum ratings are taken into account. A complete description of the LM101 is given elsewhere;[1] but, briefly, it differs from most other monolithic amplifiers, such as the LM709,[2] in that it has a ±30V differential input voltage range, a +15V, −12V common mode range with ±15V supplies and it can be compensated with a single 30 pF capacitor. The LM102,[3] which is also used here, is designed specifically as a voltage follower and features a maximum input current of 10 nA and a 10V/µs slew rate.

OPERATIONAL-AMPLIFIER OSCILLATOR

The free-running multivibrator shown in Figure 1 is an excellent example of an application where one does not normally consider using an operational amplifier. However, this circuit operates at low frequencies with relatively small capacitors because it can use a longer portion of the capacitor time constant since the threshold point of the operational amplifier is well determined. In addition, it has a completely-symmetrical output waveform along with a buffered output, although the symmetry can be varied by returning R2 to some voltage other than ground.



*Chosen for oscillation at 100 Hz

FIGURE 1. Free-Running Multivibrator

Another advantage of the circuit is that it will always self start and cannot hang up since there is more dc negative feedback than positive feedback. This can be a problem with many "textbook" multivibrators.

Since the operational amplifier is used open loop, the usual frequency compensation components are not required since they will only slow it down. But even without the 30 pF capacitor, the LM101 does have speed limitations which restrict the use of this circuit to frequencies below about 2 kHz.

The large input voltage range of the LM101 (both differential and single ended) permits large voltage swings on the input so that several time constants of the timing capacitor, C1, can be used. With most other amplifiers, R2 must be reduced to keep from exceeding these ratings, which requires that C1 be increased. Nonetheless, even when large values are needed for C1, smaller polarized capacitors may be used by returning them to the positive supply voltage instead of ground.

LEVEL SHIFTING AMPLIFIER

Frequently, in the design of linear equipment, it is necessary to take a voltage which is referred to some dc level and produce an amplified output which is referred to ground. The most straightforward way of doing this is to use a differential amplifier similar to that shown in Figure 2a. This circuit, however, has the disadvantages that the signal source is loaded by current from the input divider, R3 and R4, and that the feedback resistors must be very well matched to prevent erroneous outputs from the common mode input signal.

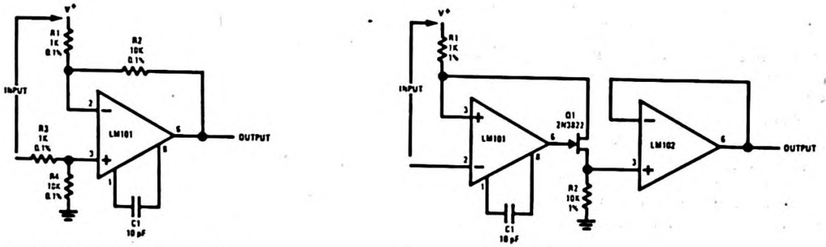
A circuit which does not have these problems is shown in Figure 2b. Here, an FET transistor on the output of the operational amplifier produces a voltage drop across the feedback resistor, R1, which is equal to the input voltage. The voltage across R2 will then be equal to the input voltage multiplied by the ratio, R2/R1; and the common mode rejection will be as good as the basic rejection of the amplifier, independent of the resistor tolerances. This voltage is buffered by an LM102 voltage follower to give a low impedance output.

An advantage of the LM101 in this circuit is that it will work with input voltages up to its positive supply voltages as long as the supplies are less than ±15V.

VOLTAGE COMPARATORS

The LM101 is well suited to comparator applications for two reasons: first, it has a large differential input voltage range and, second, the output is easily clamped to make it compatible with various driver and logic circuits. It is true that it doesn't have the speed of the LM710[4] (10 μs versus 40 ns, under equivalent conditions); however, in many linear applications speed is not a problem and the lower input currents along with higher voltage capability of the LM101 is a tremendous benefit.

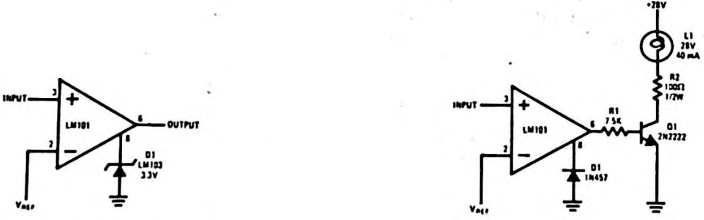
Two comparator circuits using the LM101 are shown in Figure 3. The one in Figure 3a shows a clamping scheme which makes the output signal directly compatible with DTL or TTL integrated circuits. An LM103 breakdown diode clamps the output at 0V or 4V in the low or high states, respectively. This particular diode was chosen because it has a sharp breakdown and low equivalent capacitance. When working as a comparator, the amplifier operates open loop so normally no frequency compensation is needed. Nonetheless, the stray capacitance between Pins 5 and 6 of the amplifier should be minimized to prevent low level oscillations when the comparator is in the active region. If this becomes a problem, a 3 pF capacitor on the normal compensation terminals will eliminate it.



a. Standard Differential Amplifier

b. Level-Isolation Amplifier

FIGURE 2. Level-Shifting Amplifiers



a. Comparator for Driving DTL and TTL Integrated Circuits

b. Comparator and Lamp Driver

FIGURE 3. Voltage Comparator Curcuits

Figure 3b shows the connection of the LM101 as a comparator and lamp driver. Q1 switches the lamp, with R2 limiting the current surge resulting from turning on a cold lamp. R1 determines the base drive to Q1 while D1 keeps the amplifier from putting excessive reverse bias on the emitter-base junction of Q1 when it turns off.

MORE OUTPUT CURRENT SWING

Because almost all monolithic amplifiers use class-B output stages, they have good loaded output voltage swings, delivering ±10V at 5 mA with ±15V supplies. Demanding much more current from the integrated circuit would require, for one, that the output transistors be made considerably larger. In addition, the increased dissipation could give rise to troublesome thermal gradients on the chip as well as excessive package heating in high-temperature applications. It is therefore advisable to use an external buffer when large output currents are needed.

A simple way of accomplishing this is shown in Figure 4. A pair of complementary transistors are used on the output of the LM101 to get the increased current swing. Although this circuit does have a dead zone, it can be neglected at frequencies below 100 Hz because of the high gain of the amplifier. R1 is included to eliminate parasitic oscillations from the output transistors. In addition, adequate bypassing should be used on the collectors of the output transistors to insure that the output signal is not coupled back into the amplifier. This circuit does not have current limiting, but it can be added by putting 50Ω resistors in series with the collectors of Q1 and Q2.

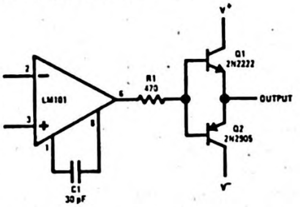


FIGURE 4. High Current Output Buffer

AN FET AMPLIFIER

For ambient temperatures less than about 70°C, junction field effect transistors can give exceptionally low input currents when they are used on the input stage of an operational amplifier. However, monolithic FET amplifiers are not now available since it is no simple matter to diffuse high quality FET's on the same chip as the amplifier. Nonetheless, it is possible to make a good FET amplifier using a discrete FET pair in conjunction with a monolithic circuit.

Such a circuit is illustrated in Figure 5. A matched FET pair, connected as source followers, is put in front of an integrated operational amplifier. The composite circuit has roughly the same gain as the integrated circuit by itself and is compensated for unity gain with a 30 pF capacitor as shown. Although it works well as a summing amplifier, the circuit leaves something to be desired in applications requiring high common mode rejection. This happens both because resistors are used for current sources and because the FET's by themself do not have good common mode rejection.

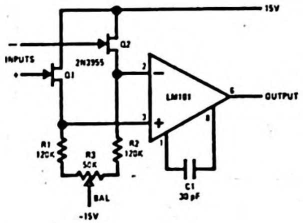


FIGURE 5. FET Operational Amplifier

STORAGE CIRCUITS

A sample-and-hold circuit which combines the low input current of FET's with the low offset voltage of monolithic amplifiers is shown in Figure 6. The circuit is a unity gain amplifier employing an operational amplifier and an FET source follower. In operation, when the sample switch, Q2, is turned on, it closes the feedback loop to make the output equal to the input, differing only by the offset voltage of the LM101. When the switch is opened, the charge stored on C2 holds the output at a level equal to the last value of the input voltage.

Some care must be taken in the selection of the holding capacitor. Certain types, including paper and mylar, exhibit a polarization phenomenon which causes the sampled voltage to drop off by about 50 mV, and then stabilize, when the capacitor is exercised over a 5V range during the sample interval. This drop off has a time constant in the order of seconds. The effect, however, can be minimized by using capacitors with teflon, polyethylene, glass or polycarbonate dielectrics.

Although this circuit does not have a particularly low output resistance, fixed loads do not upset the accuracy since the loading is automatically compensated for during the sample interval. However, if the load is expected to change after sampling, a buffer such as the LM102 must be added between the FET and the output.

A second pole is introduced into the loop response of the amplifier by the switch resistance and the holding capacitor, C2. This can cause problems with overshoot or oscillation if it is not compensated for by adding a resistor, R1, in series with the LM101 compensation capacitor such that the breakpoint of the R1C1 combination is roughly equal to that of the switch and the holding capacitor.

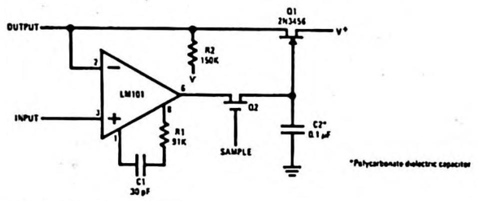


FIGURE 6. Low Drift Sample and Hold

It is possible to use an MOS transistor for Q1 without worrying about the threshold stability. The threshold voltage is balanced out during every sample interval so only the short-term threshold stability is important. When MOS transistors are used along with mechanical switches, drift rates less than 10 mV/min can be realized.

Additional features of the circuit are that the amplifier acts as a buffer so that the circuit does not load the input signal. Further, gain can also be provided by feeding back to the inverting input of the LM101 through a resistive divider instead of directly.

The peak detector in Figure 7 is similar in many respects to the sample-and-hold circuit. A diode is used in place of the sampling switch. Connected as shown, it will conduct whenever the input is greater than the output, so the output will be equal to the peak value of the input voltage. In this case, an LM102 is used as a buffer for the storage capacitor, giving low drift along with a low output resistance.

As with the sample and hold, the differential input voltage range of the LM101 permits differences between the input and output voltages when the circuit is holding.

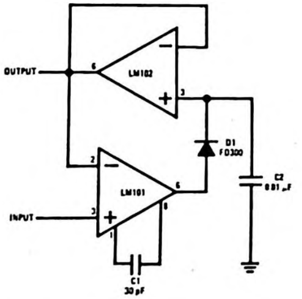


FIGURE 7. Positive Peak Detector with Buffered Output

NON-LINEAR AMPLIFIERS

When a non-linear transfer function is needed from an operational amplifier, many methods of obtaining it present themself. However, they usually require diodes and are therefore difficult to temperature compensate for accurate breakpoints. One way of getting around this is to make the output swing so large that the diode threshold is negligible by comparison, but this is not always practical.

A method of producing very sharp, temperature-stable breakpoints in the transfer function of an operational amplifier is shown in Figure 8. For small input signals, the gain is determined by R1 and R2. Both Q2 and Q3 are conducting to some degree, but they do not affect the gain because their current gain is high and they do not feed any appreciable current back into the summing mode. When the output voltage rises to 2V (determined by R3, R4 and V^-), Q3 draws enough current to saturate, connecting R4 in parallel with R2. This cuts the gain in half. Similarly, when the output voltage rises to 4V, Q2 will saturate, again halving the gain.

Temperature compensation is achieved in this circuit by including Q1 and Q4. Q4 compensates the emitter-base voltage of Q2 and Q3 to keep the voltage across the feedback resistors, R4 and R6, very nearly equal to the output voltage while Q1 compensates for the emitter base voltage of these transistors as they go into saturation, making the voltage across R3 and R5 equal to the negative supply voltage. A detrimental effect of Q4 is that it causes the output resistance of the amplifier to increase at high output levels. It may therefore be necessary to use an output buffer if the circuit must drive an appreciable load.

SERVO PREAMPLIFIER

In certain servo systems, it is desirable to get the rate signal required for loop stability from some sort of electrical, lead network. This can, for example, be accomplished with reactive elements in the feedback network of the servo preamplifier.

Many saturating servo amplifiers operate over an extremely wide dynamic range. For example, the maximum error signal could easily be 1000 times the signal required to saturate the system. Cases like this create problems with electrical rate networks because they cannot be placed in any part

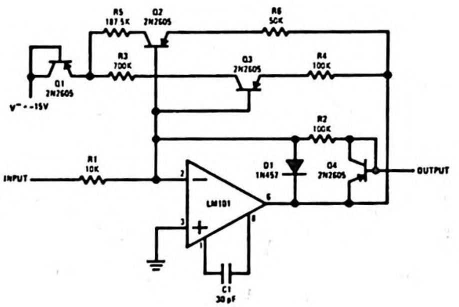


FIGURE 8. Nonlinear Operational Amplifier with Temperature-Compensated Breakpoints

of the system which saturates. If the signal into the rate network saturates, a rate signal will only be developed over a narrow range of system operation; and instability will result when the error becomes large. Attempts to place the rate networks in front of the error amplifier or make the error amplifier linear over the entire range of error signals frequently gives rise to excessive dc error from signal attenuation.

These problems can be largely overcome using the kind of circuit shown in Figure 9. This amplifier operates in the linear mode until the output voltage reaches approximately 3V with 30 μA output current from the solar cell sensors. At this point the breakdown diodes in the feedback loop begin to conduct, drastically reducing the gain. However, a rate signal will still be developed because current is being fed back into the rate network (R1, R2 and C1) just as it would if the amplifier had remained in the linear operating region. In fact, the amplifier will not actually saturate until the error current reaches 6 mA, which would be the same as having a linear amplifier with a ±600V output swing.

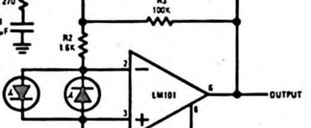


FIGURE 9. Saturating Servo Preamplifier with Rate Feedback

COMPUTING CIRCUITS

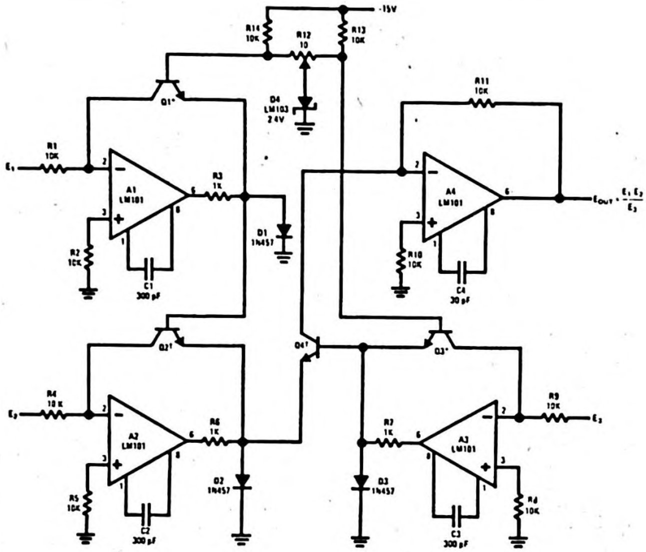
In analog computation it is a relatively simple matter to perform such operations as addition, subtraction, integration and differentiation by incorporating the proper resistors and capacitors in the feedback circuit of an amplifier. Many of these circuits are described in reference 5. Multiplication and division, however, are a bit more difficult. These operations are usually performed by taking the logarithms of the quantities, adding or subtracting as required and then taking the antilog.

At first glance, it might appear that obtaining the log of a voltage is difficult; but it has been shown[6] that the emitter-base voltage of a silicon transistor follows the log of its collector current over as many as nine decades. This means that common transistors can be used to perform the log and antilog operations.

A circuit which performs both multiplication and division in this fashion is shown in Figure 10. It gives an output which is proportional to the product of two inputs divided by a third, and it is about the same complexity as a divider alone.

The circuit consists of three log converters and an antilog generator. Log converters similar to these have been described elsewhere,[7] but a brief description follows. Taking amplifier A1, a logging transistor, Q1, is inserted in the feedback loop such that its collector current is equal to the input voltage divided by the input resistor, R1. Hence, the emitter-base voltage of Q1 will vary as the log of the input voltage, E1.

A2 is a similar amplifier operating with logging transistor, Q2. The emitter-base junctions of Q1 and Q2 are connected in series, adding the log voltages. The third log converter produces the log of E3. This is series-connected with the antilog transistor, Q4; and the combination is hooked in parallel with the output of the other two log convertors. Therefore, the emitter-base of Q4 will see the log of E3 subtracted from the sum of the logs of E1 and E2. Since the collector current of a transistor varies as the exponent of the emitter-base voltage, the collector current of Q4 will be proportional to the product of E1 and E2 divided by E3. This current is fed to the summing amplifier, A4, giving the desired output.



*,†2N3728 matched pairs

FIGURE 10. Analog Multiplier/Divider

This circuit can give 1-percent accuracy for input voltages from 500 mV to 50V. To get this precision at lower input voltages, the offset of the amplifiers handling them must be individually balanced out. The zener diode, D4, increases the collector-base voltage across the logging transistors to improve high current operation. It is not needed, and is in fact undesirable, when these transistors are running at currents less than 0.3 mA. At currents above 0.3 mA, the lead resistances of the transistors can become important (0.25Ω is 1-percent at 1 mA) so the transistors should be installed with short leads and no sockets.

An important feature of this circuit is that its operation is independent of temperature because the scale factor change in the log converter with temperature is compensated by an equal change in the scale factor of the antilog generator. It is only required that Q1, Q2, Q3 and Q4 be at the same temperature. Dual transistors should be used and arranged as shown in the figure so that thermal mismatches between cans appear as inaccuracies in scale factor (0.3-percent/°C) rather than a balance error (8-percent/°C). R12 is a balance potentiometer which nulls out the offset voltages of all the logging transistors. It is adjusted by setting all input voltages equal to 2V and adjusting for a 2V output voltage.

The logging transistors provide a gain which is dependent on their operating level, which complicates frequency compensation. Resistors (R3, R6 and R7) are put in the amplifier output to limit the maximum loop gain, and the compensation capacitor is chosen to correspond with this gain. As a result, the amplifiers are not especially designed for speed, but techniques for optimizing this parameter are given in reference 6.

Finally, clamp diodes D1 through D3, prevent exceeding the maximum reverse emitter-base voltage of the logging transistors with negative inputs.

ROOT EXTRACTOR*

Taking the root of a number using log converters is a fairly simple matter. All that is needed is to take the log of a voltage, divide it by, say 1/2 for the square root, and then take the antilog. A circuit which accomplishes this is shown in Figure 11. A1 and Q1 form the log converter for the input signal. This feeds Q2 which produces a level shift to give zero voltage into the R4, R5 divider for a 1V input. This divider reduces the log voltage by the ratio for the root desired and drives the buffer amplifier, A2. A2 has a second level shifting diode, Q3, its feedback network which gives the output voltage needed to get a 1V output from the antilog generator, consisting of A3 and Q4, with a unity

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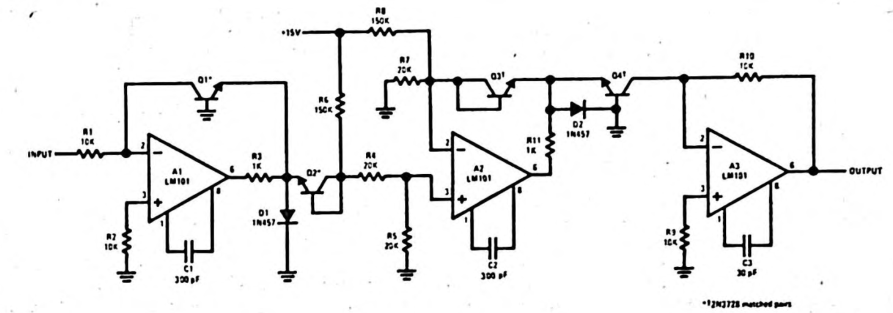
*The "extraction" used here doubtless has origin in the dental operation most of us would fear less than having to find even a square root without tables or other aids.



+15V
R8
150K
R7
20K
R6
150K
Q1*
Q2*
Q3†
Q4†
R1
10K
INPUT
2
3
A1
LM101
6
8
1
R2
10K
C1
300 pF
R3
1K
D1
1N457
R4
20K
R5
20K
A2
LM101
C2
300 pF
R11
1K
D2
1N457
R10
10K
A3
LM101
R9
10K
C3
30 pF
OUTPUT
*†2N3728 matched pairs

FIGURE 11. Root Extractor

input. The offset voltages of the transistors are nulled out by imbalancing R6 and R8 to give 1V output for 1V input, since any root of one is one.

Q2 and Q3 are connected as diodes in order to simplify the circuitry. This doesn't introduce problems because both operate over a very limited current range, and it is really only required that they match. R7 is a gain-compensating resistor which keeps the currents in Q2 and Q3 equal with changes in signal level.

As with the multiplier/divider, the circuit is insensitive to temperature as long as all the transistors are at the same temperature. Using transistor pairs and matching them as shown minimizes the effects of gradients.

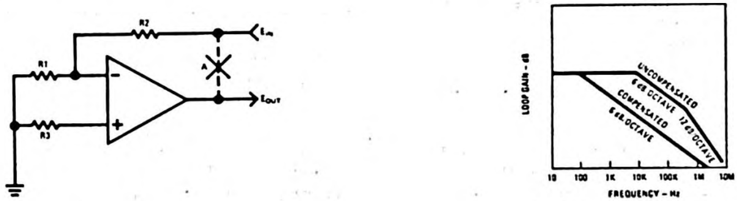
The circuit has 1-percent accuracy for input voltages between 0.5 and 50V. For lower input voltages, A1 and A3 must have their offsets balanced out individually.

FREQUENCY COMPENSATION HINTS

The ease of designing with operational amplifiers sometimes obscures some of the rules which must be followed with any feedback amplifier to keep it from oscillating. In general, these problems stem from stray capacitance, excessive capacitive loading, inadequate supply bypassing or improper frequency compensation.

In frequency compensating an operational amplifier, it is best to follow the manufacturer's recommendations. However, if operating speed and frequency response is not a consideration, a greater stability margin can ususally be obtained by increasing the size of the compensation capacitors. For example, replacing the 30 pF compensation capacitor on the LM101 with a 300 pF capacitor will make it ten times less susceptible to oscillation problems in the unity-gain connection. Similarly, on the LM709, using 0.05 μF, 1.5 kΩ, 2000 pF and 51Ω components instead of 5000 pF, 1.5 kΩ, 200 pF and 51Ω will give 20 dB more stability margin. Capacitor values less than those specified by the manufacturer for a particular gain connection should not be used since they will make the amplifier more sensitive to strays and capacitive loading, or the circuit can even oscillate with worst-case units.

The basic requirement for frequency compensating a feedback amplifier is to keep the frequency roll-off of the loop gain from exceeding 12 dB/octave when it goes through unity gain. Figure 12a shows what is meant by loop gain. The feedback loop is broken at the output, and the input sources are replaced by their equivalent impedance. Then the response is measured such that the feedback network is included.



R2
R1
R3
A
E_{in}
E_{OUT}
LOOP GAIN – dB
UNCOMPENSATED
6 dB OCTAVE
12 dB OCTAVE
COMPENSATED
6 dB OCTAVE
10
100
1K
10K
100K
1M
10M
FREQUENCY – Hz

a. Measuring Loop Gain

b. Typical Response

FIGURE 12. Illustrating Loop Gain

Figure 12b gives typical responses for both uncompensated and compensated amplifiers. An uncompensated amplifier generally rolls off at 6 dB/octave, then 12 dB/octave and even 18 dB/octave as various frequency-limiting effects within the amplifier come into play. If a loop with this kind of response were closed, it would oscillate. Frequency compensation causes the gain to roll off at a uniform 6 dB/octave right down through unity gain. This allows some margin for excess rolloff in the external circuitry.

Some of the external influences which can affect the stability of an operational amplifier is shown in Figure 13. One is the load capacitance which can come from wiring, cables or an actual capacitor on the output. This capacitance works against the output impedance of the amplifier to attenuate high frequencies. If this added rolloff occurs before the loop gain goes through zero, it can cause instability. It should be remembered that this single rolloff point can give more than 6 dB/octave rolloff since the output impedance of the amplifier can be increasing with frequency.

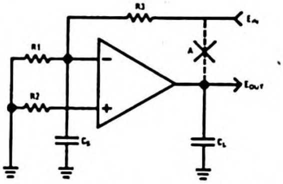


FIGURE 13. External Capacitances That Affect Stability

A second source of excess rolloff is stray capacitance on the inverting input. This becomes extremely important with large feedback resistors as might be used with an FET-input amplifier. A relatively simple method of compensating for this stray capacitance is shown in Figure 14: a lead capacitor, C1, put across the feedback resistor. Ideally, the ratio of the stray capacitance to the lead capacitor should be equal to the closed-loop gain of the amplifier. However, the lead capacitor can be made larger as long as the amplifier is compensated for unity gain. The only disadvantage of doing this is that it will reduce the bandwidth of the amplifier. Oscillations can also result if there is a large resistance on the non-inverting input of the amplifier. The differential input impedance of the amplifier falls off at high frequencies (especially with bipolar input transistors) so this resistor can produce troublesome rolloff if it is much greater than 10K, with most amplifiers. This is easily corrected by bypassing the resistor to ground.

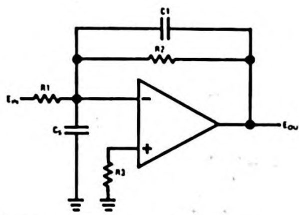


FIGURE 14. Compensating Stray Input Capacitance

When the capacitive load on an integrated amplifier is much greater than 100 pF, some consideration must be given to its effect on stability. Even though the amplifier does not oscillate readily, there may be a worst-case set of conditions under which it will. However, the amplifier can be stabilized for any value of capacitive loading using the circuit shown in Figure 15. The capacitive load is isolated from the output of the amplifier with R4 which has a value of 50Ω to 100Ω for both the LM101 and the LM709. At high frequencies, the feedback path is through the lead capacitor, C1, so that the lag produced by the load capacitance does not cause instability. To use this circuit, the amplifier must be compensated for unity gain, regardless of the closed loop dc gain. The value of C1 is not too important, but at a minimum its capacitive reactance should be one-tenth the resistance of R2 at the unity-gain crossover frequency of the amplifier.

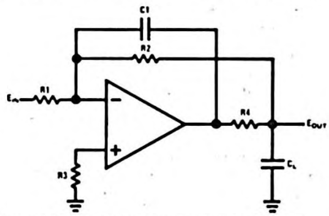


FIGURE 15. Compensating for Very Large Capacitive Loads

When an operational amplifier is operated open loop, it might appear at first glance that it needs no frequency compensation. However, this is not always the case because the external compensation is sometimes required to stabilize internal feedback loops.

The LM101 will not oscillate when operated open loop, although there may be problems if the capacitance between the balance terminal on pin 5 and the output is not held to an absolute minimum. Feedback between these two points is regenerative if it is not balanced out with a larger feedback capacitance across the compensation terminals. Usually a 3 pF compensation capacitor will completely eliminate the problem. The LM709 will oscillate when operated open loop unless a 10 pF capacitor is connected across the input compensation terminals and a 3 pF capacitor is connected on the output compensation terminals.

Problems encountered with supply bypassing are insidious in that they will hardly ever show up in a Nyquist plot. This problem has not really been thoroughly investigated, probably because one sure cure is known: bypass the positive and negative supply terminals of each amplifier to ground with at least a 0.01 μF capacitor.

For example, a LM101 can take over 1 mH inductance in either supply lead without oscillation. This should not suggest that they should be run without bypass capacitors. It has been established that 100 LM101's on a single printed circuit board with common supply busses will oscillate if the supplies are not bypassed about every fifth device. This happens even though the inputs and outputs are completely isolated.

The LM709, on the other hand, will oscillate under many load conditions with as little as 18 inches of wire between the negative supply lead and a bypass capacitor. Therefore, it is almost essential to have a set of bypass capacitors for every device.

Operational amplifiers are specified for power supply rejection at frequencies less than the first break frequency of the open loop gain. At higher frequencies, the rejection can be reduced depending on how the amplifier is frequency compensated. For both the LM101 and LM709, the rejection of high frequency signals on the positive supply is excellent. However, the situation is different for the negative supplies. These two amplifiers have compensation capacitors from the output down to a signal point which is referred to the negative supply, causing the high frequency rejection for the negative supply to be much reduced. It is therefore important to have sufficient bypassing on the negative supply to remove transients if they can cause trouble appearing on the output. One fairly large (22 μF) tantalum capacitor on the negative power lead for each printed-circuit card is usually enough to solve potential problems.

When high-current buffers are used in conjunction with operational amplifiers, supply bypassing and decoupling are even more important since they can feed a considerable amount of signal back into the supply lines. For reference, bypass capacitors of at least 0.1 μF are required for a 50 mA buffer.

When emitter followers are used to drive long cables, additional precautions are required. An emitter follower by itself — which is not contained in a feedback loop — will frequently oscillate when connected to a long length of cable. When an emitter follower is connected to the output of an operational amplifier, it can produce oscillations that will persist no matter how the loop gain is compensated. An analysis of why this happens is not very enlightening, so suffice it to say that these oscillations can usually be eliminated by putting a ferrite bead[8] between the emitter follower and the cable.

Considering the loop gain of an amplifier is a valuable tool in understanding the influence of various factors on the stability of feedback amplifiers. But it is not too helpful in determining if the amplifier is indeed stable. The reason is that most problems in a well-designed system are caused by secondary effects — which occur only under certain conditions of output voltage, load current, capacitive loading, temperature, etc. Making frequency-phase plots under all these conditions would require unreasonable amounts of time, so it is invariably not done.

A better check on stability is the small-signal transient response. It can be shown mathematically that the transient response of a network has a one-for-one correspondence with the frequency domain response.[†] The advantage of transient response tests is that they are displayed instantaneously on an oscilloscope, so it is reasonable to test a circuit under a wide range of conditions.

Exact methods of analysis using transient response will not be presented here. This is not because these methods are difficult, although they are. Instead, it is because it is very easy to determine which conditions are unfavorable from the overshoot and ringing on the step response. The stability margin can be determined much more easily by how much greater the aggravating conditions can be made before the circuit oscillates than by analysis of the response under given conditions. A little practice with this technique can quickly yield much better results than classical methods even for the inexperienced engineer.

SUMMARY

A number of circuits using operational amplifiers have been proposed to show their versatility in circuit design. These have ranged from low frequency oscillators through circuits for complex analog computation. Because of the low cost of monolithic amplifiers, it is almost foolish to design dc amplifiers without integrated circuits. Moreover, the price makes it practical to take advantage of operational-amplifier performance in a variety of circuits where they are not normally used.

Many of the potential oscillation problems that can be encountered in both discrete and integrated operational amplifiers were described, and some conservative solutions to these problems were presented. The areas discussed included stray capacitance, capacitive loading and supply bypassing. Finally, a simplified method of quickly testing the stability of amplifier circuits over a wide range of operating conditions was suggested.

[†] The frequency-domain characteristics can be determined from the impulse response of a network and this is directly relatable to the step response through the convolution integral.

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Application of the LH0002 Current Amplifier

National Semiconductor
Application Note 13
September 1968

INTRODUCTION

The LH0002 Current Amplifier integrated building block provides a wide band unity gain amplifier capable of providing peak currents of up to ±200 mA into a 50 ohm load.

The circuit uses thick film technology to integrate 2 NPN and 2 PNP complementary matched silicon transistors with 4 cermet resistors on a single alumina ceramic substrate. A circuit schematic is shown in Figure 1. The negative thermal feedback provided by the close proximity of the components on a single substrate eliminates any thermal runaway problem that could occur if this circuit were constructed using discrete components.

A typical circuit features a dynamic input impedance of 200 Kohms, an output impedance of 6 ohms, DC to 50 MHz bandwidth, and an output voltage swing that approaches supply voltage. A complete list of the guaranteed and typical values for the electrical characteristics under the stated conditions is given in Table 1. These features make the LH0002 ideal for integration with an operational amplifier inside a closed loop configuration

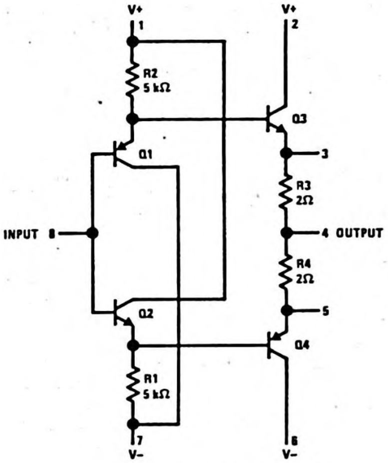


FIGURE 1. Circuit Schematic

TABLE 1. Electrical characteristics, specification applies for $T_A = 25°C$ with +12.0V on pins 1 and 2; –12.0V on pins 6 and 7.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$ $V_{IN} = 3.0\ V_{PP}$, f = 1.0 kHz $T_A = -55°C$ to 125°C	.95	.97		
Input Impedance	$R_S = 200\ k\Omega$, $V_{IN} = 1.0\ V_{rms}$, f = 1.0 kHz, $R_L = 1.0\ k\Omega$	180	200	–	kΩ
Output Impedance	$V_{IN} = 1.0\ V_{rms}$, f = 1.0 kHz $R_L = 50\Omega$, $R_S = 10\ k\Omega$	–	6	10	Ω
Output Voltage Swing	$R_L = 1.0\ k\Omega$, f = 1.0 kHz	±10	±11	–	V
DC Input Offset Voltage	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$ $T_A = -55°C$ to 125°C	–	±40	±100	mV
DC Input Offset Current	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$ $T_A = -55°C$ to 125°C	–	±6.0	±10	μA
Harmonic Distortion	$V_{IN} = 5.0\ V_{rms}$, f = 1.0 kHz	–	0.1	–	%
Bandwidth	$V_{IN} = 1.0\ V_{rms}$, $R_L = 50\Omega$, f = 1 MHz	30	50	–	MHz
Positive Supply Current	$R_S = 10\ k\Omega$, $R_L = 1\ k\Omega$	–	+6.0	+10.0	mA
Negative Supply Current	$R_S = 10\ k\Omega$, $R_L = 1\ k\Omega$	–	–6.0	–10.0	mA

to increase its current output. The symmetrical class B output portion of the circuit also provides a constant low output impedance for both the positive and negative slopes of output pulses.

CIRCUIT OPERATION

The majority of circuit applications will use symmetrical power supplies, with equal positive voltage being applied to pins 1 and 2, and equal negative voltage applied to pins 6 and 7. The reason that pin 2 and pin 6 are not connected internally to pin 1 and pin 7, respectively, is to increase the versatility of circuit operation by allowing a decreased voltage to be applied to pins 2 and 6 to minimize the power dissipation in Q3 and Q4. The larger voltage applied to the input stage also provides increased current drive as required to the output stage.

The operation of the circuit can be understood by considering that the input pin 8 is at V_{IN}. The emitter of Q1 will be approximately 0.6 volt more positive than V_{IN} at 25°C, and the converse is true for Q2. This 0.6 volt will provide a forward bias on Q3 to cancel out the Q1 base to emitter drop which in turn would provide V_{IN} at the output if all junctions, resistors, power supplies, etc., were electrically identical. The greatest error is introduced because the forward drops in the base-emitter junctions for the NPN and PNP devices are slightly different. For example, the V_{BE} of the NPN will be typically 0.6V and the V_{BE} of the PNP will be typically 0.64V under the same conditions of $I_C = 2.4$ mA at $V_{CE} = 12.0$V at 25°C. These are the approximate input stage circuit conditions for Q1 and Q2 for plus and minus 12V supplies. Fortunately, this error in both input and output offset voltage is almost always negligible when it is used inside the closed loop of a high gain operational amplifier.

A plot of input impedance vs frequency is shown in Figure 2. Inspection of this plot shows that the input impedance can be closely approximated to that of a simple first order linear network with a 45° phase lag at 0.6 MHz and a 90° phase lag at approximately one decade higher in frequency. This information is very useful for designers who have to integrate circuits which have large source impedances over a wide frequency range. The output impedance of the amplifier is very low, 6 ohms typically, and in conjunction with a voltage bandwidth of approximately 50 MHz can be considered to be insignificant for most applications for this type of device.

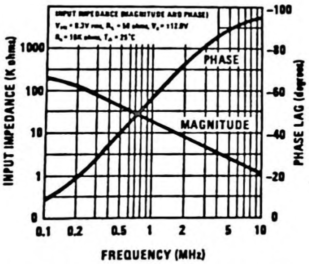


FIGURE 2. Input Impedance vs Frequency

A plot of the voltage bandwidth is shown in Figure 3. Inspection of this plot shows that phase information as well as gain information was included to assist users of this device. For example, at 10 MHz, less than an 8° phase lag would be subtracted from the phase margin of an operational amplifier when it is integrated with this device. The open loop gain of the operational amplifier would be decreased by less than 10% at 10 MHz and therefore can be considered to be insignificant for most applications.

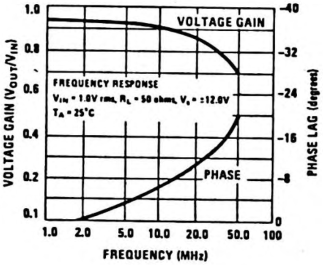


FIGURE 3. Frequency Response

APPLICATIONS

Figure 4 shows the LH0002 integrated with the LH0005 to provide differential inputs and outputs. In order for this circuit to funtion properly, a load must be floated between the outputs of the two devices to provide a complete loop of feedback. A differential head on a scope across the load presents a true waveform of the actual signal being applied to it. If only one end of the load is displayed, it will appear distorted because this information is being fed back negatively to the input in order to cancel out the loop distortion of the overall amplifier. With the compensation shown, a 20V peak to peak signal can be applied to a 100 ohm load to 80 KHz. The overall circuit is approximately 33% efficient under these conditions. A derating factor and/or heat sink must be used at higher temperatures, as shown by the LH0002 and LH0005 data sheets.

Additional output power could also be obtained by connecting another LH0002 to pin 9 of the operational amplifier. The overall load distortion under high circuit voltage gain configurations would also be reduced using two LH0002's because the LH0002 is more linear than the simple output circuits of these particular operational amplifiers.

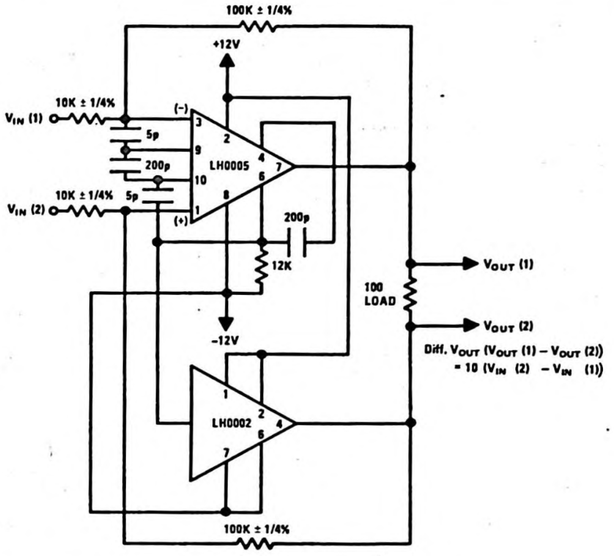

100K ± 1/4%
+12V
10K ± 1/4%
VIN (1)
(−)
3
2
5p
9
200p
LH0005
4
7
6
10
10K ± 1/4%
5p
VIN (2)
8
1
(+)
200p
12K
100
LOAD
VOUT (1)
VOUT (2)
−12V
Diff. VOUT (VOUT (1) − VOUT (2))
= 10 (VIN (2) − VIN (1))
1
LH0002
2
4
6
7
100K ± 1/4%

FIGURE 4. Differential Input-Output Operational Amplifier Integration

Figure 5 shows the LH0002 integrated with the LH101 in a booster follower configuration. The configuration is stable without the requirement for any external compensation; however, it would behoove the designer to be conservative and bypass both the negative and positive power supplies with at least a 0.01 μf capacitor to cancel out any power supply lead inductance. A 100 ohm damping resistor, located right at the input of the LH0002, might also be required between the operational amplifier and the booster amplifier. The physical layout will determine the requirement for this type of oscillation suppression. Current limiting can be added by incorporating series resistors from pins 2 and 6 to their respective power supplies. The exact value would be a function of power supply voltage and required operating temperature.

A breadboard of this configuration was assembled to empirically check the increase in offset voltage due to the addition of the LH0002. The offset voltage was measured with and without an LH0002 inside the loop with a voltage gain of 100, at −55°C, 25°C and 125°C. The additional offset voltage was less than 0.3% for all three temperature conditions even though the offset voltage of the LH0002 is much higher than that of the LH101. The high open loop gain of the LH101 divides out this source of circuit error. The integration of this device also allows higher closed loop circuit gain without excessive cross-over distortion than would be obtainable with the simple booster amplifier shown in Figure 6.

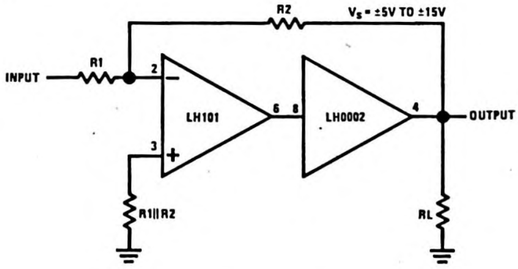

R2
VS = ±5V TO ±15V
INPUT
R1
2
−
LH101
3
+
6
8
LH0002
4
OUTPUT
R1||R2
RL

FIGURE 5. LH101-LH0002 Booster Amplifier Integration.

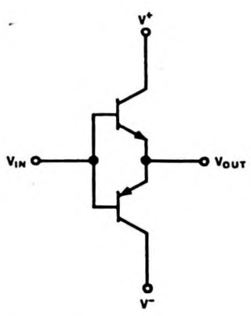


FIGURE 6. Simple Booster Amplifier

Figure 7 shows the LH0002 being used as a level shifter with a high pass filter on the input in order to reference the output to zero quiescent volts. The purpose of the 10 Kohm resistor is to provide current bias to the circuit's input transistors to reduce the output offset voltage. Figure 3, Input Impedance vs Frequency, provides a useful design aid in order to determine the value of the capacitor for the particular application. The 10 Kohm resistor, of course, has to be considered as being in parallel with the circuit's input impedance.

For a pulse input signal, the output impedance of the circuit remains low for both the positive and negative portions of the output pulse. This circuit provides both fast rise and fall times for pulse signals, even with capacitive loading. The LH0002 data sheet shows typical rise and fall times for both positive and negative pulses into a 50 ohm load.

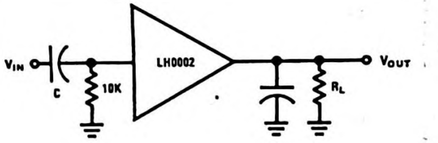


FIGURE 7. Level Shifter

Figure 8 shows the LH0002 being used to drive a pulse-transformer. The low output offset voltage allows the pulse transformer to be directly coupled to the amplifier without using a coupling capacitor to prevent saturation. The pulse transformer can be used to change the amplitude and impedance level of the pulse, the polarity of the pulses, or, with the aid of a center-tapped winding, positive and negative pulses simultaneously.

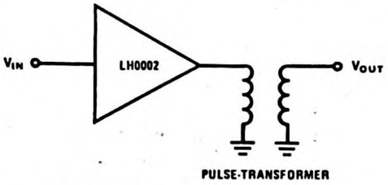


FIGURE 8. Driver for a Pulse-Transformer

The LH0002 can also be used to drive long transmission lines. Figure 9 shows a circuit configuration to match the output impedance of the amplifier to the load and coaxial cable for proper line termination to minimize reflections. A capacitor can be added to empirically adjust the time response of the waveform.

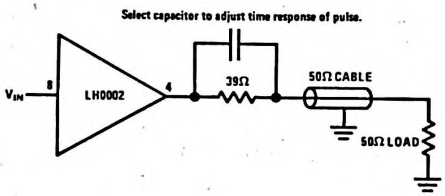


FIGURE 9. Transmission Line Driver

SUMMARY

The multitude of different applications suggested in this article shows the versatility of the LH0002. The applications specially covered were for a differential input-output operational amplifier, booster amplifier, level shifter, driver for a pulse-transformer, and transmission line driver.

An Applications Guide for Op Amps

National Semiconductor
Application Note 20
February 1969

INTRODUCTION

The general utility of the operational amplifier is derived from the fact that it is intended for use in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and loop combination. To suit it for this usage, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open-loop 3 dB point at infinite frequency rolling off at 6 dB per octave. Unfortunately, the unit cost—in quantity—would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has yielded circuits which are quite good engineering approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high quality of these amplifiers allows the implementation of equipment and systems functions impractical with discrete components. An example is the low frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase-locking.

The availability of the low-cost integrated amplifier makes it mandatory that systems and equipments engineers be familiar with operational amplifier applications. This paper will present amplifier usages ranging from the simple unity-gain buffer to relatively complex generator and wave-shaping circuits. The general theory of operational amplifiers is not within the scope of this paper and many excellent references are available in the literature.[1,2,3,4] The approach will be shaded toward the practical, amplifier parameters will be discussed as they affect circuit performance, and application restrictions will be outlined.

The applications discussed will be arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. The integrated amplifiers shown in the figures are for the most part internally compensated so frequency stabilization components are not shown; however, other amplifiers may be used to achieve greater operating speed in many circuits as will be shown in the text. Amplifier parameter definitions are contained in Appendix I.

THE INVERTING AMPLIFIER

The basic operational amplifier circuit is shown in Figure 1. This circuit gives closed-loop gain of R2/R1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R3 should be chosen to be equal to the parallel combination of R1 and R2 to minimize the offset voltage error due to bias current and that there will be an offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.

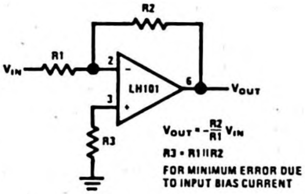

R2
R1
V_{IN}
2
3
LH101
6
V_{OUT}
R3
$V_{OUT} = -\frac{R2}{R1} V_{IN}$
R3 = R1 || R2
FOR MINIMUM ERROR DUE TO INPUT BIAS CURRENT

FIGURE 1. Inverting Amplifier

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier, however the contribution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances and offset current causes the main error for high source resistances.

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak to peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15 pF compensating capacitor, since the feedback network has an attenuation of 6 dB, while it requires 30 pF in the non-inverting unity gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 slew rate in the inverting unity gain connection will be twice that for the non-inverting connection and the inverting gain of ten connection will yield eleven times the slew rate of the non-inverting unity gain connection. The compensation trade-off for a particular connection is stability versus bandwidth, larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

The preceding discussion of offset voltage, bias current and stability is applicable to most amplifier applications and will be referenced in later sections. A more complete treatment is contained in Reference 4.

THE NON-INVERTING AMPLIFIER

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3 dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain.

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance.

Applications cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.

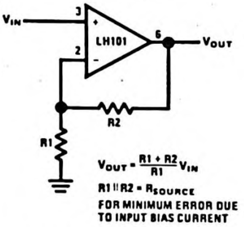


FIGURE 2. Non-Inverting Amplifier

THE UNITY-GAIN BUFFER

The unity-gain buffer is shown in Figure 3. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common mode rejection, whichever is less.

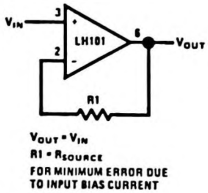
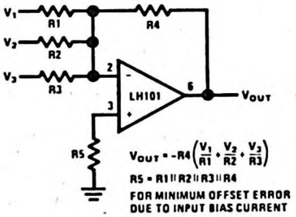


FIGURE 3. Unity Gain Buffer

Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance. Since this is the case, a low bias current amplifier such as the LH102[6] should be chosen as a unity-gain buffer when working from high source resistances. Bias current compensation techniques are discussed in Reference 5.

The cautions to be observed in applying this circuit are three: the amplifier must be compensated for unity gain operation, the output swing of the amplifier may be limited by the amplifier common mode range, and some amplifiers exhibit a latch-up mode when the amplifier common mode range is exceeded. The LH101 may be used in this circuit with none of these problems; or, for faster operation, the LM102 may be chosen.



$$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$$

$R5 = R1 \parallel R2 \parallel R3 \parallel R4$

FOR MINIMUM OFFSET ERROR DUE TO INPUT BIAS CURRENT

FIGURE 4. Summing Amplifier

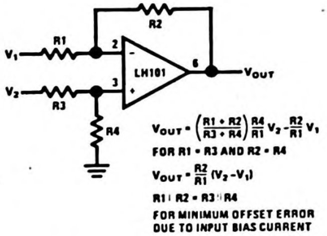
SUMMING AMPLIFIER

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 4. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor, R4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in Figure 1 by assuming the input resistor to be the parallel combination of R1, R2, and R3. Application cautions are the same as for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.

THE DIFFERENCE AMPLIFIER

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to the two inputs. This circuit is shown in Figure 5 and is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.



$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1$$

FOR $R1 = R3$ AND $R2 = R4$

$$V_{OUT} = \frac{R2}{R1}(V_2 - V_1)$$

$R1 \parallel R2 = R3 \parallel R4$

FOR MINIMUM OFFSET ERROR DUE TO INPUT BIAS CURRENT

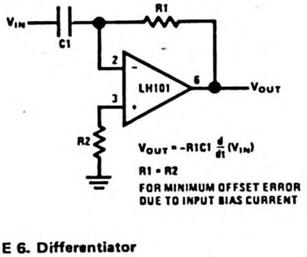
FIGURE 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal; inverting input impedance is the same as for the inverting amplifier of Figure 1 and the non-inverting input impedance is the sum of R3 and R4. Gain for either input is the ratio of R1 to R2 for the special case of a differential input single-ended output where R1 = R3 and R2 = R4. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

DIFFERENTIATOR

The differentiator is shown in Figure 6 and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R2C1, is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.



$$V_{OUT} = -R1C1\frac{d}{dt}(V_{IN})$$

$R1 = R2$

FOR MINIMUM OFFSET ERROR DUE TO INPUT BIAS CURRENT

FIGURE 6. Differentiator

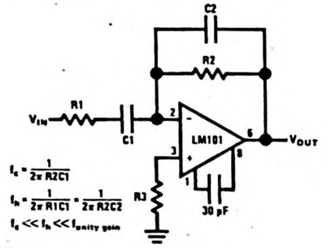

C2
R2
R1
V_IN
C1
2
3
6
8
1
LM101
V_OUT
R3
30 pF
$f_c = \frac{1}{2\pi R2C1}$
$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$
$f_c << f_h << f_{unity\ gain}$

FIGURE 7. Practical Differentiator

A practical differentiator is shown in Figure 7. Here both the stability and noise problems are corrected by addition of two additional components, R1 and C2. R2 and C2 form a 6 dB per octave high frequency roll-off in the feedback network and R1C1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave to reduce the effect of high frequency input and amplifier noise. In addition R1C1 and R2C2 form lead networks in the feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R2C1 and prevent loop instability. A gain frequency plot is shown in Figure 8 for clarity.

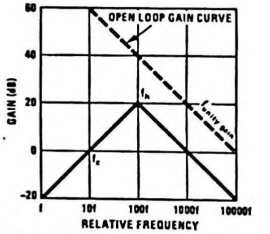


FIGURE 8. Differentiator Frequency Response

INTEGRATOR

The integrator is shown in Figure 9 and performs the mathematical operation of integration. This circuit is essentially a low-pass filter with a frequency response decreasing at 6 dB per octave. An amplitude-frequency plot is shown in Figure 10.

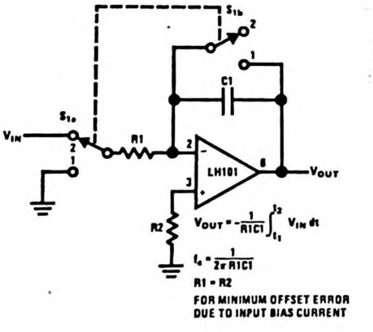

S_{1b}
2
1
C1
S_{1a}
V_IN
2
1
R1
2
3
6
LH101
V_OUT
R2
$V_{OUT} = -\frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$
$f_c = \frac{1}{2\pi R1C1}$
R1 = R2
FOR MINIMUM OFFSET ERROR
DUE TO INPUT BIAS CURRENT

FIGURE 9. Integrator

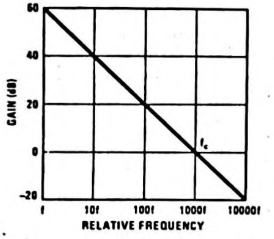


FIGURE 10. Integrator Frequency Response

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as S_1. When S_1 is in position 1, the amplifier is connected in unity-gain and capacitor C1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant times the time integral of the input voltage.

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R2 must equal R1 for minimum error due to bias current.

SIMPLE LOW-PASS FILTER

The simple low-pass filter is shown in Figure 11. This circuit has a 6 dB per octave roll-off after a closed-loop 3 dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R3 to R1. The circuit may be considered as an AC integrator at frequencies well above f_c; however, the time domain response is that of a single RC rather than an integral.

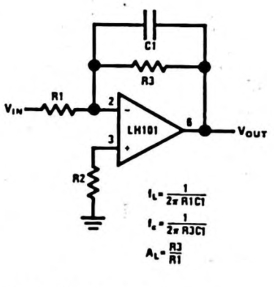

C1
R3
R1
V_IN
2
3
6
LH101
V_OUT
R2
$f_L = \frac{1}{2\pi R1C1}$
$f_c = \frac{1}{2\pi R3C1}$
$A_L = \frac{R3}{R1}$

FIGURE 11. Simple Low Pass Filter

R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The amplifier should be compensated for unity-gain or an internally compensated amplifier can be used.

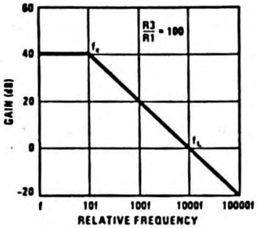


FIGURE 12. Low Pass Filter Response

A gain frequency plot of circuit response is shown in Figure 12 to illustrate the difference between this circuit and the true integrator.

THE CURRENT-TO-VOLTAGE CONVERTER

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage with a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current-to-voltage transducer is shown in Figure 13. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R1. The scale factor of this circuit is R1 volts per amp. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.

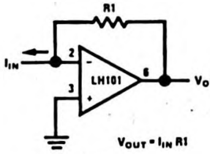


FIGURE 13. Current to Voltage Converter

This basic circuit is useful for many applications other than current measurement. It is shown as a photocell amplifier in the following section.

The only design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation. Valuable techniques for bias current compensation are contained in Reference 5.

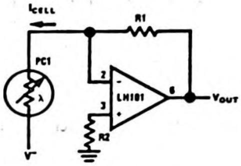


FIGURE 14. Amplifier for Photoconductive Cell

PHOTOCELL AMPLIFIERS

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in Figures 14, 15, and 16 respectively.

All photogenerators display some voltage dependence of both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

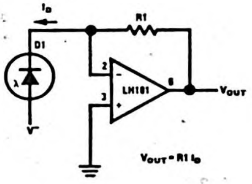


FIGURE 15. Photodiode Amplifier

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.

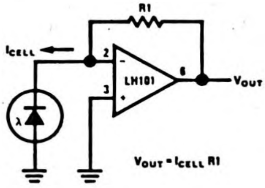


FIGURE 16. Photovoltaic Cell Amplifier

The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R2 is elective: in the case of photovoltaic cells or of photodiodes, it is not required in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

PRECISION CURRENT SOURCE

The precision current source is shown in Figures 17 and 18. The configurations shown will sink or source conventional current respectively.

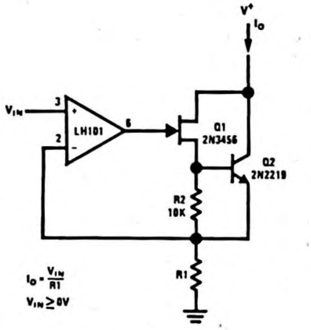


FIGURE 17. Precision Current Sink

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 volt more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and they are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I_{bias}.

The source and sink illustrated in Figures 17 and 18 use an FET to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET-bipolar combination in cases where the output current is high and the base current of the Darlington input would not cause a significant error.

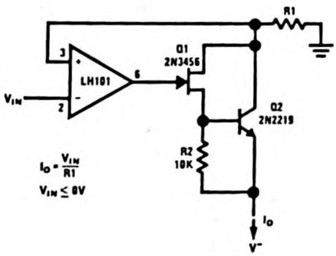


FIGURE 18. Precision Current Source

The amplifiers used must be compensated for unity-gain and additional compensation may be required depending on load reactance and external transistor parameters.

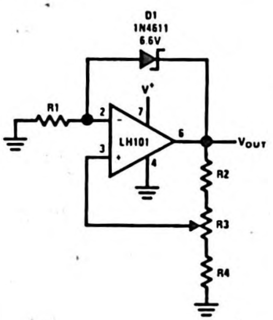


FIGURE 19a. Positive Voltage Reference

ADJUSTABLE VOLTAGE REFERENCES

Adjustable voltage reference circuits are shown in Figures 19 and 20. The two circuits shown have different areas of applicability. The basic difference between the two is that Figure 19 illustrates a voltage source which provides a voltage greater than the reference diode while Figure 20 illustrates a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

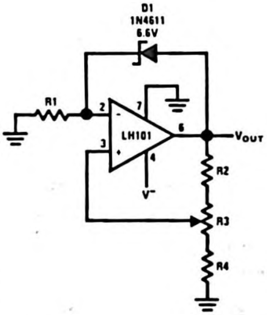


FIGURE 19b. Negative Voltage Reference

High precision extended temperature applications of the circuit of Figure 19 require that the range of adjustment of V_{OUT} be restricted. When this is done, R1 may be chosen to provide optimum zener current for minimum zener T.C. Since I_Z is not a function of V^+, reference T.C. will be independent of V^+

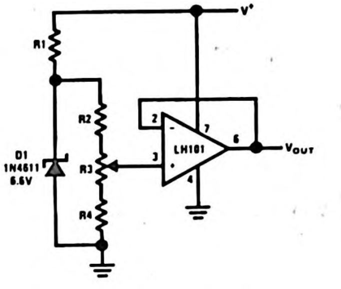


FIGURE 20a. Positive Voltage Reference

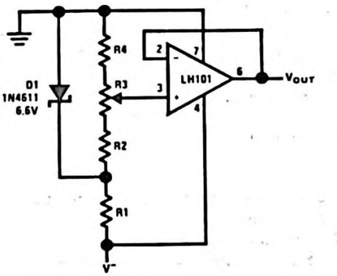


FIGURE 20b. Negative Voltage Reference

The circuit of Figure 20 is suited for high precision extended temperature service if V^+ is reasonably constant since I_Z is dependent on V^+. R1, R2, R3, and R4 are chosen to provide the proper I_Z for minimum T.C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity-gain operation or, if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier input.

The circuits shown employ a single power supply, this requires that common mode range be considered in choosing an amplifier for these applications. If the common mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 may be used with a single power supply since the common mode range is from V^+ to within approximately 2 volts of V^-.

THE RESET STABILIZED AMPLIFIER

The reset stabilized amplifier is a form of chopper-stabilized amplifier and is shown in Figure 21. As shown, the amplifier is operated closed-loop with a gain of one.

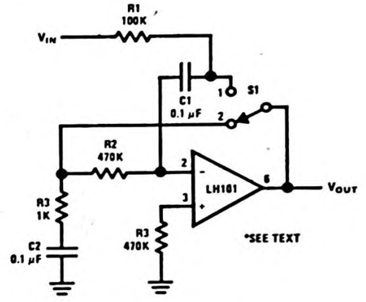


FIGURE 21. Reset Stabilized Amplifier

The connection is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R2 due to input bias current. The voltage at the inverting input will be equal to input offset voltage. Capacitor C1 will charge to the sum of input offset voltage and V_{IN} through R1. When C1 is charged, no current flows through the source resistance and R1 so there is no error due to input resistance. S_1 is then changed to position 1. The voltage stored on C1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from $(V_{OS} + I_{bias}R2)$ to $V_{IN} + I_{bias}R2)$ as S_1 is changed from position 2 to position 1. Amplifier bias current is supplied through R2 from the output of the amplifier or from C2 when S_1 is in position 2 and position 1 respectively. R3 serves to reduce the offset at the amplifier output if the amplifier must have maximum linear range or if it is desired to DC couple the amplifier.

An additional advantage of this connection is that input resistance approaches infinity as the capacitor C1 approaches full charge, eliminating errors due to loading of the source resistance. The time spent in position 2 should be long with respect to the changing time of C1 for maximum accuracy.

The amplifier used must be compensated for unity gain operation and it may be necessary to overcompensate because of the phase shift across R2 due to C1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and overcompensation does not reduce accuracy.

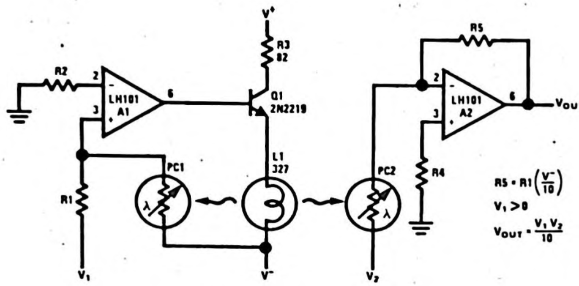


FIGURE 22. Analog Multiplier

THE ANALOG MULTIPLIER

A simple embodiment of the analog multiplier is shown in Figure 22. This circuit circumvents many of the problems associated with the log-antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1, When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminated PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen equal to the product of R1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in-rush current when first turning on the lamp, L1.

THE FULL-WAVE RECTIFIER AND AVERAGING FILTER

The circuit shown in Figure 23 is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full-wave rectifier, and deletion of C1 provides an absolute value generator.

Circuit operation may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a simple unity-gain inverter with input resistor, R1, and feedback resistor, R2, giving a positive going output.

For positive inputs, A1 operates as a normal amplifier connected to the A2 summing point through resistor, R5. Amplifier A1 then acts as a simple unity-gain inverter with input resistor, R3, and

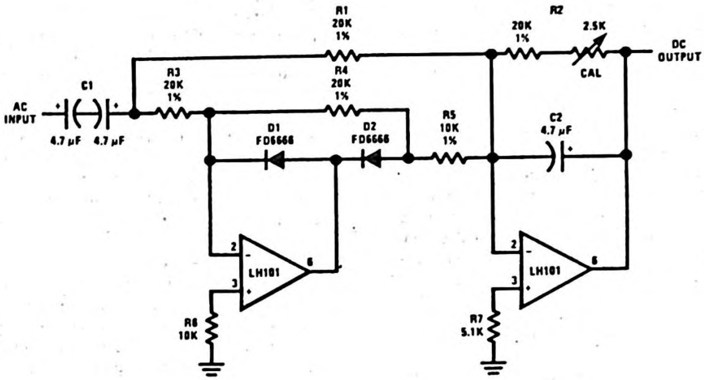


FIGURE 23. Full-Wave Rectifier and Averaging Filter

feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one-half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

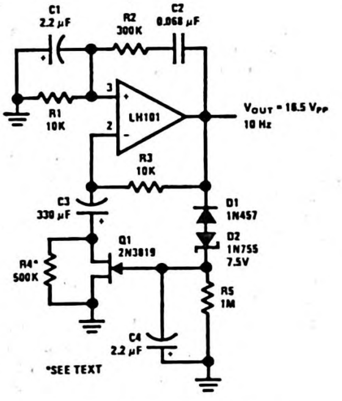
The amplifiers chosen must be compensated for unity-gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

SINE WAVE OSCILLATOR

An amplitude-stabilized sine-wave oscillator is shown in Figure 24. This circuit provides high purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten filament lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

The Wein Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wein Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency. To stabilize the frequency of oscillation, and to reduce harmonic distortion.



*SEE TEXT

FIGURE 24. Wein Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and D2 to conduct, charging C4. The charge stored in C4 provides bias to Q1, which determines amplifier gain. C3 is a low frequency roll-off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by amplifier open-loop gain and by the response time of the negative feedback loop filter, R5 and C4. A trade-off is necessary in determining amplitude stabilization time constant and oscillator distortion. R4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general-purpose oscillator.

TRIANGLE-WAVE GENERATOR

A constant amplitude triangular-wave generator is shown in Figure 25. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency.

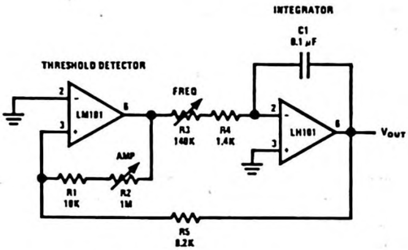


FIGURE 25. Triangular-Wave Generator

The generator embodies an integrator as a ramp generator and a threshold detector with hysterisis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a SchmittTrigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feed-back loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R3 and R4 causing a current I^+ to flow. The integrator then generates a negative-going ramp with a rate of $I^+/C1$ volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of $I^-/C1$ volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

Triangular-wave frequency is determined by R3, R4 and C1 and the positive and negative saturation voltages of the amplifier A1. Amplitude is determined by the ratio of R5 to the combination of R1 and R2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in Figure 26.

The integrator should be compensated for unity-gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

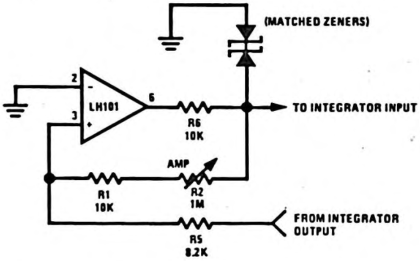
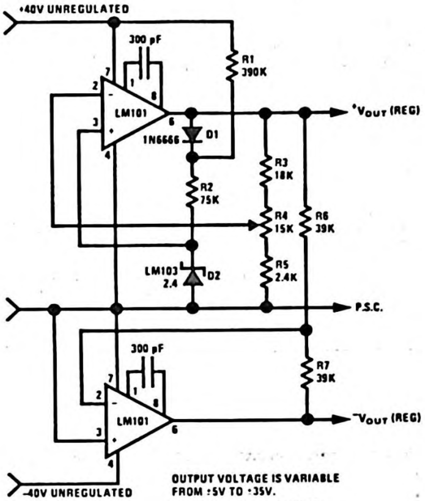


FIGURE 26. Threshold Detector with Regulated Output

TRACKING REGULATED POWER SUPPLY

A tracking regulated power supply is shown in Figure 27. This supply is very suitable for powering an operational amplifier system since positive and negative voltages track, eliminating common mode signals originating in the supply voltage. In addition, only one voltage reference and a minimum number of passive components are required.


+40V UNREGULATED
300 pF
R1
390K
LM101
+VOUT (REG)
1N6666
D1
R3
18K
R2
75K
R4
15K
R6
39K
LM103
2.4
D2
R5
2.4K
P.S.C.
300 pF
R7
39K
LM101
-VOUT (REG)
-40V UNREGULATED

OUTPUT VOLTAGE IS VARIABLE FROM ±5V TO ±35V.

NEGATIVE OUTPUT TRACKS POSITIVE OUTPUT TO WITHIN THE RATIO OF R6 TO R7.

FIGURE 27. Tracking Power Supply

Power supply operation may be understood by considering first the positive regulator. The positive regulator compares the voltage at the wiper of R4 to the voltage reference, D2. The difference between these two voltages is the input voltage for the amplifier and since R3, R4, and R5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R1 and diode D1 provide this start-up current. D1 decouples the reference string from the amplifier output during start-up and R1 supplies the start-up current from the unregulated positive supply. After start-up, the low amplifier output impedance reduces reference current variations due to the current through R1.

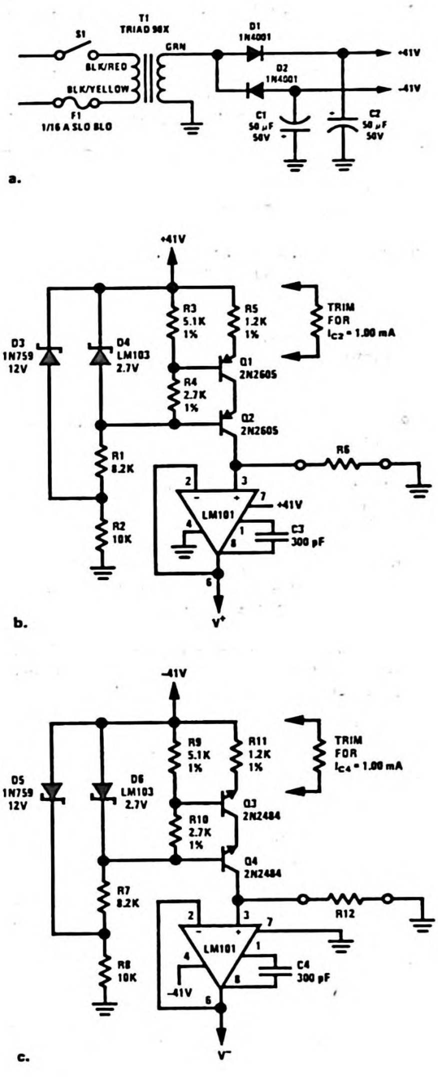
The negative regulator is simply a unity-gain inverter with input resistor, R6, and feedback resistor, R7.

The amplifiers must be compensated for unity-gain operation.

The power supply may be modulated by injecting current into the wiper of R4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

PROGRAMMABLE BENCH POWER SUPPLY

The complete power supply shown in Figure 28 is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.


S1
T1
TRIAD 90X
BLK/RED
BLK/YELLOW
GRN
F1
1/16 A SLO BLO
D1
1N4001
+41V
D2
1N4001
-41V
C1
50 μF
50V
C2
50 μF
50V
+41V
R3
5.1K
1%
R5
1.2K
1%
TRIM
FOR
IC2 = 1.00 mA
D3
1N759
12V
D4
LM103
2.7V
Q1
2N2605
R4
2.7K
1%
Q2
2N2605
R1
8.2K
R6
LM101
+41V
C3
300 pF
R2
10K
V+
-41V
R9
5.1K
1%
R11
1.2K
1%
TRIM
FOR
IC4 = 1.00 mA
D5
1N759
12V
D6
LM103
2.7V
Q3
2N2484
R10
2.7K
1%
Q4
2N2484
R7
8.2K
R12
LM101
C4
300 pF
R8
10K
-41V
V-

a.

b.

c.

FIGURE 28. Low-Power Supply for Integrated Circuit Testing

Programming sensitivity of the positive and negative supply is 1V/1000Ω of resistors R6 and R12 respectively. The output voltage of the positive regulator may be varied from approximately +2V to +38V with respect to ground and the negative regulator output voltage may be varied from −38V to 0V with respect to ground. Since LH101 amplifiers are used, the supplies are inherently short circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1.0 μF range.

CONCLUSIONS

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The cautions noted in each section will show the more common pitfalls encountered in amplifier usage.

APPENDIX I

DEFINITION OF TERMS

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Common Mode Rejection Ratio: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other gounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

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Designs for Negative Voltage Regulators

National Semiconductor
Application Note 21
December 1968

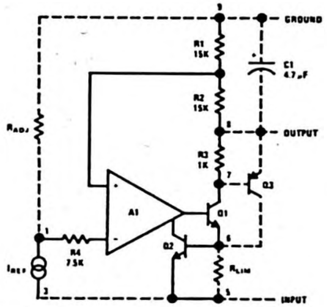
AN-21 Designs for Negative Voltage Regulators

INTRODUCTION

A number of IC voltage regulators have been introduced to date, but these have been designed primarily to regulate positive voltages. Most can be adapted as negative regulators, at some sacrifice in complexity, performance and flexibility. This note, however, describes an IC, which is designed specifically as a negative regulator. It is intended to complement the LM100 and LM105 positive regulators, providing a line of IC's for practically every regulator application.

Unique features of the circuit are that it supplies any output voltage from 0V down to −40V, while operating from a single unregulated supply. The output voltage is proportional to a single programming resistor, and remote sensing can be done at the load. It also regulates within 0.01% in circuits using a separate, floating bias supply, where the maximum output voltage is limited only by the breakdown of external pass transistors. The device is designed for either linear or switching regulator applications.

In the circuits described, emphasis is placed on practical considerations for the design of reliable regulators. Many of the pitfalls which cause unexpected failures are explained, and protection schemes for many of the hazards facing regulators are given. Most of the design hints are sufficiently general to apply equally to other IC's or even regulators designed entirely with discrete components.



A functional diagram of the LM104 regulator and external circuitry (dash line) is shown in the figure. The internal reference is a temperature compensated current source, I_{ref}. A voltage which is proportional to an external programming resistor, R_{adj}, is fed into an error amplifier, A1. This drives an internal series pass transistor, Q1, to supply an output voltage equal to twice the voltage across the programming resistor. External pass transistors can be added, as is Q3, to increase the output-current capability. Short-circuit protection makes the circuit exhibit a constant-current characteristic when Q2 is turned on by the voltage drop across an external current-limit resistor, R_{lim}. A more complete description of the integrated circuit itself is given in the back of the text.

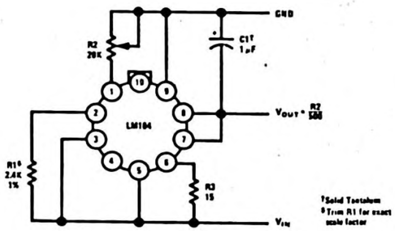
LOW POWER REGULATOR OR BIAS SUPPLY

This circuit can provide output voltages between 0V and −40V at currents up to 25 mA. The output voltage is linearly dependent on the value of R2, giving approximately 2V for each 1 KΩ of resistance. The exact scale factor can be set up by trimming R1. This should be done at the maximum output voltage setting in order to compensate for any mismatch in the internal divider resistors of the integrated circuit.

Short-circuit protection is provided by R3. The value of this resistor should be chosen so that the voltage drop across it is 300 mV at the maximum load current. This insures worst-case operation up to full load over a −55°C to 125°C temperature range. With a lower maximum operating temperature, the design value for this voltage can be increased linearly to 525 mV at 25°C.

For an output voltage setting of 15V, the regulation, no load to full load, is better than 0.05%; and the line regulation is better than 0.2% for a ±20% input voltage variation. Noise and ripple can be greatly reduced by bypassing R2 with a 10 μF capacitor. This will keep the ripple on the output less than 0.5 mV for a 1V, 120 Hz ripple on the unregulated input. The capacitor also improves the line-transient response by a factor of five.

An output capacitor of at least 1 μF is required to keep the regulator from oscillating. This should be a low inductance capacitor, preferably solid tantalum, installed with short leads. It is not usually necessary to bypass the input, but at least a 0.01 μF bypass is advisable when there are long leads connecting the circuit to the unregulated power source.

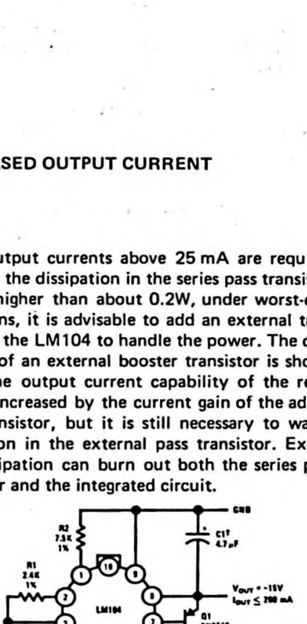


†Solid Tantalum
‡Trim R1 for exact scale factor

It is important to watch power dissipation in the integrated circuit even with load currents of 25 mA or less. The dissipation can be in excess of 1W with large input-output voltage differentials, and this is above ratings for the device.

INCREASED OUTPUT CURRENT

When output currents above 25 mA are required or when the dissipation in the series pass transistor can be higher than about 0.2W, under worst-case conditions, it is advisable to add an external transistor to the LM104 to handle the power. The connection of an external booster transistor is shown here. The output current capability of the regulator is increased by the current gain of the added PNP transistor, but it is still necessary to watch dissipation in the external pass transistor. Excessive dissipation can burn out both the series pass transistor and the integrated circuit.



For example, with the circuit shown, the worst-case input voltage can be 25V. With a shorted output at 125°C, the current through the pass transistor will be 300 mA; and the dissipation in it will be 7.5W. This clearly establishes the need for an efficient heat sink.

For lower-power operation, a 2N2905 with a clip on heat sink can be used for the external pass transistor. However, when the worst case dissipation is above 0.5W, it is advisable to employ a power device such as the 2N3740 with a good heat sink.

The current limit resistor is chosen so that the voltage drop across it is 300 mV, with maximum load current, for operation to 125°C. With lower maximum ambients this voltage drop could be increased by 2.2 mV/°C. If possible, a fast-acting fuse rated about 25% higher than the maximum load current should be included in series with the unregulated input.

When a booster transistor is used, the minimum input-output voltage differential of the regulator will be increased by the emitter-base voltage of the added transistor. This establishes the minimum differential at 2 to 3V, depending on the base drive required by the external transistor.

HIGH CURRENT REGULATOR

When output currents in the ampere range are needed, it is necessary to add a second booster transistor to the LM104 circuitry. This connection is shown in the accompanying figure. The output current capability of the LM104 is increased by the product of the current gains of Q1 and Q2. However, it is still necessary to watch the dissipation in both the series pass transistor, Q2, and its driver, Q1. A clip-on heat sink is definitely required for Q1, and it is advisable to replace the 2N2905 with a 2N3740 which has a good heat sink when output currents greater than 1A are needed. A 1000 pF capacitor should also be added between Pins 4 and 5 to compensate for the poorer frequency response of the 2N3740. The need for an efficient heat sink on Q2 should be obvious.

Experience shows that a single-diffused transistor such as a 2N3055 (or a 2N3772 for higher currents) is preferred over a double diffused, high-frequency transistor for the series pass element. The slower, single-diffused devices are less prone to secondary breakdown and oscillations in linear regulator applications.

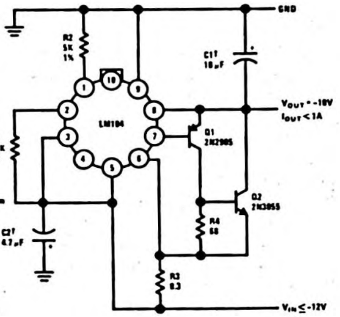
As with the lower-current regulators, C1 is required to frequency compensate the regulator and prevent oscillations. It is also advisable to bypass the input with C2 if the regulator is located any distance from the output filter of the unregulated supply. The resistor across the emitter base junction of Q2 fixes the minimum collector current of Q1 to minimize oscillation problems with light loads. It is still possible to experience oscillations with certain physical layouts, but these can almost always be eliminated by stringing a ferrite bead, such as a Ferroxcube K5-001-00/3B, on the emitter lead of Q2.

The use of two booster transistors does not appreciably increase the minimum input-output voltage differential over that for a single transistor. The minimum differential will be 2 to 3V, depending on the drive current required from the integrated circuit.

With high current regulators, remote sensing is sometimes required to eliminate the effect of line resistance between the regulator and the load. This can be accomplished by returning R2 and Pin 9 of the LM104 to the ground end of the load and connecting Pin 8 directly to the high end of the load.

The low resistance values required for the current limit resistor, R3, are sometimes not readily available. A suitable resistor can be made using a piece of resistance wire or even a short length of kovar lead wire from a standard TO-5 transistor.

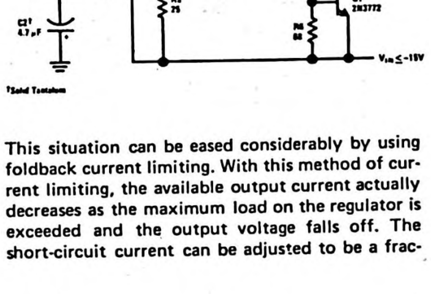
The current limit sense voltage can be reduced to about 400 mV by inserting a germanium diode (or a diode-connected germanium transistor) in series with Pin 6 of the LM104. This diode will also compensate the sense voltage and make the short circuit current essentially independent of temperature.



With high current regulators it is especially important to use a low-inductance capacitor on the output. The lead length on this capacitor must also be made short. Otherwise, the capacitor leads can resonate with smaller bypass capacitors (like 0.1 µF ceramic) which may be connected to the output. These resonances can lead to oscillations. With short leads on the output capacitor, the Q of the tuned circuit can be made low enough so that it cannot cause trouble.

FOLDBACK CURRENT LIMITING

High current regulators dissipate a considerable amount of power in the series pass transistor under full-load conditions. When the output is shorted, this dissipation can easily increase by a factor of four. Hence, with normal current limiting, the heat sink must be designed to handle much more power than the worst case full load dissipation if the circuit is to survive short-circuit conditions. This can increase the bulk of the regulator substantially.



†Solid Tantalum

This situation can be eased considerably by using foldback current limiting. With this method of current limiting, the available output current actually decreases as the maximum load on the regulator is exceeded and the output voltage falls off. The short-circuit current can be adjusted to be a fraction of the full load current, minimizing dissipation in the pass transistor.

The circuit shown here accomplishes just this. Normally Q3 is held in a non-conducting state by the voltage developed across R4. However, when the voltage across the current limit resistor, R7, increases to where it equals the voltage across R4 (about 1V), Q3 turns on and begins to rob base drive from the driver transistor, Q1. This causes an increase in the output current of the LM104, and it will go into current limiting at a current determined by R5. Since the base drive to Q1 is clamped, the output voltage will drop with heavier loads. This reduces the voltage drop across R4 and, therefore, the available output current. With the output completely shorted, the current will be about one-fifth the full-load current.

In design, R7 is chosen so that the voltage drop across it will be 1 to 2V under full load conditions. The resistance of R3 should be one-thousand times the output voltage. R4 is then determined from

$$R_4 \cong \frac{R_7\ R_3\ I_{FL}}{V_{OUT} + 0.5}$$

where I_{FL} is the load current at which limiting will occur.

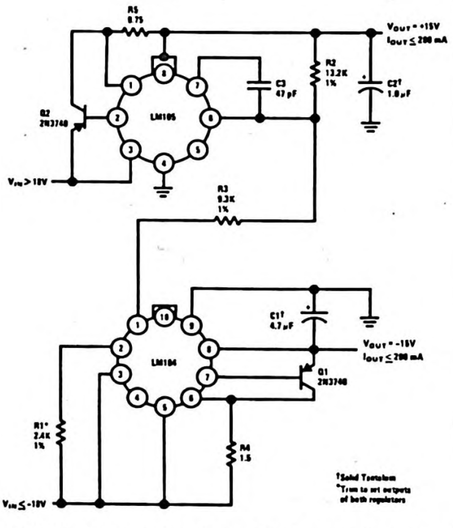
If it is desired to reduce the ratio of full load to short circuit current, this can be done by connecting a resistance of 2 to 10 KΩ across the emitter-base of Q3.

SYMMETRICAL POWER SUPPLIES

In many applications, such as powering operational amplifiers, there is a need for symmetrical positive and negative supply voltages. A circuit which is a particularly-economical solution to this design problem is shown in the adjoining figure. It uses a minimum number of components, and the voltage at both outputs can be set up within ±1.5% by a single adjustment. Further, the output voltages will tend to track with temperature and variations on the unregulated supply.

The positive voltage is regulated by an LM105, while an LM104 regulates the negative supply. The unusual feature is that the two regulators are interconnected by R3. This not only eliminates one precision resistor, but the reference current of the LM104 stabilizes the LM105 so that a ±10% variation in its reference voltage is only seen as a ±3% change in output voltage. This means that in many cases the output voltage of both regulators can be set up with sufficient accuracy by trimming a single resistor, R1.

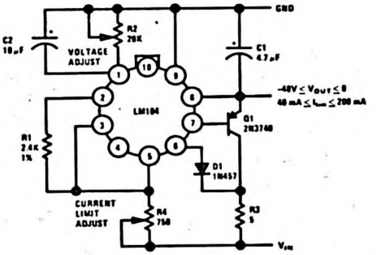
The line regulation and temperature drift of the circuit is determined primarily by the LM104, so both output voltages will tend to track. Output ripple can be reduced by about a factor of five to less than 2 mV/V by bypassing Pin 1 of the LM104 to ground with a 10 μF capacitor. A center-tapped transformer with a bridge rectifier can be used for the unregulated power source.


R5
0.75
Q2
2N3740
LM105
1
2
3
4
5
6
7
8
C3
47 pF
R2
13.2K
1%
C2†
1.0 μF
$V_{OUT} = +15V$
$I_{OUT} \leq 200$ mA
$V_{IN} > 18V$
R3
9.3K
1%
LM104
1
2
3
4
5
6
7
8
9
10
C1†
4.7 μF
$V_{OUT} = -15V$
$I_{OUT} \leq 200$ mA
Q1
2N3740
R1*
2.4K
1%
R4
1.5
$V_{IN} \leq -18V$

†Solid Tantalum
*Trim to set outputs of both regulators

ADJUSTABLE CURRENT LIMITING

In laboratory power supplies, it is often necessary to adjust the limiting current of a regulator. This, of course, can be done by using a variable resistance for the current limit resistor. However, the current-limit resistor can easily have a value below that of commercially-available potentiometers. Discrete resistance values can be switched to vary the limiting current, but this does not provide continuously-variable adjustment.



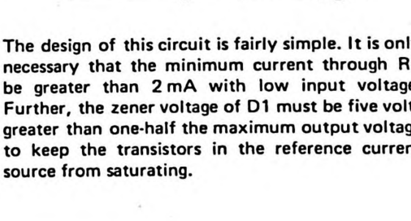
The circuit shown here solves this problem, giving a linear adjustment of limiting current over a five-to-one range. A silicon diode, D1, is included to reduce the current limit sense voltage to approximately 50 mV. Approximately 1.3 mA from the reference supply is passed through a potentiometer, R4, to buck out the diode voltage. Therefore, the effective current limit sense voltage is nearly proportional to the resistance of R4. The current through R4 is fairly insensitive to changes in ambient temperature, and D1 compensates for temperature variations in the current limit sense voltage of the LM104. Therefore, the limiting current will not be greatly affected by temperature.

It is important that a potentiometer be used for R4 and connected as shown. If a rheostat connection were used, it could open while it was being adjusted and momentarily increase the current limit sense voltage to many times its normal value. This could destroy the series pass transistors under short-circuit conditions.

The inclusion of R4 will soften the current limiting characteristics of the LM104 somewhat because it acts as an emitter-degeneration resistor for the current-limit transistor. This can be avoided by reducing the value of R4 and developing the voltage across R4 with additional bleed current to ground.

IMPROVING LINE REGULATION

The line regulation for voltage variations on the reference supply terminal of the LM104 is about five times worse than it is for changes on the unregulated input. Therefore, a zener-diode preregulator can be used on the reference supply to improve line regulation. This is shown in the figure.



†Solid Tantalum

The design of this circuit is fairly simple. It is only necessary that the minimum current through R4 be greater than 2 mA with low input voltage. Further, the zener voltage of D1 must be five volts greater than one-half the maximum output voltage to keep the transistors in the reference current source from saturating.

USING PROTECTIVE DIODES

It is a little known fact that most voltage regulators can be damaged by shorting out the unregulated input voltage while the circuit is operating—even though the output may have short-circuit protection. When the input voltage to the regulator falls instantaneously to zero, the output capacitor is still charged to the nominal output voltage. This applies voltage of the wrong polarity across the series pass transistor and other parts of the regulator, and they try to discharge the output capacitor into the short. The resulting current surge can damage or destroy these parts.

When the LM104 is used as the control element of the regulator, the discharge path is through internal junctions forward biased by the voltage reversal. If the charge on the output capacitor is in the order of 40 volt • µF, the circuit can be damaged during the discharge interval. However, the problem is not only seen with integrated circuit regulators. It also happens with discrete regulators where the series-pass transistor usually gets blown out.

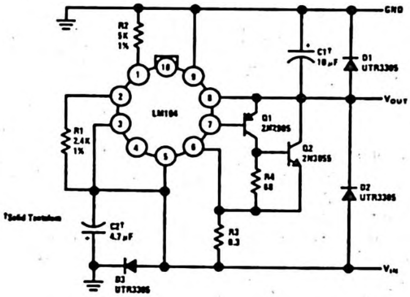
The problem can be eliminated by connecting a diode between the output and the input such that it discharges the output capacitor when the input is shorted. The diode should be capable of handling large current surges without excessive voltage drop, but it does not have to be a power diode since it does not carry current continuously. It should also be relatively fast. Ordinary rectifier diodes will not do because they look like an open circuit in the forward direction until minority carriers are injected into the intrinsic base region of the PIN structure.

This problem is not just caused by accidental physical shorts on the input. It has shown up more than once when regulators are driven from high-frequency dc-dc converters. Tantalum capacitors are frequently used as output filters for the rectifiers. When these capacitors are operated near their maximum voltage ratings with excessive high frequency ripple across them, they have a tendency to sputter—that is, short momentarily and clear themselves. When they short, they can blow out the regulator; but they look innocent after the smoke has cleared.

The solution to this problem is to use capacitors with conservative voltage ratings, to observe the maximum ripple ratings for the capacitor and to include a protective diode between the input and output of the regulator to protect it in case sputtering does occur.

Heavy loads operating from the unregulated supply can also destroy a voltage regulator. When the input power is switched off, the input voltage can drop faster than the output voltage, causing a voltage reversal across the regulator, especially when the output of the regulator is lightly loaded. Inductive loads such as a solenoid are particularly troublesome in this respect. In addition to causing a voltage reversal between the input and the output, they can reverse the input voltage causing additional damage.

In cases like this, it is advisable to use a multiple-pole switch or relay to disconnect the regulator from the unregulated supply separate from the other loads. If this cannot be done, it is necessary to put a diode across the input of the regulator to clamp any reverse voltages, in addition to the protective diode between the input and the output.

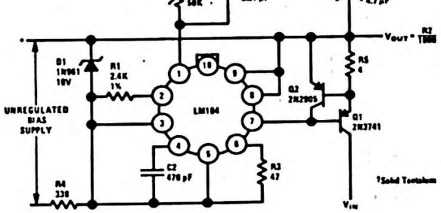


Yet another failure mode can occur if the regulated supply drives inductive loads. When power is shut off, the inductive current can reverse the output voltage polarity, damaging the regulator and the output capacitor. This can be cured with a clamp diode on the output. Even without inductive loads it is usually good practice to include this clamp diode to protect the regulator if its output is accidentally shorted to a negative supply.

A regulator with all these protective diodes is shown here. D1 protects against output voltage reversal. D2 prevents a voltage reversal between the input and the output of the regulator. And D3 prevents a reversal of the input-voltage polarity. In many cases, D3 is not needed if D1 and D2 are used, since these diodes will clamp the input voltage within two diode drops of ground. This is adequate if the input voltage reversals are of short duration.

HIGH VOLTAGE REGULATOR

In the design of commercial power supplies, it is common practice to use a floating bias supply to power the control circuitry of the regulator. As shown here, this connection can be used with the LM104 to regulate output voltages that are higher than the ratings of the integrated circuit. Better regulation can also be obtained because it is a simple matter to preregulate the low current bias supply so that the integrated circuit does not see ripple or line voltage variations and because the reduced operating voltage minimizes power dissipation and associated thermal effects from the current delivered to the booster transistor.



†Solid Tantalum

The bias for the LM104, which is normally obtained from a separate winding on the main power transformer, is preregulated by D1. R4 is selected so that it can provide the 3 mA operating current for the integrated circuit as well as the base drive of the booster transistor, Q1, with full load and minimum line voltage. The booster transistor regulates the voltage from the main supply, and its breakdown voltage will determine the maximum operating voltage of the complete regulator.

The connection of the LM104 is somewhat different than usual: the internal divider for the error amplifier is shorted out by connecting Pins 8 and 9 together. This makes the output voltage equal to the voltage drop across the adjustment resistor, R2, instead of twice this voltage as is normally the case. C2 and C3 must also be added to prevent oscillation. The value of C3 can be increased to 4.7 μF to reduce noise on the output.

It is necessary to add Q2 and R5 to provide current limiting. When the output current becomes high enough to turn on Q2, there will be an abrupt rise in the output current of the LM104 as Q2 tries to remove base drive from the booster transistor. Any further increases in load current will cause the LM104 to limit at a current determined by R3, and the output voltage will collapse. The value of R3 must be selected so that the integrated circuit can deliver the base current of Q1, at full load, without limiting.

A second, NPN booster transistor can be used in a compound connection with Q1 to increase the output current of the regulator. However, with very-high-voltage regulators, the most economical solution may be to use a high voltage PNP driving a vacuum tube for the series pass element.

Remote sensing, which eliminates the effects of voltage dropped in the leads connecting the regulator to the load, can be provided by connecting R2 to the ground end of the load and Pins 8 and 9 to the high end of the load.

SWITCHING REGULATOR

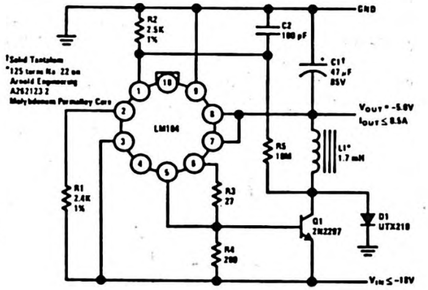
Linear regulators have the advantages of fast response to load transients as well as low noise and ripple. However, since they must dissipate the difference between the unregulated-supply power and the output power, they sometimes have a low efficiency. This is not always a problem with ac line-operated equipment because the power loss is easily afforded, because the input voltage is already fairly-well regulated and because losses can be minimized by adjustment of transformer ratios in the power supply. In systems operating from a fixed dc input voltage, the situation is often much different. It might be necessary to regulate a 28V input voltage down to 5V. In this case, the power loss can quickly become excessive. This is true even if efficiency is not one of the more important criteria, since high power dissipation calls for expensive power transistors and elaborate heat sinking methods.

Switching regulators can be used to greatly reduce dissipation. Efficiencies approaching 90% can be realized even though the regulated output voltage is only a fraction of the input voltage. With proper design, transient response and ripple can also be made quite acceptable.

This circuit, which uses the LM104 as a self-oscillating switching regulator, operates in much the same way as a linear regulator. The reference current is set up at 1 mA with R1, and R2 determines the output voltage in the normal fashion. The circuit is made to oscillate by applying positive feedback through R5 to the non-inverting input on the error amplifier of the LM104. When the output voltage is low, the internal pass transistor of the integrated circuit turns on and drives Q1 into saturation. The current feedback through R5 then increases the magnitude of the reference voltage developed across R2. Q1 will remain on until the output voltage comes up to twice this reference voltage. At this point, the error amplifier goes into linear operation, and the positive feedback makes the circuit switch off. When this happens, the reference voltage is lowered by feedback through R5, and the circuit will stay off until the output voltage drops to where the error amplifier again goes into linear operation. Hence, the circuit regulates with the output voltage oscillating about the nominal value with a peak-to-peak ripple of around 40 mV.

The power conversion from the input voltage to a lower output voltage is obtained by the action of the switch transistor, Q1, the catch diode, D1, and the LC filter. The inductor is made large enough so that the current through it is essentially constant throughout the switching cycle. When Q1 turns on, the voltage on its collector will be nearly equal to the unregulated input voltage. When it turns off, the magnetic field in L1 begins to collapse, driving the collector voltage of Q1 to ground where it is clamped by D1.

If, for example, the input voltage is 10V and the switch transistor is driven at a 50% duty cycle, the average voltage on the collector of Q1 will be 5V. This waveform will be filtered by L1 and C1 and appear as a 5V dc voltage on the output. Since the inductor current comes from the input while Q1 is on but from ground through D1 while Q1 is off, the average value of the input current will be half the output current. The power output will therefore equal the input power if switching losses are neglected.



†Solid Tantalum

*125 turns No. 22 on Arnold Engineering A262123-2 Molybdenum Permalloy Core

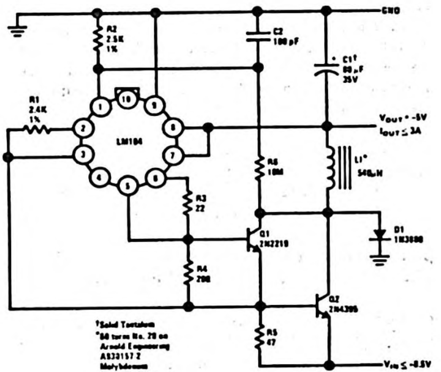
In design, the value of R3 is chosen to provide sufficient base drive to Q1 at the maximum load current. R4 must be low enough so that the bias current coming out of Pin 5 of the LM104 (approximately 300 µA) does not turn on the switch transistor. The purpose of C2 is to remove transients that can appear across R2 and cause erratic switching. It should not be made so large that it severely integrates the waveform fed back to this point.

For additional information on switching regulators see "Designing Switching Regulators," National Semiconductor AN-2, August, 1968.

HIGH CURRENT SWITCHING REGULATOR

Output currents up to 3A can be obtained using the switching regulator circuit shown here. The circuit is identical to the one described previously, except that Q2 has been added to increase the output current capability by about an order of magnitude. It should be noted that the reference supply terminal is returned to the base of Q2, rather than the unregulated input. This is done because the LM104 will not function properly if Pin 5 gets more than 2V more positive than Pin 3. The reference current, as well as the bias currents for Pins 3 and 5, is supplied from the unregulated input through R5, so its resistance must be low enough so that Q2 is not turned on with about 2 mA flowing through it.

The line regulation of this circuit is worsened somewhat by the unregulated input voltage being fed back into the reference for the regulator through R6. This effect can be eliminated by connecting a 0.01 μF capacitor in series with R6 to remove the dc component of the feedback.



†Solid Tantalum

*60 turns No. 20 on Arnold Engineering A930157-2 Molybdenum Permalloy Core

There are a number of precautions that should be observed with all switching regulators, although they are more inclined to cause problems in high-current applications:

For one, fast switching diodes and transistors must be used. If D1 is an ordinary junction rectifier, voltages in the order of 10V can be developed across it in the forward direction when the switch transistor turns off. This happens because low-frequency rectifiers are usually manufactured with a PIN structure which presents a high forward impedance until enough minority carriers are injected into the diode base region to increase its conductance. This not only causes excessive dissipation in the diode, but the diode also presents a short circuit to the switch transistor, when it first turns on, until all the charge stored in the base region of the diode is removed. Similarly, a high frequency switch transistor must be used as excessive switching losses in low frequency transistors, like the 2N3055, make them overheat.

It is important that the core material used for the inductor have a soft saturation characteristic. Cores that saturate abruptly produce excessive peak currents in the switch transistor if the output current becomes high enough to run the core close to saturation. Powdered molybdenum-permalloy cores, on the other hand, exhibit a gradual reduction in permeability with excessive current, so the only effect of output currents above the design value is a gradual increase in switching frequency.

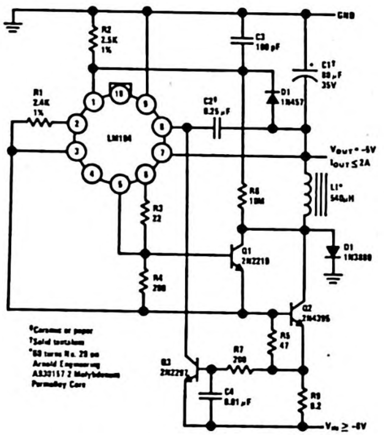
One thing that is frequently overlooked in the design of switching circuits is the ripple rating of the filter capacitors. Excessive high-frequency ripple can cause these capacitors to fail. This is an especially-important consideration for capacitors used on the unregulated input as the ripple current through them can be higher than the dc load current. The situation is eased somewhat for the filter capacitor on the output of the regulator since the ripple current is only a fraction of the load current. Nonetheless, proper design usually requires that the voltage rating of this capacitor be higher than that dictated by the dc voltage across it for reliable operation.

One unusual problem that has been noted in working with switching regulators is excessive dissipation in the switch transistors caused by high emitter-base saturation voltage. This can also show up as erratic operation if Q1 is the defective device. This saturation voltage can be as high as 5V and is the result of poor alloying on the base contact of the transistor. A defective transistor will not usually show up on a curve tracer because the low base current needed for linear operation does not produce a large voltage drop across the poorly-alloyed contact. However, a bad device can be spotted by probing on the bases of the switch transistors while the circuit is operating.

It is necessary that the catch diode, D1, and any bypass capacitance on the unregulated input be returned to ground separately from the other parts of the circuit. These components carry large current transients and can develop appreciable voltage transients across even a short length of wire. If C1, C2, or R2 have any common ground impedance with the catch diode or the input bypass capacitor, the transients can appear directly on the output.

SWITCHING REGULATOR WITH CURRENT LIMITING

The switching regulator circuits described previously are not protected from overloads or a short-circuited output. The current limiting of the LM104 is used to limit the base drive of the switch transistor, but this does not effectively protect the switch transistor from excessive current. Providing short circuit protection is no simple problem, since it is necessary to keep the regulator operating in the switching mode when the output is shorted. Otherwise, the dissipation in the switch transistor will become excessive even though the current is limited.



*Ceramic or paper

†Solid tantalum

*60 turns No. 20 on Arnold Engineering A930157-2 Molybdenum Permalloy Core

A circuit which provides current limiting and protects the regulator from short circuits is shown here. The current through the switch transistor produces a voltage drop across R9. When this voltage becomes large enough to turn on Q3, current limiting is initiated. This occurs because Q3 takes over as the control transistor and regulates the voltage on Pin 8 of the LM104. This point, which is the feedback terminal of the error amplifier, is separated from the actual output of the regulator by not shorting the regulated output and booster output terminals of the integrated circuit. Hence, with excessive output current, the circuit still operates as a switching regulator with Q3 regulating the voltage fed back to the error amplifier as the output voltage falls off.

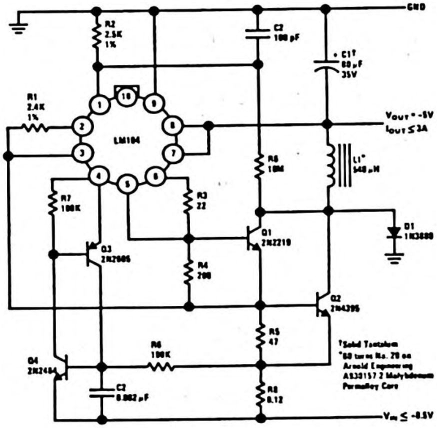
A resistor, R7, is included so that excessive base current will not be driven into the base of Q3. C4 insures that Q3 does not turn on from the current spikes through the switch transistor caused by pulling the stored charge out of the catch diode (these are about twice the load current). This capacitor also operates in conjunction with C2 to produce sufficient phase delay in the feedback loop so that the circuit will oscillate in current limiting. However, C4 should not be made so large that it appreciably integrates the rectangular waveform of the current through the switch transistor.

As the output voltage falls below half the design value, D1 pulls down the reference voltage across R2. This permits the current limiting circuitry to keep operating when the unregulated input voltage drops below the design value of output voltage, with a short on the output of the regulator.

A transistor with good high-current capability was chosen for Q3 so that it does not suffer from secondary breakdown effects from the large peak currents (about 200 mA) through it. With a shorted output, these peak currents occur with the full input voltage across Q3. The average dissipation in Q3 is, however, low.

SWITCHING REGULATOR WITH OVERLOAD SHUTOFF

An alternate method for protecting a switching regulator from excessive output currents is shown here. When the output current becomes too high, the voltage drop across the current-sense resistor, R8, fires an SCR which shuts off the regulator. The regulator remains off, dissipating practically no power, until it is reset by removing the input voltage.



†Solid Tantalum

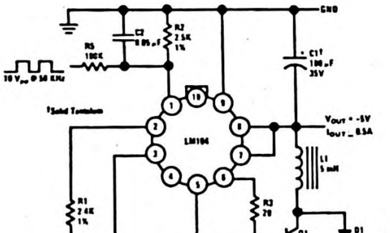
*60 turns No. 20 on Arnold Engineering A930157 2 Molybdenum Permalloy Core

In the actual circuit, complementary transistors, Q3 and Q4, replace the SCR since it is difficult to find devices with a low enough holding current (about 25 μA). When the voltage drop across R8 becomes large enough to turn on Q4, this removes the base drive for the output transistors of the LM104 through Pin 4. When this happens Q3 latches Q4, holding the regulator off until the input voltage is removed. It will then start when power is applied if the overload has been removed.

With this circuit, it is necessary that the shutoff current be 1.5 times the full load current. Otherwise, the circuit will shut off when it is switched on with a full load because of the excess current required to charge the output capacitor. The shutoff current can be made closer to the full load current by connecting a 10 μF capacitor across R2 which will limit the charging current for C1 by slowing the risetime of the output voltage when the circuit is turned on. However, this capacitor will also bypass the positive feedback from R6 which makes the regulator oscillate. Therefore, it is necessary to put a 270Ω resistor in the ground end of the added capacitor and provide feedback to this resistor from the collector of Q1 through a 1 MΩ resistor.

DRIVEN SWITCHING REGULATOR

When a number of switching regulators are operated from a common power source, it is desirable to synchronize their operation to more uniformly distribute the switched current waveforms in the input line. Synchronous operation can also be beneficial when a switching regulator is operated in conjunction with a power converter.



A circuit which synchronizes the switching regulator with a square wave drive signal is shown here. It differs from the switching regulators described previously in that positive feedback is not used. Instead, a triangular wave with a peak-to-peak amplitude of 25 mV is applied to the noninverting input of the error amplifier. The waveform is obtained by integrating the square wave synchronizing signal. This triangular wave causes the error amplifier to switch because its gain is high enough that the waveform easily overdrives it. The switching duty cycle is controlled by the output voltage fed back to the error amplifier. If the output voltage goes up, the duty cycle will decrease since the error amplifier will pick off a smaller portion of the triangular wave. Similarly, the duty cycle will decrease if the output voltage drops. Hence, the duty cycle is controlled to produce the desired output voltage.

Without a synchronous drive signal, the circuit will self oscillate at a frequency determined by L1 and C1. This self-oscillation frequency must be lower than the synchronous drive frequency. Therefore, more filtering is required for a driven regulator than for a self-oscillating regulator operating at the same frequency. This also means that a driven regulator will have less output ripple.

The value of C2 is chosen so that its capacitive reactance at the drive frequency is less than one-tenth the resistance of R2. The amplitude of the triangular wave is set at 25 mV with R5. It is advisable to ac couple the drive signal by putting a capacitor in series with R5 so that it does not disturb the dc reference voltage developed for the error amplifier.

THE LM104 REGULATOR

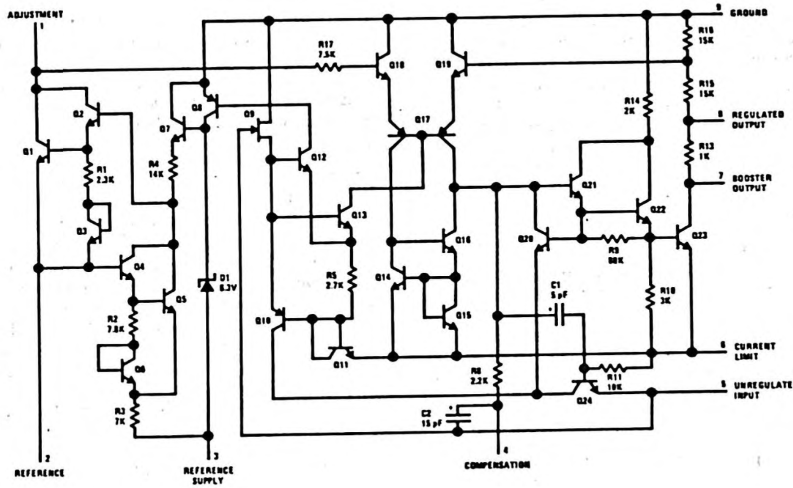
The basic reference for the regulator is zener diode D1. The reference diode is supplied from a PNP current source, Q8, which has a fixed current gain of 2. This arrangement permits the circuit to operate with unregulated input voltages as low as 7V, substantially increasing the efficiency of low-voltage regulators.

The reference supply is temperature compensated by using the negative temperature coefficient of the transistor emitter-base voltages to cancel the positive coefficient of the zener diode. The design produces a nominal 2.4V between the reference and reference supply terminals of the integrated circuit. Connecting an external 2.4 KΩ resistor between those terminals gives a 1 mA reference current from the collectors of Q1 and Q2, which is independent of temperature. The reference voltage supplied to the error amplifier is developed across a second external resistor connected between the adjustment terminal and ground.

The reference supply terminal is normally connected to the unregulated supply. However, improved line regulation can be obtained by pre-regulating the voltage on this terminal. This improvement occurs because Q1, Q2, and Q7 do not see changes in input voltage. Normally, it is the change in the emitter-base voltage of these transistors with changes in collector-base voltage which determines the line regulation.

When the reference supply and unregulated input terminals are operated from separate voltage sources, it is important to make sure that the unregulated input terminal of the integrated circuit does not get more than 2V more positive than the reference supply terminal. If this happens, the collector-isolation junction of Q6 becomes forward biased and disrupts the reference.

The error amplifier of the regulator is quite similar to the LM101 operational amplifier. Emitter


ADJUSTMENT
1
Q1
Q2
R1
2.3K
Q3
Q4
Q5
R2
7.8K
Q6
R3
7K
R4
14K
Q7
Q8
D1
6.3V
Q9
Q10
Q11
Q12
Q13
R5
2.7K
Q14
Q15
Q16
Q17
Q18
Q19
R17
7.5K
R16
15K
R15
15K
R14
2K
R13
1K
Q20
Q21
Q22
Q23
Q24
R9
60K
R10
3K
R11
10K
R8
2.2K
C1
5 pF
C2
15 pF
9 GROUND
8 REGULATED OUTPUT
7 BOOSTER OUTPUT
6 CURRENT LIMIT
5 UNREGULATED INPUT
4 COMPENSATION
2
REFERENCE
3
REFERENCE SUPPLY

follower input transistors, Q18 and Q19, drive a dual PNP which is operated in the common-base configuration. The current gain of these PNP transistors is fixed at 4 so that the base can be driven by a current source (Q13). Active collector loads are used for the input stage so that a voltage gain of 2000 is obtained. Q21 and Q22 provide enough current gain to keep the internal, series-pass transistor from loading the input stage. R14 limits the base drive on Q23 when it saturates with low, unregulated input voltages. The collector of Q23 is brought out separately so that an external booster transistor can be added for increased output current capability. R13 established the minimum operating current in Q23 when booster transistors are used.

One feature of the error amplifier is that it operates properly with common mode voltages all the way up to ground. Because of this, the circuit will regulate with output voltages to zero volts.

Current limiting is provided by Q24. When the voltage between the current limit and unregulated input terminals becomes large enough to turn on Q24, it will pull Q10 out of saturation and remove base drive from Q21 through Q20. This causes the series pass transistor to exhibit a constant current characteristic. The pre-load current, provided for Q24 by Q10 before current limiting is initiated, gives a much sharper current-limit characteristic. C1 and R11 are included in the limiting circuitry to suppress oscillations.

The error amplifier is connected to a divider on the output (R15 and R16) to keep the reference current generator from saturating with low input-output voltage differentials. A compensating resistor, R17, which is equal to the equivalent resistance of the divider is included to minimize offset error in the error amplifier.

The major feedback loop is frequency compensated by the brute-force method of rolling off the response with a relatively large capacitor on the output. C2 is included on the integrated circuit to compensate for the effects of series resistance in the output capacitor. A compensation point is also brought out so that more capacitance can be added across C2 for certain regulator configurations. R8 improves the load-transient response, especially when compensation is added on Pin 4.

The purpose of Q9, which is a collector FET, is to bias the current-source transistors, Q12 and Q13. It also supplies the preload current for the current-limit transistor, Q24, through Q10.

AN-23 The LM105 — An Improved Positive Regulator

The LM105 — An Improved Positive Regulator

National Semiconductor
Application Note 23
January 1969

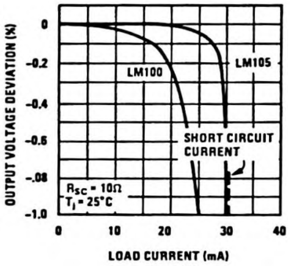
INTRODUCTION

IC voltage regulators are seeing rapidly increasing usage. The LM100, one of the first, has already been widely accepted. Designed for versatility, this circuit can be used as a linear regulator, a switching regulator, a shunt regulator, or even a current regulator. The output voltage can be set between 2V and 30V with a pair of external resistors, and it works with unregulated input voltages down to 7V. Dissipation limitations of the IC package restrict the output current to less than 20 mA, but external transistors can be added to obtain output currents in excess of 5A. The LM100 and an extensive description of its use in many practical circuits are described in References 1-3.

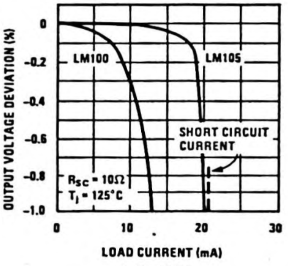
One complaint about the LM100 has been that it does not have good enough regulation for certain applications. In addition, it becomes difficult to prove that the load regulation is satisfactory under worst-case design conditions. These problems prompted development of the LM105, which is nearly identical to the LM100 except that a gain stage has been added for improved regulation. In the great majority of applications, the LM105 is a plug-in replacement for the LM100.

THE IMPROVED REGULATOR

The load regulation of the LM100 is about 0.1%, no load to full load, without current limiting. When short circuit protection is added, the regulation begins to degrade as the output current becomes greater than about half the limiting current. This is illustrated in Figure 1. The LM105, on the other hand, gives 0.1% regulation up to currents closely approaching the short circuit current. As shown in Figure 1b, this is particularly significant at high temperatures.



a. T_j = 25°C



b. T_j = 125°C

FIGURE 1. Comparison Between the Load Regulation of the LM100 and LM105 for Equal Short Circuit Currents

The current limiting characteristics of a regulator are important for two reasons: First, it is almost mandatory that a regulator be short-circuit protected because the output is distributed to enough places that the probability of it becoming shorted is quite high. Secondly, the sharpness of the limiting characteristics is not improved by the addition of external booster transistors. External transistors can increase the maximum output current, but they do not improve the load regulation at currents approaching the short circuit current. Thus, it can be seen that the LM105 provides more than ten times better load regulation in practical power supply designs.

Figure 2 shows that the LM105 also provides better line regulation than the LM100. These curves give the percentage change in output voltage for an incremental change in the unregulated input voltage. They show that the line regulation is worst for small differences between the input and output voltages. The LM105 provides about three times better regulation under worst case conditions. Bypassing the internal reference of the regulator makes the ripple rejection of the LM105 almost a factor of ten better than the LM100 over the entire operating range, as shown in the figure. This bypass capacitor also eliminates noise generated in the internal reference zener of the IC.

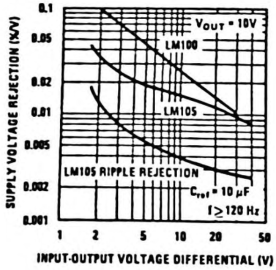


FIGURE 2. Comparison Between the Line Regulation Characteristics of the LM100 and LM105.

The LM105 has also benefited from the use of new IC components developed after the LM100 was designed. These have reduced the internal power consumption so that the LM105 can be specified for input voltages up to 50V and output voltages to 40V. The minimum preload current required by the LM100 is not needed on the LM105.

CIRCUIT DESCRIPTION

The differences between the LM100 and the LM105 can be seen by comparing the schematic diagrams in Figures 3 and 4. Q4 and Q5 have been added to the LM105 to form a common-collector, common-base, common-emitter amplifier, rather than the single common-emitter differential amplifier on the LM100.

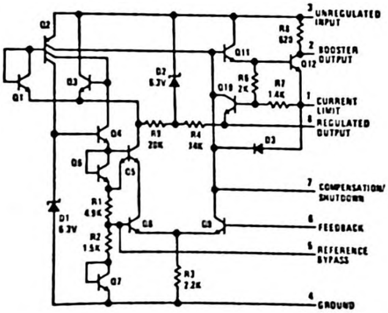

Q2
Q1
Q3
Q4
Q6
Q5
Q7
Q8
Q9
Q10
Q11
Q12
D1
6.3V
D2
6.3V
D3
R1
4.9K
R2
1.5K
R3
20K
R4
34K
R3
2.2K
R6
2K
R7
1.4K
R8
620
3 UNREGULATED INPUT
2 BOOSTER OUTPUT
1 CURRENT LIMIT
8 REGULATED OUTPUT
7 COMPENSATION/SHUTDOWN
6 FEEDBACK
5 REFERENCE BYPASS
4 GROUND

FIGURE 3. Schematic Diagram of the LM100 Regulator.

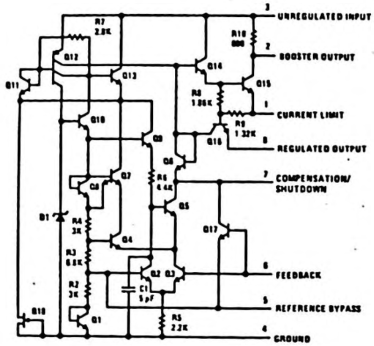

R7
2.8K
R10
800
Q11
Q12
Q13
Q14
Q15
R8
1.86K
R9
1.32K
Q16
Q10
Q9
Q8
Q7
Q6
R6
4.4K
Q5
D1
R4
3K
R3
6.8K
Q4
Q17
Q2
Q3
C1
5 pF
R2
3K
R5
2.2K
Q1
Q18
3 UNREGULATED INPUT
2 BOOSTER OUTPUT
1 CURRENT LIMIT
8 REGULATED OUTPUT
7 COMPENSATION/SHUTDOWN
6 FEEDBACK
5 REFERENCE BYPASS
4 GROUND

FIGURE 4. Schematic Diagram of the LM105 Regulator.

In the LM100, generation of the reference voltage starts with zener diode, D1, which is supplied with a fixed current from one of the collectors of Q2. This regulated voltage, which has a positive temperature coefficient, is buffered by Q4, divided down by R1 and R2 and connected in series with a diode-connected transistor, Q7. The negative temperature coefficient of Q7 cancels out the positive coefficient of the voltage across R2, producing a temperature-compensated 1.8V on the base of Q8. This point is also brought outside the circuit so that an external capacitor can be added to bypass any noise from the zener diode.

Transistors Q8 and Q9 make up the error amplifier of the circuit. A gain of 2000 is obtained from this single stage by using a current source, another collector on Q2, as a collector load. The output of the amplifier is buffered by Q11 and used to drive the series-pass transistor, Q12. The collector of Q12 is brought out so that an external PNP transistor, or PNP–NPN combination, can be added for increased output current.

Current limiting is provided by Q10. When the voltage across an external resistor connected between Pins 1 and 8 becomes high enough to turn on Q10, it removes the base drive from Q11 so the regulator exhibits a constant-current characteristic. Prebiasing the current limit transistor with a portion of the emitter-base voltage of Q12 from R6 and R7 reduces the current limit sense voltage. This increases the efficiency of the regulator, especially when foldback current limiting is used. With foldback limiting, the voltage dropped across the current sense resistor is about four times larger than the sense voltage.

As for the remaining details, the collector of the amplifier, Q9, is brought out so that external collector-base capacitance can be added to frequency-stabilize the circuit when it is used as a linear regulator. This terminal can also be grounded to shut the regulator off. R9 and R4 are used to start up the regulator, while the rest of the circuitry establishes the proper operating levels for the current source transistor, Q2.

The reference circuitry of the LM105 is the same, except that the current through the reference divider, R2, R3 and R4, has been reduced by a factor of two on the LM105 for reduced power consumption. In the LM105, Q2 and Q3 form an emitter coupled amplifier, with Q3 being the emitter-follower input and Q2 the common-base output amplifier. R6 is the collector load for this stage, which has a voltage gain of about 20. The second stage is a differential amplifier, using Q4 and Q5. Q5 actually provides the gain. Since it has a current source as a collector load, one of the collectors of Q12, the gain is quite high: about 1500. This gives a total gain in the error amplifier of about 30,000, which is ten times higher than the LM100.

It is not obvious from the schematic, but the first stage (Q2 and Q3) and second stage (Q4 and Q5) of the error amplifier are closely balanced when the circuit is operating. This will be true regardless of the absolute value of components and over the operating temperature range. The only thing affecting balance is component matching, which is good in a monolithic integrated circuit, so the error amplifier has good drift characteristics over a wide temperature range.

Frequency compensation is accomplished with an external integrating capacitor around the error amplifier, as with the LM100. This scheme makes the stability insensitive to loading conditions—resistive or reactive—while giving good transient response. However, an internal capacitor, C1, is added to prevent minor-loop oscillations due to the increased gain.

Additional differences between the LM100 and LM105 are that a field-effect transistor, Q18, connected as a current source starts the regulator when power is first applied. Since this current source is connected to ground, rather than the output, the minimum load current before the regulator drops out of operation with large input-output voltage differentials is greatly reduced. This also minimizes power dissipation in the integrated circuit when the difference between the input and output voltage is at the worst-case value. With the LM105 circuit configuration, it was also necessary to add Q17 to eliminate a latch-up mechanism which could exist with lower output-voltage settings. Without Q17, this could occur when Q3 saturated and cut off the second stage amplifiers, Q4 and Q5, causing the output to latch at a voltage nearly equal to the unregulated input.

POWER LIMITATIONS

Although it is desirous to put as much of the regulator as possible on the IC chip, there are certain basic limitations. For one, it is not a good idea to put the series pass transistor on the chip. The power that must be dissipated in the pass transistor is too much for practical IC packages. Further, IC's must be rated at a lower maximum operating temperature than power transistors. This means that even with a power package, a massive heat sink would be required if the pass transistor was included in the IC.

Assuming that these problems could be solved, it is still not advisable to put the pass transistor on the same chip with the reference and control circuitry: changes in the unregulated input voltage or load current produce gross variations in chip temperature. These variations worsen load and line regulation due to temperature interaction with the control and reference circuitry.

To elaborate, it is reasonable to neglect the package problem since it is potentially solvable. The lower, maximum operating temperatures of IC's, however, present a more basic problem. The control circuitry in an IC regulator runs at fairly low currents. As a result, it is more sensitive to leakage currents and other phenomena which degrades the performance of semiconductors at high temperatures. Hence, the maximum operating temperature is limited to 150°C in military temperature range applications. On the other hand, a power transistor operating at high currents may be run at temperatures up to 200°C, because even a 1 mA leakage current would not affect its operation in a properly designed circuit. Even if the pass transistor developed a permanent 1 mA leakage from channeling, operating under these conditions of high stress, it would not affect circuit operation. These conditions would not trouble the pass transistor, but they would most certainly cause complete failure of the control circuitry.

These problems are not eliminated in applications with a lower maximum operating temperature. Integrated circuits are sold for limited temperature range applications at considerably lower cost. This is mainly based on a lower maximum junction temperature. They may be rated so that they do not blow up at higher temperatures, but they are not guaranteed to operate within specifications at these temperatures. Therefore, in applications with a lower maximum ambient temperature, it is necessary to purchase an expensive full temperature range part in order to take advantage of the theoretical maximum operating temperatures of the IC.

Figure 5 makes the point about dissipation limitations more strongly. It gives the maximum short circuit output current for an IC regulator in a TO-5 package, assuming a 25°C temperature rise between the chip and ambient and a quiescent current of 2 mA. Dual-in-line or flat packages give results which are, at best, slightly better, but are usually worse. If the short circuit current is not of prime concern, Figure 5 can also be used to give the maximum output current as a function of input-output voltage differential. However, the increased dissipation due to the quiescent current flowing at the maximum input voltage must be taken into account. In addition, the input-output differential must be measured with the maximum expected input voltages.

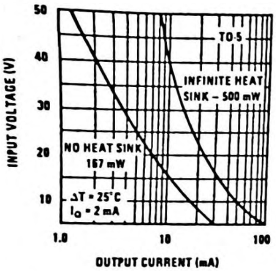


FIGURE 5. Dissipation Limited Short Circuit Output Current for an IC.Regulator in a TO-5 Package.

The 25°C temperature rise assumed in arriving at Figure 5 is not at all unreasonable. With military temperature range parts, this is valid for a maximum junction temperature of 150°C with a 125°C ambient. For low cost parts, marketed for limited temperature range applications, this maximum differential appropriately derates the maximum junction temperature.

In practical designs, the maximum permissible dissipation will always be to the left of the curve shown for an infinite heat sink in Figure 5. This curve is realized with the package immersed in circulating acetone, freon or mineral oil. Most heat sinks are not quite as good.

To summarize, power transistors can be run with a temperature differential, junction to ambient, 3 to 5 times as great as an integrated circuit. This means that they can dissipate much more power, even with a smaller heat sink. This, coupled with the fact that low cost, multilead power packages are not available and that there can be thermal interactions between the control circuitry and the pass transistor, strongly suggests that the pass transistors be kept separate from the integrated circuit.

USING BOOSTER TRANSISTORS

Figure 6 shows how an external pass transistor is added to the LM105. The addition of an external PNP transistor does not increase the minimum input output voltage differential. This would happen if an NPN transistor was used in a compound emitter follower connection with the NPN output transistor of the IC. A single-diffused, wide base transistor like the 2N3740 is recommended because it causes fewer oscillation problems than double-diffused, planar devices. In addition, it seems to be less prone to failure under overload conditions; and low cost devices are available in power packages like the TO-66 or even TO-3.

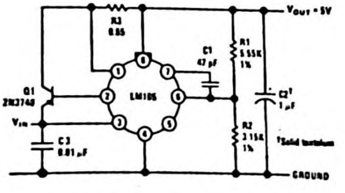


FIGURE 6. 0.2A Regulator.

When the maximum dissipation in the pass transistor is less than about 0.5W, a 2N2905 may be used as a pass transistor. However, it is generally necessary to carefully observe thermal deratings and provide some sort of heat sink.

In the circuit of Figure 6, the output voltage is determined by R1 and R2. The resistor values are selected based on a feedback voltage of 1.8V to Pin 6 of the LM105. To keep thermal drift of the output voltage within specifications, the parallel combination of R1 and R2 should be approximately 2K. However, this resistance is not critical. Variations of ±30% will not cause an appreciable degradation of temperature drift.

The 1 μF output capacitor, C2, is required to suppress oscillations in the feedback loop involving the external booster transistor, Q1, and the output transistor of the LM105. C1 compensates the internal regulator circuitry to make the stability independent for all loading conditions. C3 is not normally required if the lead length between the regulator and the output filter of the rectifier is short.

Current limiting is provided by R3. The current limit resistor should be selected so that the maximum voltage drop across it, at full load current, is equal to the voltage given in Figure 7 at the maximum junction temperature of the IC. This assures a no load to full load regulation better than 0.1% under worst-case conditions.

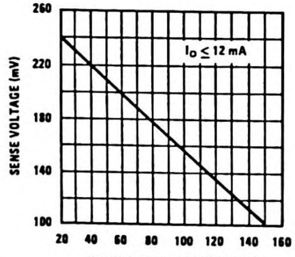


FIGURE 7. Maximum Voltage Drop Across Current Limit Resistor at Full Load for Worst Case Load Regulation of 0.1%.

The short circuit output current is also determined by R3. Figure 8 shows the voltage drop across this resistor, when the output is shorted, as a function of junction temperature in the IC.

With the type of current limiting used in Figure 6, the dissipation under short circuit conditions can be more than three times the worst-case full load dissipation. Hence, the heat sink for the pass tran-

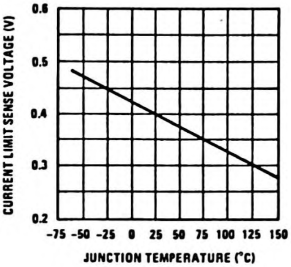


FIGURE 8. Voltage Drop Across Current Limit Resistor Required to Initiate Current Limiting.

sistor must be designed to accommodate the increased dissipation if the regulator is to survive more than momentarily with a shorted output. It is encouraging to note, however, that the short circuit current will decrease at higher ambient temperatures. This assists in protecting the pass transistor from excessive heating.

FOLDBACK CURRENT LIMITING

With high current regulators, the heat sink for the pass transistor must be made quite large in order to handle the power dissipated under worst-case conditions. Making it more than three times larger to withstand short circuits is sometimes inconvenient in the extreme. This problem can be solved with foldback current limiting, which makes the output current under overload conditions decrease below the full load current as the output voltage is pulled down. The short circuit current can be made but a fraction of the full load current.

A high current regulator using foldback limiting is shown in Figure 9. A second booster transistor, Q1, has been added to provide 2A output current without causing excessive dissipation in the LM105. The resistor across its emitter base junction bleeds off any collector base leakage and establishes a minimum collector current for Q2 to make the circuit easier to stabilize with light loads. The foldback characteristic is produced with R4 and R5. The voltage across R4 bucks out the voltage dropped across the current sense resistor, R3. Therefore, more voltage must be developed across R3 before current limiting is initiated. After the output voltage begins to fall, the bucking voltage is reduced, as it is proportional to the output voltage. With the output shorted, the current is reduced to a value determined by the current limit resistor and the current limit sense voltage of the LM105.

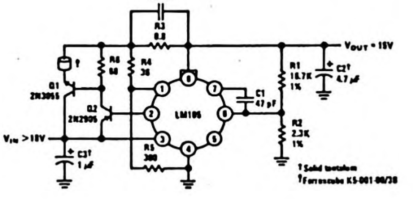


FIGURE 9. 2A Regulator with Foldback Current Limiting.

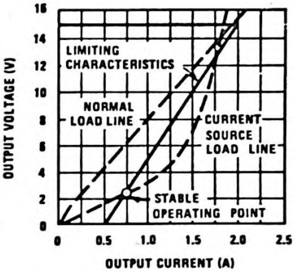


FIGURE 10. Limiting Characteristics of Regulator Using Foldback Current Limiting.

Figure 10 illustrates the limiting characteristics. The circuit regulates for load currents up to 2A. Heavier loads will cause the output voltage to drop, reducing the available current. With a short on the output, the current is only 0.5A.

In design, the value of R3 is determined from

$$R_3 = \frac{V_{lim}}{I_{SC}}, \tag{1}$$

where V_{lim} is the current limit sense voltage of the LM105, given in Figure 8, and I_{SC} is the design value of short circuit current. R5 is then obtained from

$$R_5 = \frac{V_{OUT} + V_{sense}}{I_{bleed} + I_{bias}}, \tag{2}$$

where V_{OUT} is the regulated output voltage, V_{sense} is maximum voltage across the current limit resistor for 0.1% regulation as indicated in Figure 7, I_{bleed} is the preload current on the regulator output provided by R5 and I_{bias} is the maximum current coming out of Pin 1 of the LM105 under full load conditions. I_{bias} will be equal to 2 mA plus the worst-case base drive for the PNP booster transistor, Q2. I_{bleed} should be made about ten times greater than I_{bias}.

Finally, R4 is given by

$$R_4 = \frac{I_{FL}\, R_3 - V_{sense}}{I_{bleed}} \tag{3}$$

where I_{FL} is the output current of the regulator at full load.

It is recommended that a ferrite bead be strung on the emitter of the pass transistor, as shown in Figure 9, to suppress oscillations that may show up with certain physical configurations. It is advisable to also include C4 across the current limit resistor.

In some applications, the power dissipated in Q2 becomes too great for a 2N2905 under worst-case conditions. This can be true even if a heat sink is used, as it should be in almost all applications. When dissipation is a problem, the 2N2905 can be replaced with a 2N3740. With a 2N3740, the ferrite bead and C4 are not needed because this transistor has a lower cutoff frequency.

One of the advantages of foldback limiting is that it sharpens the limiting characteristics of the IC. In addition, the maximum output current is less sensitive to variations in the current limit sense voltage of the IC: in this circuit, a 20% change in sense voltage will only affect the trip current by 5%. The temperature sensitivity of the full load current is likewise reduced by a factor of four, while the short circuit current is not.

Even though the voltage dropped across the sense resistor is larger with foldback limiting, the minimum input-output voltage differential of the complete regulator is not increased above the 3V specified for the LM105 as long as this drop is less than 2V. This can be attributed to the low sense voltage of the IC by itself.

Figure 10 shows that foldback limiting can only be used with certain kinds of loads. When the load looks predominately like a current source, the load line can intersect the foldback characteristic at a point where it will prevent the regulator from coming up to voltage, even without an overload. Fortunately, most solid state circuitry presents a load line which does not intersect. However, the possibility cannot be ignored, and the regulator must be designed with some knowledge of the load.

With foldback limiting, power dissipation in the pass transistor reaches a maximum at some point between full load and short circuited output. This is illustrated in Figure 11. However, if the maximum dissipation is calculated with the worst-case input voltage, as it should be, the power peak is not too high.

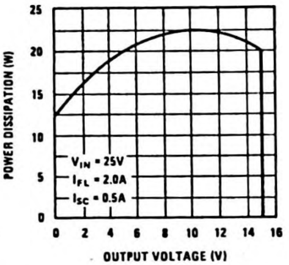


FIGURE 11. Power Dissipation in Series Pass Transistors Under Overload Conditions in Regulator Using Foldback Current Limiting.

HIGH CURRENT REGULATOR

The output current of a regulator using the LM105 as a control element can be increased to any desired level by adding more booster transistors, increasing the effective current gain of the pass transistors. A circuit for a 10A regulator is shown in Figure 12. A third NPN transistor has been included to get higher current. A low frequency device is used for Q3 because it seems to better withstand abuse. However, high frequency transistors must be used to drive it. Q2 and Q3 are both double-diffused transistors with good frequency response. This insures that Q3 will present the dominant lag in the feedback loop through the booster transistors, and back around the output transistor of the LM105. This is further insured by the addition of C3.

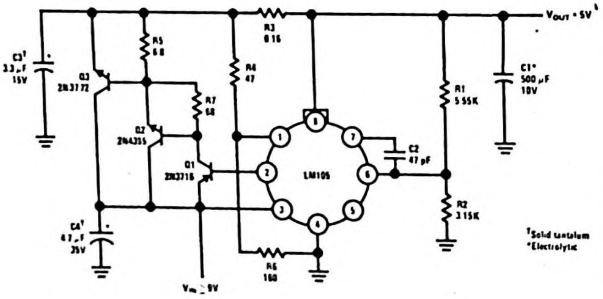


FIGURE 12. 10A Regulator with Foldback Current Limiting.

The circuit, as shown, has a full load capability of 10A. Foldback limiting is used to give a short circuit output current of 2.5A. The addition of Q3 increases the minimum input-output voltage differential, by 1V, to 4V.

DOMINANT FAILURE MECHANISMS

By far, the biggest reason for regulator failures is overdissipation in the series pass transistors. This has been borne out by experience with the LM100. Excessive heating in the pass transistors causes them to short out, destroying the IC. This has happened most frequently when PNP booster transistors in a TO-5 can, like the 2N2905, were used. Even with a good heat sink, these transistors cannot dissipate much more than 1W. The maximum dissipation is less in many applications. When a single PNP booster is used and power can be a problem, it is best to go to a transistor like the 2N3740, in a TO-66 power package, using a good heat sink.

Using a compound PNP/NPN booster does not solve all problems. Even when breadboarding with transistors in TO-3 power packages, heat sinks must be used. The TO-3 package is not very good, thermally, without a heat sink. Dissipation in the PNP transistor driving the NPN series pass transistor cannot be ignored either. Dissipation in the driver with worst-case current gain in the pass transistor must be taken into account. In certain cases, this could require that a PNP transistor in a power package be used to drive the NPN pass transistor. In almost all cases, a heat sink is required if a PNP driver transistor in a TO-5 package is selected.

With output currents above 3A, it is good practice to replace a 2N3055 pass transistor with a 2N3772. The 2N3055 is rated for higher currents than 3A, but its current gain falls off rapidly. This is especially true at either high temperatures or low input-output voltage differentials. A 2N3772 will give substantially better performance at high currents, and it makes life much easier for the PNP driver.

The second biggest cause of failures has been the output filter capacitors on power inverters providing unregulated power to the regulator. If these capacitors are operated with excessive ripple across them, and simultaneously near their maximum dc voltage rating, they will sputter. That is, they short momentarily and clear themselves. When they short, the output capacitor of the regulator is discharged back through the reverse biased pass transistors or the control circuitry, frequently causing destruction. This phenomenon is especially prevalent when solid tantalum capacitors are used with high-frequency power inverters. The maximum ripple allowed on these capacitors decreases linearly with frequency.

The solution to this problem is to use capacitors with conservative voltage ratings. In addition, the maximum ripple allowed by the manufacturer at the operating frequency should also be observed. The problem can be eliminated completely by installing a diode between the input and output of the regulator such that the capacitor on the output is discharged through this diode if the input is shorted. A fast switching diode should be used as ordinary rectifier diodes are not always effective.

Another cause of problems with regulators is severe voltage transients on the unregulated input. Even if these transients do not cause immediate failure in the regulator, they can feed through and destroy the load. If the load shorts out, as is frequently the case, the regulator can be destroyed by subsequent transients.

This problem can be solved by specifying all parts of the regulator to withstand the transient conditions. However, when ultimate reliability is needed, this is not a good solution. Especially since the regulator can withstand the transient, yet severely overstress the circuitry on its output by feeding the transients through. Hence, a more logical recourse is to include circuitry which suppresses the transients. A method of doing this is shown in Figure 13. A zener diode, which can handle large peak currents, clamps the input voltage to the regulator while an inductor limits the current through the zener during the transient. The size of the inductor is determined from

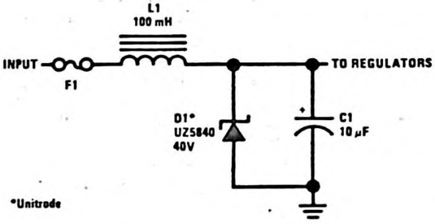


FIGURE 13. Suppression Circuitry to Remove Large Voltage Spikes from Unregulated Supplies.

$$L = \frac{\Delta V \Delta t}{I} \qquad (4)$$

where ΔV is the voltage by which the input transient exceeds the breakdown voltage of the diode, Δt is the duration of the transient and I is the peak current the zener can handle while still clamping the input voltage to the regulator. As shown, the suppression circuit will clamp 70V, 4 ms transients on the unregulated supply.

CONCLUSIONS

The LM105 is an exact replacement for the LM100 in the majority of applications, providing about ten times better regulation. There are, however, a few differences:

In switching regulator applications,[2] the size of the resistor used to provide positive feedback should be doubled as the impedance seen looking back into the reference bypass terminal is twice that of the LM100 (2 KΩ versus 1 KΩ). In addition, the minimum output voltage of the LM105 is 4.5V, compared with 2V for the LM100. In low voltage regulator applications, the effect of this is obvious. However, it also imposes some limitations on current regulator and shunt regulator designs.[3] Lastly, clamping the compensation terminal (Pin 7) within a diode drop of ground or the output terminal will not guarantee that the regulator is shut off, as it will with the LM100. This restricts the LM105 in the overload shutoff schemes[3] which can be used with the LM100.

Dissipation limitations of practical packages dictate that the output current of an IC regulator be less than 20 mA. However, external booster transistors can be added to get any output current desired. Even with satisfactory packages, considerably larger heat sinks would be needed if the pass transistors were put on the same chip as the reference and control circuitry, because an IC must be run at a lower maximum temperature than a power transistor. In addition, heat dissipated in the pass transistor couples into the low level circuitry and degrades performance. All this suggests that the pass transistor be kept separate from the IC.

Overstressing series pass transistors has been the biggest cause of failures with IC regulators. This not only applies to the transistors within the IC, but also to the external booster transistors. Hence, in designing a regulator, it is of utmost importance to determine the worst-case power dissipation in all the driver and pass transistors. Devices must then be selected which can handle the power. Further, adequate heat sinks must be provided as even power transistors cannot dissipate much power by themselves.

Normally, the highest power dissipation occurs when the output of the regulator is shorted. If this condition requires heat sinks which are so large as to be impractical, foldback current limiting can be used. With foldback limiting, the power dissipated under short circuit conditions can actually be made less than the dissipation at full load.

The LM105 is designed primarily as a positive voltage regulator. A negative regulator, the LM104, which is a functional complement to the LM105, is described in Reference 4.

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A Simplified Test Set for Op Amp Characterization

National Semiconductor
Application Note 24
M. Yamatake
June 1969

INTRODUCTION

The test set described in this paper allows complete quantitative characterization of all dc operational amplifier parameters quickly and with a minimum of additional equipment. The method used is accurate and is equally suitable for laboratory or production test—for quantitative readout or for limit testing. As embodied here, the test set is conditioned for testing the LM709 and LM101 amplifiers; however, simple changes discussed in the text will allow testing of any of the generally available operational amplifiers.

Amplifier parameters are tested over the full range of common mode and power supply voltages with either of two output loads. Test set sensitivity and stability are adequate for testing all presently available integrated amplifiers.

The paper will be divided into two sections, i.e., a functional description, and a discussion of circuit operation. Complete construction information will be given including a layout for the tester circuit boards.

FUNCTIONAL DESCRIPTION

The test set operates in one of three basic modes. These are: (1) Bias Current Test; (2) Offset Voltage, Offset Current Test; and (3) Transfer Function Test. In the first two of these tests, the amplifier under test is exercised throughout its full common mode range. In all three tests, power supply voltages for the circuit under test may be set at ±5V, ±10V, ±15V or ±20V.

POWER SUPPLY

Basic waveforms and dc operating voltages for the test set are derived from a power supply section comprising a positive and a negative rectifier and filter, a test set voltage regulator, a test circuit voltage regulator, and a function generator. The dc supplies will be discussed in the section dealing with detailed circuit description.

The waveform generator provides three output functions, a ±19V square wave, a −19V to +19V pulse with a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic waveform from which both the pulse and triangular wave outputs are derived.

The square wave generator is an operational amplifier connected as an astable multivibrator. This amplifier provides an output of approximately ±19V at 16 Hz. This square wave is used to drive junction FET switches in the test set and to generate the pulse and triangular waveforms.

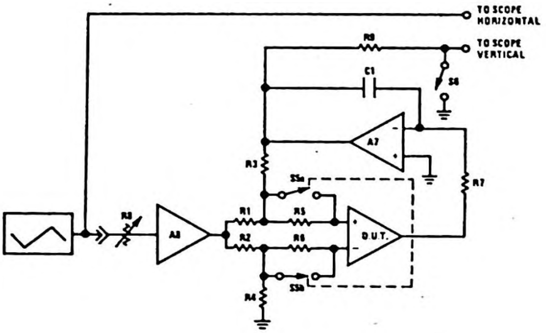


FIGURE 1. Functional Diagram of Bias Current Test Circuit

The pulse generator is a monostable multivibrator driven by the output of the square wave generator. This multivibrator is allowed to swing from negative saturation to positive saturation on the positive going edge of the square wave input and has a time constant which will provide a duty cycle of approximately 1%. The output is approximately −19V to +19V.

The triangular wave generator is a dc stabilized integrator driven by the output of the square wave generator and provides a ±5V output at the square wave frequency, inverted with respect to the square wave.

The purpose of these various outputs from the power supply section will be discussed in the functional description.

BIAS CURRENT TEST

A functional diagram of the bias current test circuit is shown in Figure 1. The output of the triangular wave generator and the output of the test circuit, respectively, drive the horizontal and vertical deflection of an oscilloscope.

The device under test, (cascaded with the integrator, A_7), is connected in a differential amplifier configuration by R_1, R_2, R_3, and R_4. The inputs of this differential amplifier are driven in common from the output of the triangular wave generator through attenuator R_8. and amplifier A_8. The inputs of the device under test are connected to the feedback network through resistors R_5 and R_6, shunted by the switch S_{5a} and S_{5b}.

The feedback network provides a closed loop gain of 1,000 and the integrator time constant serves to reduce noise at the output of the test circuit as well as allowing the output of the device under test to remain near zero volts.

The bias current test is accomplished by allowing the device under test to draw input current to one of its inputs through the corresponding input resistor on positive going or negative going halves of the triangular wave generator output. This is accomplished by closing S_{5a} or S_{5b} on alternate halves of the triangular wave input. The voltage appearing across the input resistor is equal to input current times the input resistor. This voltage is multiplied by 1,000 by the feedback loop and appears at the integrator output and the vertical input of the oscilloscope. The vertical separation of the traces representing the two input currents of the amplifier under test is equivalent to the total bias current of the amplifier under test.

The bias current over the entire common mode range may be examined by setting the output of A_8 equal to the amplifier common mode range. A photograph of the bias current oscilloscope display is given as Figure 2. In this figure, the total input current of an amplifier is displayed over a ±10V common mode range with a sensitivity of 100 nA per vertical division.

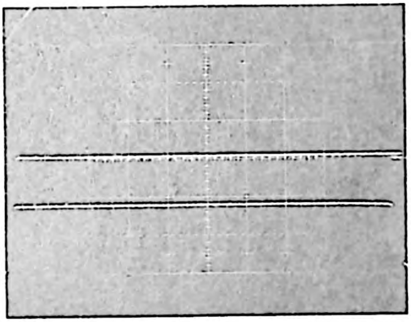


FIGURE 2. Bias Current and Common Mode Rejection Display

The bias current display of Figure 2 has the added advantage that incipient breakdown of the input stage of the device under test at the extremes of the common mode range is easily detected.

If either or both the upper or lower trace in the bias current display exhibits curvature near the horizontal ends of the oscilloscope face, then the bias current of that input of the amplifier is shown to be dependent on common mode voltage. The usual causes of this dependency are low breakdown voltage of the differential input stage or current sink.

OFFSET VOLTAGE, OFFSET CURRENT TEST

The offset voltage and offset current tests are performed in the same general way as the bias current test. The only difference is that the switches S_{5a} and S_{5b} are closed on the same half-cycle of the triangular wave input.

The synchronous operation of S_{5a} and S_{5b} forces the amplifier under test to draw its input currents through matched high and low input resistors on alternate halves of the input triangular wave. The difference between the voltage drop across the two values of input resistors is proportional to the difference in input current to the two inputs of the amplifier under test and may be measured as the vertical spacing between the two traces appearing on the face of the oscilloscope.

Offset voltage is measured as the vertical spacing between the trace corresponding to one of the two values of source resistance and the zero volt baseline. Switch S_6 and Resistor R_9 are a base line chopper whose purpose is to provide a baseline reference which is independent of test set and oscilloscope drift. S_6 is driven from the pulse output of the function generator and has a duty cycle of approximately 1% of the triangular wave.

Figure 3 is a photograph of the various waveforms presented during this test. Offset voltage and offset current are displayed at a sensitivity of 1 mV and 100 nA per division, respectively, and both parameters are displayed over a common mode range of ±10V.

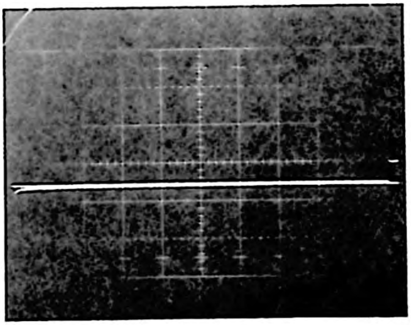


FIGURE 3. Offset Voltage, Offset Current and Common Mode Rejection Display

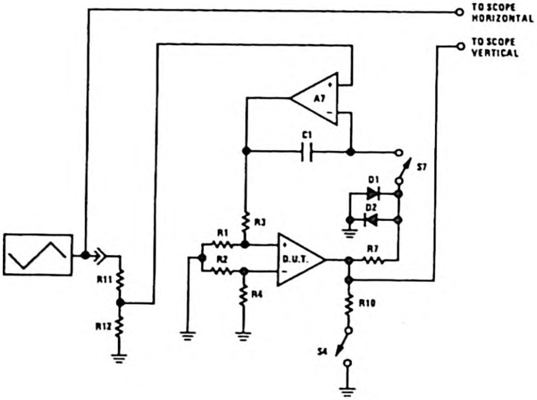


FIGURE 4. Functional Diagram of Transfer Function Circuit

TRANSFER FUNCTION TEST

A functional diagram of the transfer function test is shown in Figure 4. The output of the triangular wave generator and the output of the circuit under test, respectively, drive the horizontal and vertical inputs of an oscilloscope.

The device under test is driven by a ±2.5 mV triangular wave derived from the ±5V output of the triangular wave generator through the attenuators R_{11}, R_{12}, and R_1, R_3 and through the voltage follower, A_7. The output of the device under test is fed to the vertical input of an oscilloscope.

Amplifier A_7 performs a dual function in this test. When S_7 is closed during the bias current test, a voltage is developed across C_1 equal to the amplifier offset voltage multiplied by the gain of the feedback loop. When S_7 is opened in the transfer function test, the charge stored in C_1 continues to provide this offset correction voltage. In addition, A_7 sums the triangular wave test signal with the offset correction voltage and applies this sum to the input of the amplifier under test through the attenuator R_1, R_3. This input sweeps the input of the amplifier under test ±2.5 mV around its offset voltage.

Figure 5 is a photograph of the output of the test set during the transfer function test. This figure illustrates the function of amplifier A_7 in adjusting the dc input of the test device so that its transfer function is displayed on the center of the oscilloscope face.

The transfer function display is a plot of V_{in} vs V_{out} for an amplifier. This display provides information about three amplifier parameters: gain,

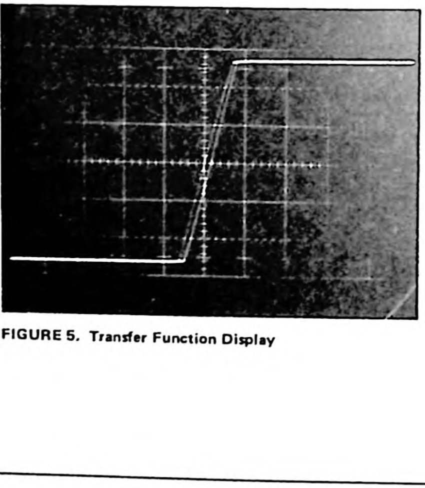
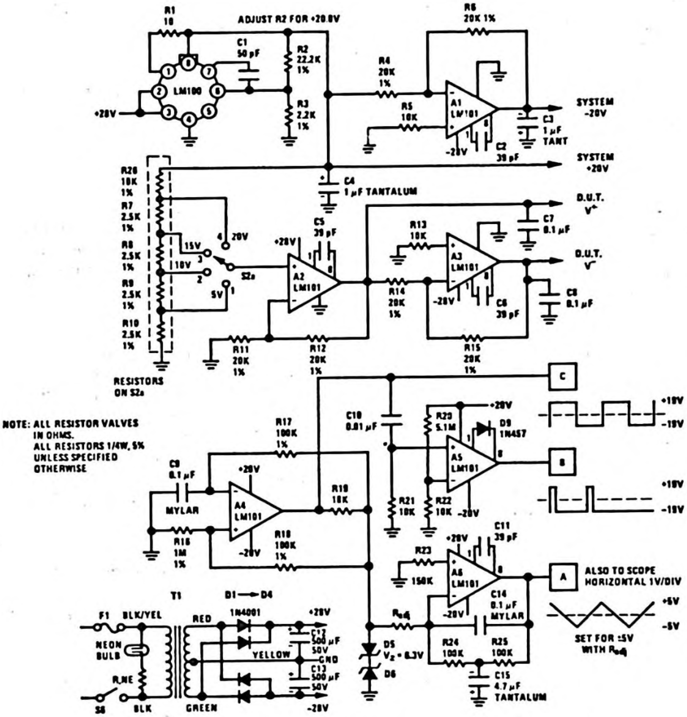


FIGURE 5. Transfer Function Display


R1
10
ADJUST R2 FOR +20.0V
R6
20K 1%
C1
50 pF
R2
22.2K
1%
LM100
+20V
R3
2.2K
1%
R4
20K
1%
R5
10K
A1
LM101
-20V
C2
39 pF
C3
1 µF
TANT
SYSTEM
-20V
SYSTEM
+20V
R20
10K
1%
R7
2.5K
1%
R8
2.5K
1%
R9
2.5K
1%
R10
2.5K
1%
RESISTORS
ON S2a
C4
1 µF TANTALUM
20V
15V
10V
5V
S2a
+20V
C5
39 pF
A2
LM101
R11
20K
1%
R12
20K
1%
R13
10K
A3
LM101
-20V
R14
20K
1%
C6
39 pF
R15
20K
1%
C7
0.1 µF
C8
0.1 µF
D.U.T.
V+
D.U.T.
V-
C
B
A
+19V
-19V
+19V
-19V
C10
0.01 µF
R23
5.1M
D9
1N457
+20V
A5
LM101
R21
10K
R22
10K
-20V
R17
100K
1%
C9
0.1 µF
MYLAR
+20V
A4
LM101
R19
10K
R16
1M
1%
-20V
R18
100K
1%
C11
39 pF
+20V
R23
150K
A6
LM101
-20V
C14
0.1 µF
MYLAR
ALSO TO SCOPE
HORIZONTAL 1V/DIV
+5V
-5V
SET FOR ±5V
WITH Radj
Radj
R24
100K
R25
100K
C15
4.7 µF
TANTALUM
D5
Vz = 6.3V
D6
T1
D1 → D4
1N4001
F1
BLK/YEL
RED
+28V
NEON
BULB
RNE
S6
BLK
GREEN
YELLOW
C12
500 µF
50V
GND
C13
500 µF
50V
-28V

NOTE: ALL RESISTOR VALVES IN OHMS.
ALL RESISTORS 1/4W, 5% UNLESS SPECIFIED OTHERWISE

FIGURE 6. Power Supply and Function Generator

gain linearity, and output swing. Gain is displayed as the slope, $\Delta V_{out}/\Delta V_{in}$ of the transfer function. Gain linearity is indicated change in slope of the V_{out}/V_{in} display as a function of output voltage. This display is particularly useful in detecting crossover distortion in a Class B output stage. Output swing is measured as the vertical deflection of the transfer function at the horizontal extremes of the display.

DETAILED CIRCUIT DESCRIPTION

POWER SUPPLIES

As shown in Figure 6, which is a complete schematic of the power supply and function generator, two power supplies are provided in the test set. One supply provides a fixed ±20V to power the circuitry in the test set; the other provides ±5V to ±20V to power the circuit under test.

The test set power supply regulator accepts +28V from the positive rectifier and filter and provides +20V through the LM100 positive regulator. Amplifier A_1 is powered from the negative rectifier and filter and operates as a unity gain inverter whose input is +20V from the positive regulator, and whose output is −20V.

The test circuit power supply is referenced to the +20V output of the positive regulator through the variable divider comprising R_7, R_8, R_9, R_{10}, and R_{26}. The output of this divider is +10V to +2.5V according to the position of S_{2a} and is fed to the non-inverting, gain-of-two amplifier, A_2. A_2 is powered from +28V and provides +20V to +5V at its output. A_3 is a unity gain inverter whose input is the output of A_2 and which is powered from −28V. The complementary outputs of amplifiers A_2 and A_3 provide dc power to the circuit under test.

LM101 amplifiers are used as A_2 and A_3 to allow operation from one ground referenced voltage each and to provide protective current limiting for the device under test.

FUNCTION GENERATOR

The function generator provides three outputs, a ±19V square wave, a −19V to +19V pulse having a 1% duty cycle, and a ±5V triangular wave. The square wave is the basic function from which the pulse and triangular wave are derived, the pulse is referenced to the leading edge of the square wave, and the triangular wave is the inverted and integrated square wave.

Amplifier A_4 is an astable multivibrator generating a square wave from positive to negative saturation. The amplitude of this square wave is approximately ±19V. The square wave frequency is determined by the ratio of R_{18} to R_{16} and by the time constant, $R_{17}C_9$. The operating frequency is stabilized against temperature and power regulation effects by regulating the feedback signal with the divider R_{19}, D_5 and D_6.

Amplifier A_5 is a monostable multivibrator triggered by the positive going output of A_4. The pulse width of A_5 is determined by the ratio of R_{20} to R_{22} and by the time constant $R_{21}C_{10}$. The output pulse of A_5 is an approximately 1% duty cycle pulse from approximately −19V to +19V.

Amplifier A_6 is a dc stabilized integrator driven from the amplitude-regulated output of A_4. Its output is a ±5V triangular wave. The amplitude of the output of A_6 is determined by the square wave voltage developed across D_5 and D_6 and the time constant R_{adj} C_{14}. DC stabilization is accomplished by the feedback network R_{24}, R_{25}, and C_{15}. The ac attenuation of this feedback network is high enough so that the integrator action at the square wave frequency is not degraded.

Operating frequency of the function generator may be varied by adjusting the time constants associated with A_4, A_5, and A_6 in the same ratio.

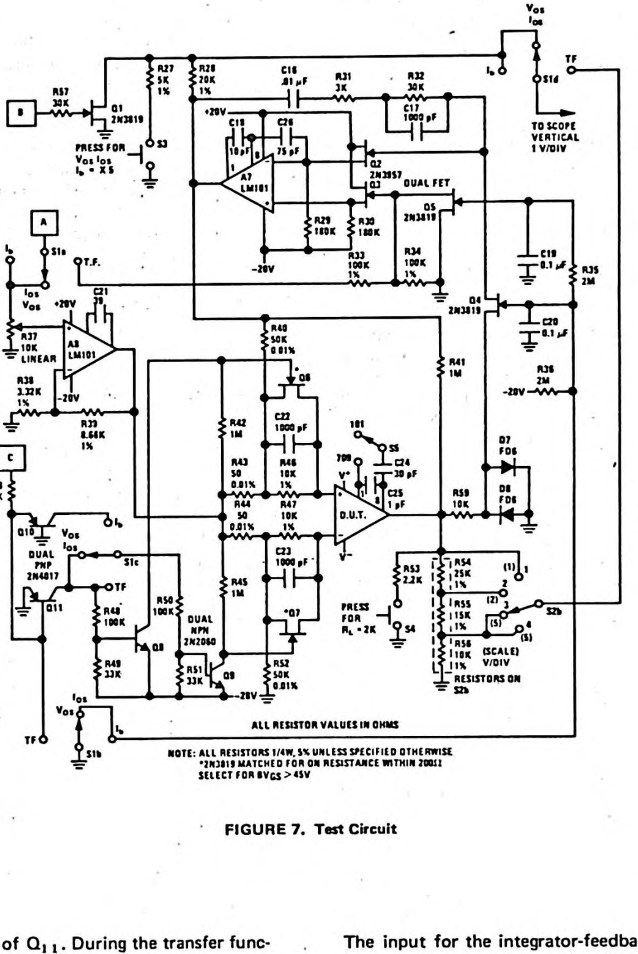
TEST CIRCUIT

A complete schematic diagram of the test circuit is shown in Figure 7. The test circuit accepts the outputs of the power supplies and function generator and provides horizontal and vertical outputs for an X-Y oscilloscope, which is used as the measurement system.

The primary elements of the test circuit are the feedback buffer and integrator, comprising amplifier A_7 and its feedback network C_{16}, R_{31}, R_{32}, and C_{17}, and the differential amplifier network, comprising the device under test and the feedback network R_{40}, R_{43}, R_{44}, and R_{52}. The remainder of the test circuit provides the proper conditioning for the device under test and scaling for the oscilloscope, on which the test results are displayed.

The amplifier A_8 provides a variable amplitude source of common mode signal to exercise the amplifier under test over its common mode range. This amplifier is connected as a non-inverting gain-of-3.6 amplifier and receives its input from the triangular wave generator. Potentiometer R_{37} allows the output of this amplifier to be varied from ±0 volts to ±18 volts. The output of this amplifier drives the differential input resistors, R_{43} and R_{44}, for the device under test.

The resistors R_{46} and R_{47} are current sensing resistors which sense the input current of the device under test. These resistors are switched into the circuit in the proper sequence by the field effect transistors Q_6 and Q_7. Q_6 and Q_7 are driven from the square wave output of the function generator by the PNP pair, Q_{10} and Q_{11}, and the NPN pair, Q_8 and Q_9. Switch sections S_{1b} and S_{1c} select the switching sequence for Q_8 and Q_9 and hence for Q_6 and Q_7. In the bias current test, the FET drivers, Q_8 and Q_9, are switched by out of phase signals from Q_{10} and Q_{11}. This opens the FET switches Q_6 and Q_7 on alternate half cycles of the square wave output of the function generator. During the offset voltage, offset current test, the FET drivers are operated synchronously



Vos
Ios
Ib
S1d
TF
TO SCOPE
VERTICAL
1 V/DIV
R57
30K
Q1
2N3819
R27
5K
1%
R28
20K
1%
PRESS FOR
Vos Ios
Ib = X 5
S3
C16
.01 μF
R31
3K
R32
30K
C17
1000 pF
+20V
C18
10 pF
C26
75 pF
A7
LM101
Q2
2N3957
Q3
DUAL FET
Q5
2N3819
R29
180K
R30
180K
-20V
R33
100K
1%
R34
100K
1%
C19
0.1 μF
R35
2M
Q4
2N3819
C20
0.1 μF
R36
2M
-20V
A
B
C
S1a
Ib
T.F.
Ios
Vos
+20V
C21
30
R37
10K
LINEAR
A8
LM101
R38
3.32K
1%
-20V
R39
6.66K
1%
R40
50K
0.01%
Q6
R41
1M
C22
1000 pF
R42
1M
101
709
S5
C24
30 pF
V+
C25
1 pF
D.U.T.
V-
D7
FD6
D8
FD6
R59
10K
R43
50
0.01%
R46
10K
1%
R44
50
0.01%
R47
10K
1%
C23
1000 pF
R45
1M
R58
30K
Q10
DUAL
PNP
2N4017
Q11
Vos
Ios
S1c
TF
R48
100K
R49
33K
Q8
R50
100K
DUAL
NPN
2N2060
R51
33K
Q9
*Q7
R52
50K
0.01%
-20V
R53
2.2K
PRESS
FOR
RL = 2K
S4
R54
25K
1%
R55
15K
1%
R56
10K
1%
(1) 1
2
(2) 3
(5) 4
(5)
S2b
(SCALE)
V/DIV
RESISTORS ON
S2b
Ios
Vos
Ib
TF
S1b

ALL RESISTOR VALUES IN OHMS

NOTE: ALL RESISTORS 1/4W, 5% UNLESS SPECIFIED OTHERWISE
*2N3819 MATCHED FOR ON RESISTANCE WITHIN 20Ω
SELECT FOR $BV_{GS} > 45V$

FIGURE 7. Test Circuit

from the output of Q_{11}. During the transfer function test, Q_6 and Q_7 are switched on continuously by turning off Q_{11}. R_{42} and R_{45} maintain the gates of the FET switches at zero gate to source voltage for maximum conductance during their on cycle. Since the sources of these switches are at the common mode input voltage of the device under test, these resistors are connected to the output of the common mode driver amplifier, A_8.

The input for the integrator-feedback buffer, A_7, is selected by the FET switches Q_4 and Q_5. During the bias current and offset voltage offset current tests, A_7 is connected as an integrator and receives its input from the output of the device under test. The output of A_7 drives the feedback resistor, R_{40}. In this connection, the integrator holds the output of the device under test near ground and serves to amplify the voltages corresponding to bias current, offset current, and offset voltage by a factor of 1,000 before presenting them to the measurement system. FET switches Q_4 and Q_5 are turned on by switch section S_{1b} during these tests.

FET switches Q_4 and Q_5 are turned off during the transfer function test. This disconnects A_7 from the output of the device under test and changes it from an integrator to a non-inverting unity gain amplifier driven from the triangular wave output of the function generator through the attenuator R_{33} and R_{34} and switch section S_{1a}. In this connection, amplifier A_7 serves two functions; first, to provide an offset voltage correction to the input of the device under test and, second, to drive the input of the device under test with a ±2.5 mV triangular wave centered about the offset voltage. During this test, the common mode driver amplifier is disabled by switch section S_{1a} and the vertical input of the measurement oscilloscope is transferred from the output of the integrator-buffer, A_7, to the output of the device under test by switch section S_{1d}. S_{2a} allows supply voltages for the device under test to be set at ±5, ±10, ±15, or ±20V. S_{2b} changes the vertical scale factor for the measurement oscilloscope to maintain optimum vertical deflection for the particular power supply voltage used. S_4 is a momentary contact pushbutton switch which is used to change the load on the device under test from 10kΩ to 2kΩ.

A delay must be provided when switching from the input tests to the transfer function tests. The purpose of this delay is to disable the integrator function of A_7 before driving it with the triangular wave. If this is not done, the offset correction voltage, stored on C_{16}, will be lost. This delay between opening FET switch Q_4, and switch Q_5, is provided by the RC filter, R_{35} and C_{19}.

Resistor R_{41} and diodes D_7 and D_8 are provided to control the integrator when no test device is present, or when a faulty test device is inserted. R_{41} provides a dc feedback path in the absence of a test device and resets the integrator to zero. Diodes D_7 and D_8 clamp the input to the integrator to approximately ±.7 volts when a faulty device is inserted.

FET switch Q_1 and resistor R_{28} provide a ground reference at the beginning of the 50-ohm-source, offset-voltage trace. This trace provides a ground reference which is independent of instrument or oscilloscope calibration. The gate of Q_1 is driven by the output of monostable multivibrator A_5, and shorts the vertical oscilloscope drive signal to ground during the time that A_5 output is positive.

Switch S_3, R_{27}, and R_{28} provide a 5X scale increase during input parameter tests to allow measurement of amplifiers with large offset voltage, offset current, or bias current.

Switch S_5 allows amplifier compensation to be changed for 101 or 709 type amplifiers.

CALIBRATION

Calibration of the test system is relatively simple and requires only two adjustments. First, the output of the main regulator is set up for 20V. Then, the triangular wave generator is adjusted to provide ±5V output by selecting R_{adj}. This sets the horizontal sweep for the X-Y oscilloscope used as the measurement system. The oscilloscope is then set up for 1V/division vertical and for a full 10 division horizontal sweep.

Scale factors for the three test positions are:

1. **Bias Current Display (Figure 2)**

I_{bias} total	100 nA/div. vertical
Common Mode Voltage	Variable horizontal

2. **Offset Voltage-Offset Current (Figure 3)**

I_{offset}	100 nA/div. vertical
V_{offset}	1 mV/div. vertical
Common Mode Voltage	Variable horizontal

3. **Transfer Function (Figure 5)**

V_{in}	0.5 mV/div.
V_{out}	5V/div. @ V_s ±20V 5V/div. @ V_s ±15V 2V/div. @ V_s ±10V 1V/div. @ V_s ± 5V

$$\text{Gain} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

CONSTRUCTION

Test set construction is simplified through the use of integrated circuits and etched circuit layout.

Figure 8 gives photographs of the completed tester. Figure 9 shows the parts location for the components on the circuit board layout of Figure 10. An attempt should be made to adhere to this layout to insure that parasitic coupling between elements will not cause oscillations or give calibration problems.

Table 1 is a listing of special components which are needed to fit the physical layout given for the tester.

TABLE 1. Partial Parts List

T_1	Triad F-90X
S_1	Centralab PA2003 non-shorting
S_2	Centralab PA2015 non-shorting
S_3, S_4	Grayhill 30-1 Series 30 subminiature pushbutton switch
S_5, S_6	Alcoswitch MST-105D SPDT

CONCLUSIONS

A semi-automatic test system has been described which will completely test the important operational amplifier parameters over the full power supply and common mode ranges. The system is simple, inexpensive, easily calibrated, and is equally suitable for engineering or quality assurance usage.

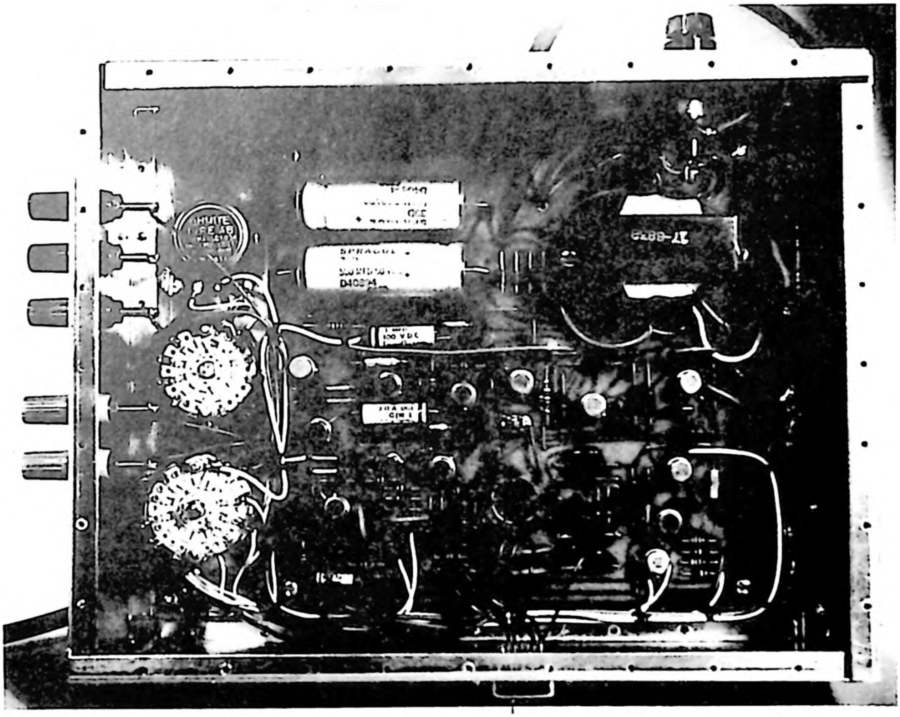


FIGURE 8a. Bottom of Test Set

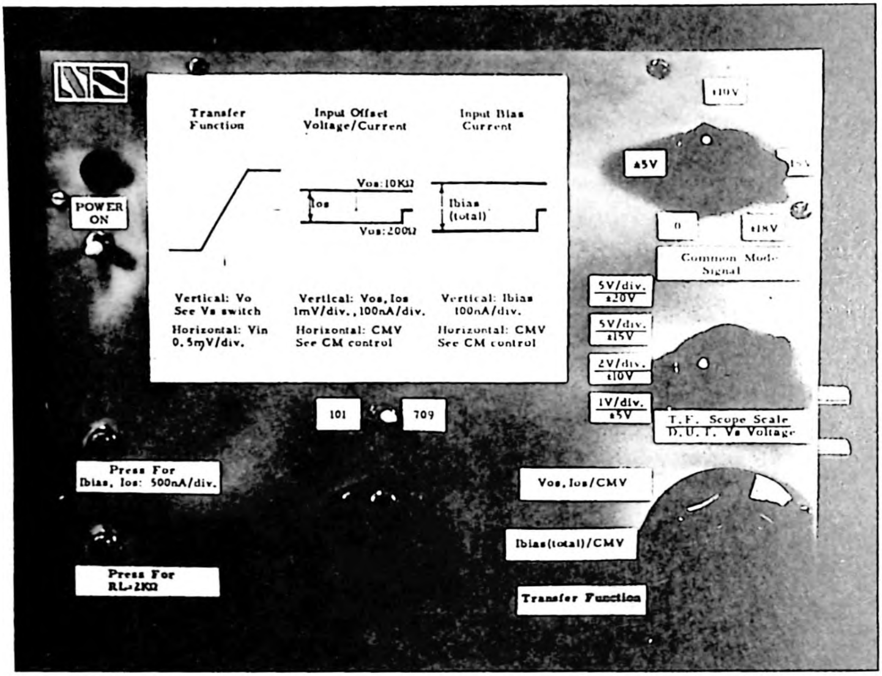

Transfer Function
Input Offset Voltage/Current
Input Bias Current
Vos:10KΩ
Ios
Vos:200Ω
Ibias (total)
Vertical: Vo See Vs switch
Horizontal: Vin 0.5mV/div.
Vertical: Vos, Ios 1mV/div., 100nA/div.
Horizontal: CMV See CM control
Vertical: Ibias 100nA/div.
Horizontal: CMV See CM control
POWER ON
±10V
±5V
±15V
0
±18V
Common Mode Signal
5V/div. ±20V
5V/div. ±15V
2V/div. ±10V
1V/div. ±5V
T.F. Scope Scale
D.U.T. Vs Voltage
101
709
Press For Ibias, Ios: 500nA/div.
Press For RL=2KΩ
Vos, Ios/CMV
Ibias(total)/CMV
Transfer Function

FIGURE 8b. Front Panel

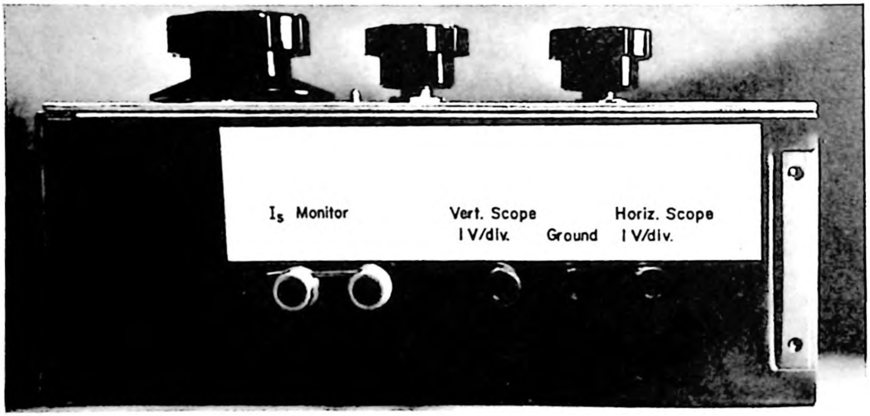

Is Monitor
Vert. Scope 1 V/div.
Ground
Horiz. Scope 1 V/div.

FIGURE 8c. Jacks

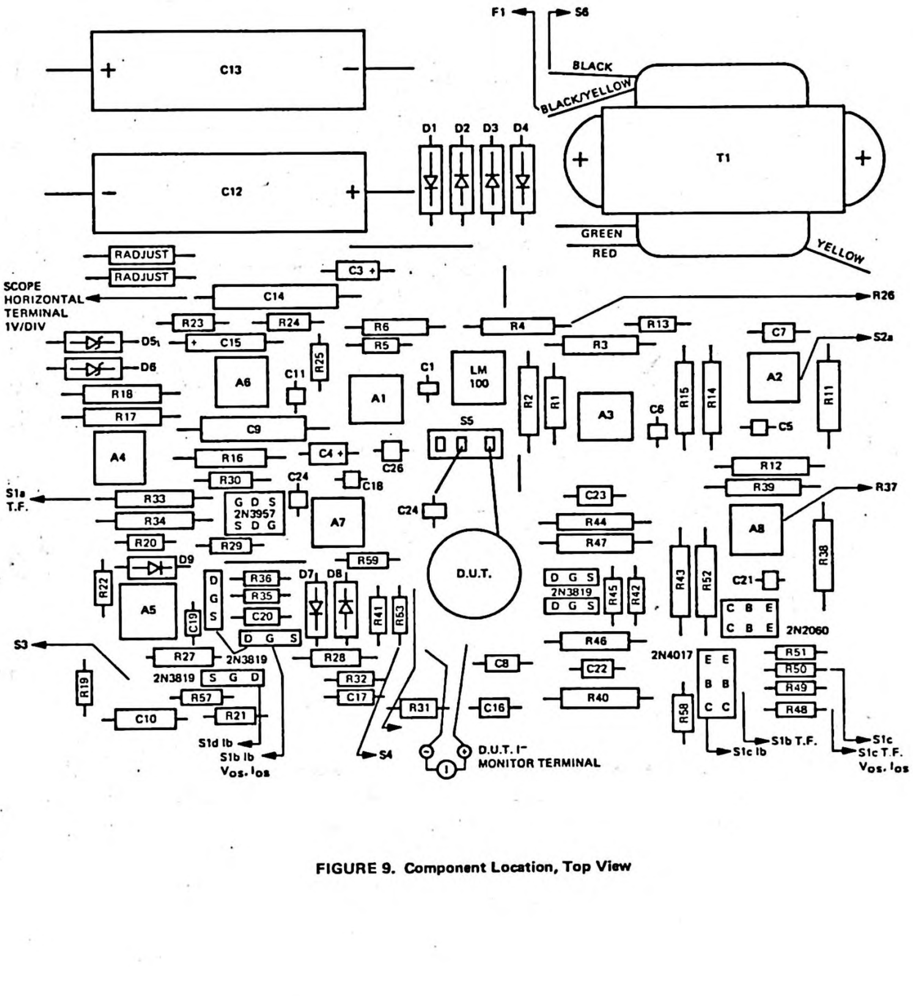

F1
S6
BLACK
BLACK/YELLOW
C13
C12
D1
D2
D3
D4
T1
GREEN
RED
YELLOW
RADJUST
RADJUST
C3
SCOPE HORIZONTAL TERMINAL 1V/DIV
C14
R26
R23
R24
R6
R4
R13
R5
R3
C7
S2a
D5
C15
D6
R25
C1
LM 100
A6
C11
A1
R2
R1
A3
C6
R15
R14
A2
R11
R18
R17
C9
C5
S5
A4
R16
C4
C26
R12
R30
C24
C18
R39
R37
S1a T.F.
R33
G D S
2N3957
S D G
A7
C24
C23
R34
R44
A8
R20
R29
R47
R38
R59
D9
D.U.T.
R22
A5
D G S
R36
D7
D8
D G S
2N3819
D G S
R45
R42
R43
R52
C21
R35
R41
R53
C B E
C B E
2N2060
C19
C20
S3
R27
2N3819
R28
R46
2N4017
R51
2N3819
S G D
R32
C8
C22
E E
B B
C C
R50
R49
R19
R57
C17
R31
C16
R40
R58
R48
C10
R21
S1d Ib
S1b Ib
Vos, Ios
S4
D.U.T. I– MONITOR TERMINAL
S1b T.F.
S1c Ib
S1c
S1c T.F.
Vos, Ios

FIGURE 9. Component Location, Top View

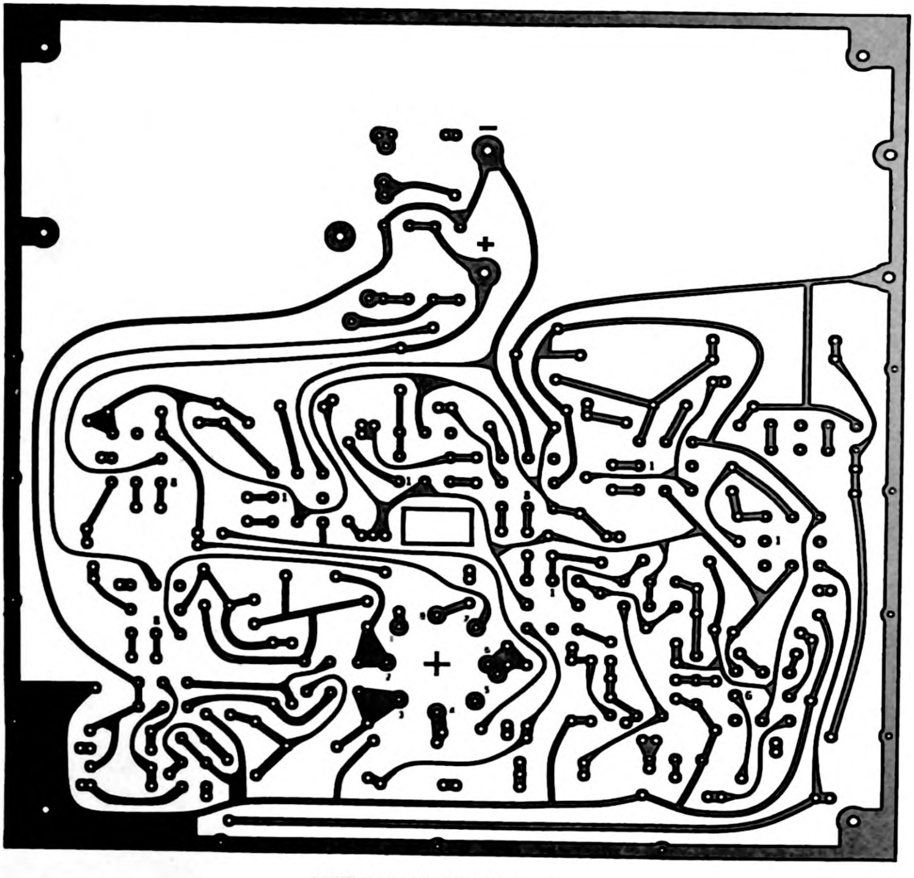

−
+
+
1
1
1
8
8
1
1
1
6
1
2
3
4
5
6
7
8

FIGURE 10. Circuit Board Layout

IC Op Amp Beats FETs on Input Current

National Semiconductor
Application Note 29
December 1969

ABSTRACT

A monolithic operational amplifier having input error currents in the order of 100 pA over a −55°C to 125°C temperature range is described. Instead of FETs, the circuit uses bipolar transistors with current gains of 5000 so that offset voltage and drift are not degraded. A power consumption of 1 mW at low voltage is also featured.

A number of novel circuits that make use of the low current characteristics of the amplifier are given. Further, special design techniques required to take advantage of these low currents are explored. Component selection and the treatment of printed circuit boards is also covered.

INTRODUCTION

A year ago, one of the loudest complaints heard about IC op amps was that their input currents were too high. This is no longer the case. Today ICs can provide the ultimate in performance for many applications—even surpassing FET amplifiers.

FET input stages have long been considered the best way to get low input currents in an op amp. Low-picoamp input currents can in fact be obtained at room temperature. However, this current, which is the leakage current of the gate junction, doubles every 10°C, so performance is severely degraded at high temperatures. Another disadvantage is that it is difficult to match FETs closely.[1] Unless expensive selection and trimming techniques are used, typical offset voltages of 50 mV and drifts of 50 μV/°C must be tolerated.

Super gain transistors[2] are now challenging FETs. These devices are standard bipolar transistors which have been diffused for extremely high current gains. Typically, current gains of 5000 can be obtained at 1 μA collector currents. This makes it possible to get input currents which are competitive with FETs. It is also possible to operate these transistors at zero collector base voltage, eliminating the leakage currents that plague the FET. Hence they can provide lower error currents at elevated temperatures. As a bonus, super gain transistors match much better than FETs with typical offset voltages of 1 mV and drifts of 3 μV/°C.

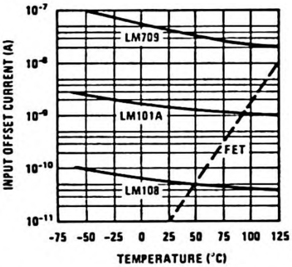


FIGURE 1. Comparing IC Op Amps With FET-Input Amplifier

Figure 1 compares the typical input offset currents of IC op amps and FET amplifiers. Although FETs give superior performance at room temperature, their advantage is rapidly lost as temperature increases. Still, they are clearly better than early IC amplifiers like the LM709.[3] Improved devices, like the LM101A,[4] equal FET performance over a −55°C to 125°C temperature range. Yet they use standard transistors in the input stage. Super gain transistors can provide more than an order of magnitude improvement over the LM101A. The LM108 uses these to equal FET performance over a 0°C to 70°C temperature range.

In applications involving 125°C operation, the LM108 is about two orders of magnitude better than FETs. In fact, unless special precautions are taken, overall circuit performance is often limited by leakages in capacitors, diodes, analog switches or printed circuit boards, rather than by the op amp itself.

EFFECTS OF ERROR CURRENT

In an operational amplifier, the input current produces a voltage drop across the source resis-

Reprinted from *EEE*, December 1969.

tance, causing a dc error. This effect can be minimized by operating the amplifier with equal resistances on the two inputs.[5] The error is then proportional to the difference in the two input currents, or the offset current. Since the current gains of monolithic transistors tend to match well, the offset current is typically a factor of ten less than the input currents.

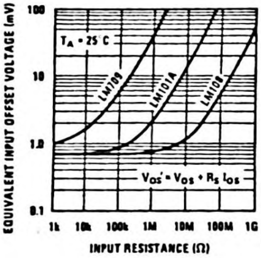


FIGURE 2. Illustrating The Effect Of Source Resistance On Typical Input Error Voltage

Naturally, error current has the greatest effect in high impedance circuitry. Figure 2 illustrates this point. The offset voltage of the LM709 is degraded significantly with source resistances greater than 10 kΩ. With the LM101A this is extended to source resistances high as 500 kΩ. The LM108, on the other hand, works well with source resistances above 10 MΩ.

High source resistances have an even greater effect on the drift of an amplifier, as shown in Figure 3. The performance of the LM709 is worsened with sources greater than 3 kΩ. The LM101A holds out to 100 kΩ sources, while the LM108 still works well at 3 MΩ.

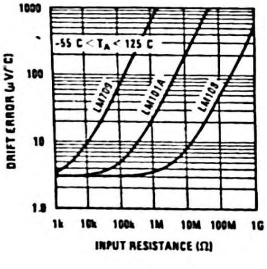


FIGURE 3. Degradation Of Typical Drift Characteristics With High Source Resistances

It is difficult to include FET amplifiers in Figure 3 because their drift is initially 50 μV/°C, unless they are selected and trimmed. Even though their drift may be well controlled (5 μV/°C) over a limited temperature range, trimmed amplifiers generally exhibit a much higher drift over a −55°C to 125°C temperature range. At any rate, their average drift rate would, at best, be like that of the LM101A where 125°C operation is involved.

Applications that require low error currents include amplifiers for photodiodes or capacitive transducers, as these usually operate at megohm impedance levels. Sample-and-hold circuits, timers, integrators and analog memories also benefit from low error currents. For example, with the LM709, worst case drift rates for these kinds of circuits is in the order of 1.5V/sec. The LM108 improves this to 3 mV/sec.—worst case over a −55°C to 125°C temperature range. Low input currents are also helpful in oscillators and active filters to get low frequency operation with reasonable capacitor values. The LM108 can be used at a frequency of 1 Hz with capacitors no larger than 0.01 μF. In logarithmic amplifiers, the dynamic range can be extended by nearly 60 dB by going from the LM709 to the LM108. In other applications, having low error currents often permits an entirely different design approach which can greatly simplify circuitry.

THE LM108

Figure 4 shows a simplified schematic of the LM108. Two kinds of NPN transistors are used on the IC chip: super gain (primary) transistors which have a current gain of 5000 with a breakdown voltage of 4V and conventional (secondary) transistors which have a current gain of 200 with an 80V breakdown. These are differentiated on the schematic by drawing the secondaries with a wider base.

Primary transistors (Q_1 and Q_2) are used for the input stage; and they are operated in a cascode connection with Q_5 and Q_6. The bases of Q_5 and Q_6 are bootstrapped to the emitters of Q_1 and Q_2 through Q_3 and Q_4, so that the input transistors are operated at zero collector-base voltage. Hence, circuit performance is not impaired by the low breakdown of the primaries, as the secondary transistors stand off the common mode voltage. This configuration also improves the common mode rejection since the input transistors do not see variations in the common mode voltage. Further, because there is no voltage across their collector-base junctions, leakage currents in the input transistors are effectively eliminated.

The second stage is a differential amplifier using high gain lateral PNPs (Q_9 and Q_{10}).[6] These devices have current gains of 150 and a breakdown voltage of 80V. R_1 and R_2 are the collector load resistors for the input stage. Q_7 and Q_8 are diode connected laterals which compensate for the

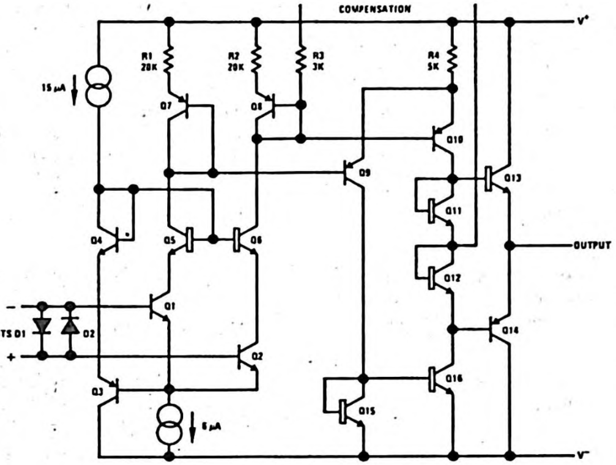


FIGURE 4. Simplified Schematic Of The LM108

emitter-base voltage of the second stage so that its operating current is set at twice that of the input stage by R_4.

The second stage uses an active collector load (Q_{15} and Q_{16}) to obtain high gain. It drives a complementary class-B output stage which gives a substantial load driving capability. The dead zone of the output stage is eliminated by biasing it on the verge of conduction with Q_{11} and Q_{12}.

Two methods of frequency compensation are available for the amplifier. In one a 30 pF capacitor is connected from the input to the output of the second stage (between the compensation terminals). This method is pin-compatible with the LM101 or LM101A. It can also be compensated by connecting a 100 pF capacitor from the output of the second stage to ground. This technique has the advantage of improving the high frequency power supply rejection by a factor of ten.

A complete schematic of the LM108 is given in the Appendix along with a description of the circuit. This includes such essential features as overload protection for the inputs and output.

PERFORMANCE

The primary design objective for the LM108 was to obtain very low input currents without sacrificing offset voltage or drift. A secondary objective was to reduce the power consumption. Speed was of little concern, as long as it was comparable with the LM709. This is logical as it is quite difficult to make high-impedance circuits fast; and low power circuits are very resistant to being made fast. In other respects, it was desirable to make the LM108 as much like the LM101A as possible.

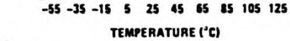


FIGURE 5. Input Currents

Figure 5 shows the input current characteristics of the LM108 over a −55°C to 125°C temperature range. Not only are the input currents low, but also they do not change radically over temperature. Hence, the device lends itself to relatively simple temperature compensation schemes, that will be described later.

There has been considerable discussion about using Darlington input stages rather than super gain transistors to obtain low input currents.[6,7] It is appropriate to make a few comments about that here.

Darlington inputs can give about the same input bias currents as super gain transistors—at room temperature. However, the bias current varies as the square of the transistor current gain. At low temperatures, super gain devices have a decided advantage. Additionally, the offset current of super gain transistors is considerably lower than Darlingtons, when measured as a percentage of bias current. Further, the offset voltage and offset voltage drift of Darlington transistors is both higher and more unpredictable.

Experience seems to tell the real truth about Darlingtons. Quite a few op amps with Darlington input stages have been introduced. However, none have become industry standards. The reason is that they are more sensitive to variations in the manufacturing process. Therefore, satisfactory performance specifications can only be obtained by sacrificing the manufacturing yield.

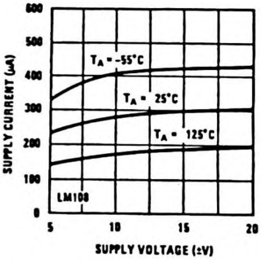


FIGURE 6. Supply Current

The supply current of the LM108 is plotted as a function of supply voltage in Figure 6. The operating current is about an order of magnitude lower than devices like the LM709. Furthermore, it does not vary radically with supply voltage which means that the device performance is maintained at low voltages and power consumption is held down at high voltages.

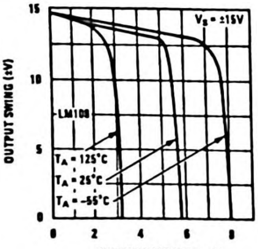


FIGURE 7. Output Swing

The output drive capability of the circuit is illustrated in Figure 7. The output swings to within a volt of the supplies, which is especially important when operating at low voltages. The output falls off rapidly as the current increases above a certain level and the short circuit protection goes into effect. The useful output drive is limited to about ±2 mA. It could have been increased by the addition of Darlington transistors on the output, but this would have restricted the voltage swing at low supply voltages. The amplifier, incidentally, works with common mode signals to within a volt of the supplies so it can be used with supply voltages as low as ±2V.

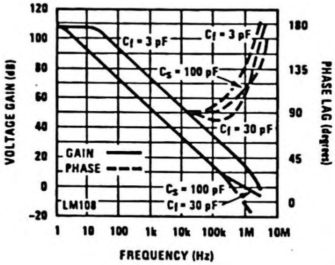
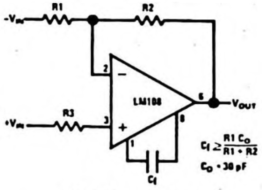
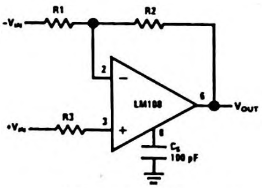


FIGURE 8. Open Loop Frequency Response

The open loop frequency response, plotted in Figure 8, indicates that the frequency response is about the same as that of the LM709 or the LM101A. Curves are given for the two compensa-



a. Standard Compensation Circuit



b. Alternate Compensation Circuit

FIGURE 9. Compensation Circuits

tion circuits shown in Figure 9. The standard compensation is identical to that of the LM101 or LM101A. The alternate compensation scheme gives much better rejection of high frequency power supply noise, as will be shown later.

With unity gain compensation, both methods give a 75-degree stability margin. However, the shunt compensation has a 300 kHz small signal bandwidth as opposed to 1 MHz for the other scheme. Because the compensation capacitor is not included on the IC chip, it can be tailored to fit the application. When the amplifier is used only at low frequencies, the compensation capacitor can be increased to give a greater stability margin. This makes the circuit less sensitive to capacitive loading, stray capacitances or improper supply bypassing. Overcompensation also reduces the high frequency noise output of the amplifier.

With closed-loop gains greater than one, the high frequency performance can be optimized by making the compensation capacitor smaller. If unity-gain compensation is used for an amplifier with a gain of ten, the gain error will exceed 1-percent at frequencies above 400 Hz. This can be extended to 4 kHz by reducing the compensation capacitor to 3 pF. The formula for determining the minimum capacitor value is given in Figure 9a. It should be noted that the capacitor value does not really depend on the closed-loop gain. Instead, it depends on the high frequency attenuation in the feedback networks and, therefore, the values of R_1 and R_2. When it is desirable to optimize performance at high frequencies, the standard compensation should be used. With small capacitor values, the stability margin obtained with shunt compensation is inadequate for conservative designs.

The frequency response of an operational amplifier is considerably different for large output signals than it is for small signals. This is indicated in Figure 10. With unity-gain compensation, the small signal bandwidth of the LM108 is 1 MHz. Yet full output swing cannot be obtained above 2 kHz. This corresponds to a slew rate of 0.3V/μs. Both the full-output bandwidth and the slew rate can be increased by using smaller compensation capacitors, as is indicated in the figure. However, this is only applicable for higher closed loop gains. The results plotted in Figure 10 are for standard compensations. With unity gain compensation, the same curves are obtained for the shunt compensation scheme.

Classical op amp theory establishes output resistance as an important design parameter. This is not true for IC op amps: The output resistance of most devices is low enough that it can be ignored, because they use class-B output stages. At low frequencies, thermal feedback between the output and input stages determines the effective output resistance, and this cannot be accounted for by conventional design theories. Semiconductor manufacturers take care of this by specifying the gain under full load conditions, which combines output resistance with gain as far as it affects overall circuit performance. This avoids the fictitious problem that can be created by an amplifier with infinite gain, which is good, that will cause the open loop output resistance to appear infinite, which is bad, although none of this affects overall performance significantly.

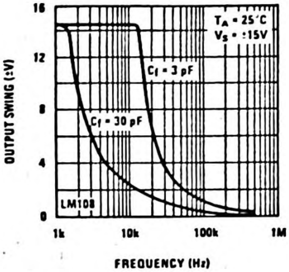


FIGURE 10. Large Signal Frequency Response

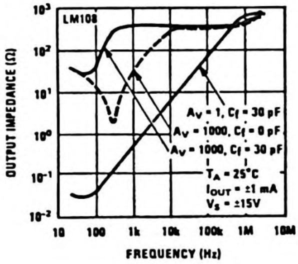


FIGURE 11. Closed Loop Output Impedance

The *closed loop* output impedance is, nonetheless, important in some applications. This is plotted for several operating conditions in Figure 11. It can be seen that the output impedance rises to about 500Ω at high frequencies. The increase occurs because the compensation capacitor rolls off the open loop gain. The output resistance can be reduced at the intermediate frequencies, for closed loop gains greater than one, by making the capacitor smaller. This is made apparent in the figure by comparing the output resistance with and without frequency compensation for a closed loop gain of 1000.

The output resistance also tends to increase at low frequencies. Thermal feedback is responsible for this phenomenon. The data for Figure 11 was taken under large-signal conditions with ±15V supplies, the output at zero and a ±1 mA current swing. Hence, the thermal feedback is accentuated more than would be the case for most applications.

In an op amp, it is desirable that performance be unaffected by variations in supply voltage. IC amplifiers are generally better than discretes in this respect because it is necessary for one single design to cover a wide range of uses. The LM108 has a power supply rejection which is typically in excess of 100 dB, and it will operate with supply voltages from ±2V to ±20V. Therefore, well-regulated supplies are unnecessary, for most applications, because a 20-percent variation has little effect on performance.

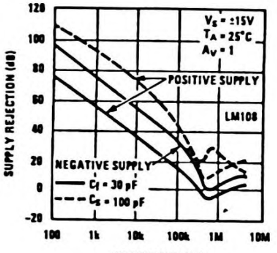


FIGURE 12. Power Supply Rejection

The story is different for high-frequency noise on the supplies, as is evident from Figure 12. Above 1 MHz, practically all the noise is fed through to the output. The figure also demonstrates that shunt compensation is about ten times better at rejecting high frequency noise than is standard compensation. This difference is even more pronounced with larger capacitor values. The shunt compensation has the added advantage that it makes the circuit virtually unaffected by the lack of supply bypassing.

Power supply rejection is defined as the ratio of the change in offset voltage to the change in the supply voltage producing it. Using this definition, the rejection at low frequencies is unaffected by the closed loop gain. However, at high frequencies, the opposite is true. The high frequency rejection is increased by the closed loop gain. Hence, an amplifier with a gain of ten will have an order of magnitude better rejection than that shown in Figure 12 in the vicinity of 100 kHz to 1 MHz.

The overall performance of the LM108 is summarized in Table 1*. It is apparent from the table and the previous discussion that the device is ideally suited for applications that require low input currents or reduced power consumption. The speed of the amplifier is not spectacular, but this is not usually a problem in high-impedance circuitry. Further, the reduced high frequency performance makes the amplifier easier to use in that less attention need be paid to capacitive loading, stray capacitances and supply bypassing.

APPLICATIONS

Because of its low input current, the LM108 opens up many new design possibilities. However, extra care must be taken in component selection and the assembly of printed circuit boards to take full advantage of its performance. Further, unusual design techniques must often be applied to get around the limitations of some components.

SAMPLE AND HOLD CIRCUITS

The holding accuracy of a sample and hold is directly related to the error currents in the components used. Therefore, it is a good circuit to start off with in explaining the problems involved. Figure 13 shows one configuration for a sample and hold. During the sample interval, Q_1 is turned on, charging the hold capacitor, C_1, up to the value of the input signal. When Q_1 is turned off, C_1 retains this voltage. The output is obtained from an op amp that buffers the capacitor so that it is not discharged by any loading. In the holding mode, an error is generated as the capacitor looses charge to supply circuit leakages. The accumulation rate for error is given by

$$\frac{dV}{dt} = \frac{I_E}{C_1},$$

where dV/dt is the time rate of change in output voltage and I_E is the sum of the input current to the op amp, the leakage current of the holding capacitor, board leakages and the "off" current of the FET switch.

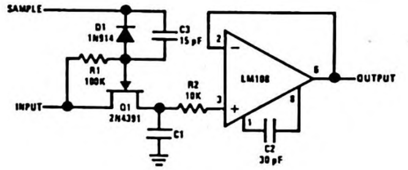


FIGURE 13. Sample And Hold Circuit

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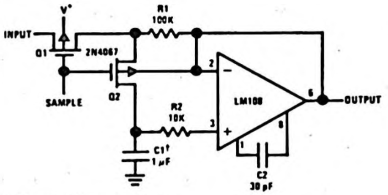
*See Appendix, page AN29-19.

When high-temperature operation is involved, the FET leakage can limit circuit performance. This can be minimized by using a junction FET, as indicated, because commercial junction FETs have lower leakage than their MOS counterparts. However, at 125°C even junction devices are a problem. Mechanical switches, such as reed relays, are quite satisfactory from the standpoint of leakage. However, they are often undesirable because they are sensitive to vibration, they are too slow or they require excessive drive power. If this is the case, the circuit in Figure 14 can be used to eliminate the FET leakage.



†Teflon, polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 3 mV/sec

FIGURE 14. Sample And Hold That Eliminates Leakage In FET Switches

When using P-channel MOS switches, the substrate must be connected to a voltage which is always more positive than the input signal. The source-to-substrate junction becomes forward biased if this is not done. The troublesome leakage current of a MOS device occurs across the substrate-to-drain junction. In Figure 14, this current is routed to the output of the buffer amplifier through R_1 so that it does not contribute to the error current.

The main sample switch is Q_1, while Q_2 isolates the hold capacitor from the leakage of Q_1. When the sample pulse is applied, both FETs turn on charging C_1 to the input voltage. Removing the pulse shuts off both FETs, and the output leakage of Q_1 goes through R_1 to the output. The voltage drop across R_1 is less than 10 mV, so the substrate of Q_2 can be bootstrapped to the output of the LM108. Therefore, the voltage across the substrate-drain junction is equal to the offset voltage of the amplifier. At this low voltage, the leakage of the FET is reduced by about two orders of magnitude.

It is necessary to use MOS switches when bootstrapping the leakages in this fashion. The gate leakage of a MOS device is still negligible at high temperatures; this is not the case with junction FETs. If the MOS transistors have protective diodes on the gates, special arrangements must be made to drive Q_2 so the diode does not become forward biased.

In selecting the hold capacitor, low leakage is not the only requirement. The capacitor must also be free of dielectric polarization phenomena.[8] This rules out such types as paper, mylar, electrolytic, tantalum or high-K ceramic. For small capacitor values, glass or silvered-mica capacitors are recommended. For the larger values, ones with teflon, polyethylene or polycarbonate dielectrics should be used.

The low input current of the LM108 gives a drift rate, in hold, of only 3 mV/sec when a 1 μF hold capacitor is used. And this number is worst case over the military temperature range. Even if this kind of performance is not needed, it may still be beneficial to use the LM108 to reduce the size of the hold capacitor. High quality capacitors in the larger sizes are bulky and expensive. Further, the switches must have a low "on" resistance and be driven from a low impedance source to charge large capacitors in a short period of time.

If the sample interval is less than about 100 μs, the LM108 may not be fast enough to work properly. If this is the case, it is advisable to substitute the LM102A,[9] which is a voltage follower designed for both low input current and high speed. It has a 30V/μs slew rate and will operate with sample intervals as short as 1 μs.

When the hold capacitor is larger than 0.05 μF, an isolation resistor should be included between the capacitor and the input of the amplifier (R_2 in Figure 14). This resistor insures that the IC will not be damaged by shorting the output or abruptly shutting down the supplies when the capacitor is charged. This precaution is not peculiar to the LM108 and should be observed on any IC op amp.

INTEGRATORS

Integrators are a lot like sample-and-hold circuits and have essentially the same design problems. In an integrator, a capacitor is used as a storage element; and the error accumulation rate is again proportional to the input current of the op amp.

Figure 15 shows a circuit that can compensate for the bias current of the amplifier. A current is fed into the summing node through R_1 to supply the bias current. The potentiometer, R_2, is adjusted so that this current exactly equals the bias current, reducing the drift rate to zero.

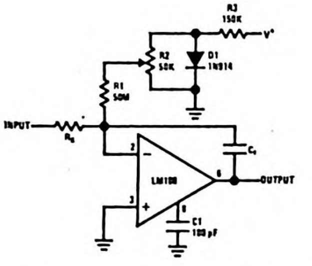
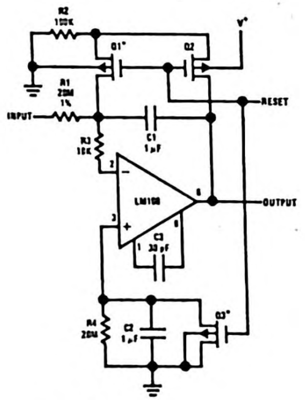


FIGURE 15. Integrator With Bias Current Compensation

The diode is used for two reasons. First, it acts as a regulator, making the compensation relatively insensitive to variations in supply voltage. Secondly, the temperature drift of diode voltage is approximately the same as the temperature drift of bias current. Therefore, the compensation is more effective if the temperature changes. Over a 0°C to 70°C temperature range, the compensation will give a factor of ten reduction in input current. Even better results are achieved if the temperature change is less.

Normally, it is necessary to reset an integrator to establish the initial conditions for integration. Resetting to zero is readily accomplished by shorting the integrating capacitor with a suitable switch. However, as with the sample and hold circuits, semiconductor switches can cause problems because of high-temperature leakage.

A connection that gets rid of switch leakages is shown in Figure 16. A negative-going reset pulse turns on Q_1 and Q_2, shorting the integrating capacitor. When the switches turn off, the leakage current of Q_2 is absorbed by R_2 while Q_1 isolates the output of Q_2 from the summing node. Q_1 has practically no voltage across its junctions because the substrate is grounded; hence, leakage currents are negligible.



*Q1 and Q3 should not have internal gate protection diodes.

FIGURE 16. Low Drift Integrator With Reset

The additional circuitry shown in Figure 16 makes the error accumulation rate proportional to the offset current, rather than the bias current. Hence, the drift is reduced by roughly a factor of 10. During the integration interval, the bias current of the non-inverting input accumulates an error across R_4 and C_2 just as the bias current on the inverting input does across R_1 and C_1. Therefore, if R_4 is matched with R_1 and C_2 is matched with C_1 (within about 5 percent) the output will drift at a rate proportional to the difference in these currents. At the end of the integration interval, Q_3 removes the compensating error accumulated on C_2 as the circuit is reset.

In applications involving large temperature changes, the circuit in Figure 16 gives better results than the compensation scheme in Figure 15—especially under worst case conditions. Over a −55°C to 125°C temperature range, the worst case drift is reduced from 3 mV/sec to 0.5 mV/sec when a 1 µF integrating capacitor is used. If this reduction in drift is not needed, the circuit can be simplified by eliminating R_4, C_2 and Q_3 and returning the non-inverting input of the amplifier directly to ground.

In fabricating low drift integrators, it is again necessary to use high quality components and minimize leakage currents in the wiring. The comments made on capacitors in connection with the sample-and-hold circuits also apply here. As an additional precaution, a resistor should be used to isolate the inverting input from the integrating capacitor if it is larger than 0.05 µF. This resistor prevents damage that might occur when the supplies are abruptly shut down while the integrating capacitor is charged.

Some integrator applications require both speed and low error current. The output amplifiers for photomultiplier tubes or solid-state radiation detectors are examples of this. Although the LM108 is relatively slow, there is a way to speed it up when it is used as an inverting amplifier. This is shown in Figure 17.

The circuit is arranged so that the high-frequency gain characteristics are determined by A_2, while A_1 determines the dc and low-frequency characteristics. The non-inverting input of A_1 is connected to the summing node through R_1. A_1 is operated as an integrator, going through unity gain at 500 Hz. Its output drives the non-inverting input.

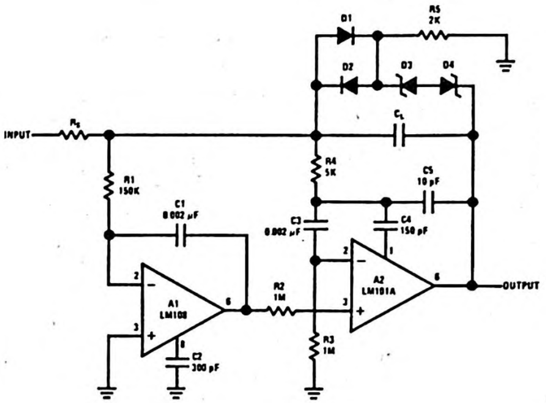


FIGURE 17. Fast Integrator

of A_2. The inverting input of A_2 is also connected to the summing node through C_3. C_3 and R_3 are chosen to roll off below 750 Hz. Hence, at frequencies above 750 Hz, the feedback path is directly around A_2, with A_1 contributing little. Below 500 Hz, however, the direct feedback path to A_2 rolls off; and the gain of A_1 is added to that of A_2.

The high frequency amplifier, A_2, is an LM101A connected with feed-forward compensation.[10] It has a 10 MHz equivalent small-signal bandwidth, a 10V/μs slew rate and a 250 kHz large-signal bandwidth, so these are the high-frequency characteristics of the complete amplifier. The bias current of A_2 is isolated from the summing node by C_3. Hence, it does not contribute to the dc drift of the integrator. The inverting input of A_1 is the only dc connection to the summing junction. Therefore, the error current of the composite amplifier is equal to the bias current of A_1.

If A_2 is allowed to saturate, A_1 will then start towards saturation. If the output of A_1 gets far off zero, recovery from saturation will be slowed drastically. This can be prevented by putting zener clamp diodes across the integrating capacitor. A suitable clamping arrangement is shown in Figure 17. D_1 and D_2 are included in the clamp circuit along with R_5 to keep the leakage currents of the zeners from introducing errors.

In addition to increasing speed, this circuit has other advantages. For one, it has the increased output drive capability of the LM101A. Further, thermal feedback is virtually eliminated because the LM108 does not see load variations. Lastly, the open loop gain is nearly infinite at low frequencies as it is the product of the gains of the two amplifiers.

SINE WAVE OSCILLATOR

Although it is comparatively easy to build an oscillator that approximates a sine wave, making one that delivers a high-purity sinusoid with a stable frequency and amplitude is another story. Most satisfactory designs are relatively complicated and require individual trimming and temperature compensation to make them work. In addition, they generally take a long time to stabilize to the final output amplitude.

A unique solution to most of these problems is shown in Figure 18. A_1 is connected as a two-pole low-pass active filter, and A_2 is connected as an integrator. Since the ultimate phase lag introduced by the amplifiers is 270 degrees, the circuit can be made to oscillate if the loop gain is high enough at the frequency where the lag is 180 degrees. The gain is actually made somewhat higher than is required for oscillation to insure starting. Therefore, the amplitude builds up until it is limited by some nonlinearity in the system.

Amplitude stabilization is accomplished with zener clamp diodes, D_1 and D_2. This does introduce distortion, but it is reduced by the subsequent low pass filters. If D_1 and D_2 have equal breakdown voltages, the resulting symmetrical clipping will

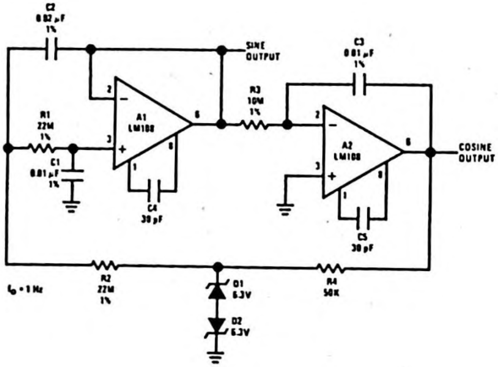


FIGURE 18. Sine Wave Oscillator

virtually eliminate the even-order harmonics. The dominant harmonic is then the third, and this is about 40 dB down at the output of A_1 and about 50 dB down on the output of A_2. This means that the total harmonic distortion on the two outputs is 1 percent and 0.3 percent, respectively.

The frequency of oscillation and the oscillation threshold are determined by R_1, R_2, R_3, C_1, C_2 and C_3. Therefore precision components with low temperature coefficients should be used. If R_3 is made lower than shown, the circuit will accept looser component tolerances before dropping out of oscillation. The start up will also be quicker. However, the price paid is that distortion is increased. The value of R_4 is not critical, but it should be made much smaller than R_2 so that the effective resistance at R_2 does not drop when the clamp diodes conduct.

The output amplitude is determined by the breakdown voltages of D_1 and D_2. Therefore, the clamp level should be temperature compensated for stable operation. Diode-connected (collector shorted to base) NPN transistors with an emitter-base breakdown of about 6.3V work well, as the positive temperature coefficient of the diode in reverse breakdown nearly cancels the negative temperature coefficient of the forward-biased diode. Added advantages of using transistors are that they have less shunt capacitance and sharper breakdowns than conventional zeners.

The LM108 is particularly useful in this circuit at low frequencies, since it permits the use of small capacitors. The circuit shown oscillates at 1 Hz, but uses capacitors in the order of 0.01 μF. This makes it much easier to find temperature-stable precision capacitors. However, some judgment must be used as large value resistors with low temperature coefficients are not exactly easy to come by.*

The LM108s are useful in this circuit for output frequencies up to 1 kHz. Beyond that, better performance can be realized by substituting an LM102A for A_1 and an LM101A with feedforward compensation for A_2. The improved high-frequency response of these devices extends the operating frequency out to 100 kHz.

CAPACITANCE MULTIPLIER

Large capacitor values can be eliminated from most systems just by raising the impedance levels, if suitable op amps are available. However, sometimes it is not possible because the impedance levels are already fixed by some element of the system like a low impedance transducer. If this is the case, a capacitance multiplier can be used to increase the effective capacitance of a small capacitor and couple it into a low impedance system.

Previously, IC op amps could not be used effectively as capacitance multipliers because the equivalent leakages generated due to offset current were significantly greater than the leakages of large tantalum capacitors. With the LM108, this has changed. The circuit shown in Figure 19 generates an equivalent capacitance of 100,000 μF with a worst case leakage of 8 μA—over a −55°C to 125°C temperature range.

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*Large-value resistors are available from Victoreen Instrument, Cleveland, Ohio and Pyrofilm Resistor Co., Whippany, New Jersey.

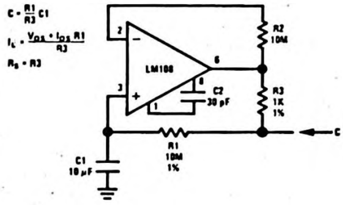


FIGURE 19. Capacitance Multiplier

The performance of the circuit is described by the equations given in Figure 19, where C is the effective output capacitance, I_L is the leakage current of this capacitance and R_s is the series resistance of the multiplied capacitance. The series resistance is relatively high, so high-Q capacitors cannot be realized. Hence, such applications as tuned circuits and filters are ruled out. However, the multiplier can still be used in timing circuits or servo compensation networks where some resistance is usually connected in series with the capacitor or the effect of the resistance can be compensated for.

One final point is that the leakage current of the multiplied capacitance is not a function of the applied voltage. It persists even with no voltage on the output. Therefore, it can generate offset errors in a circuit, rather than the scaling errors caused by conventional capacitors.

INSTRUMENTATION AMPLIFIER

In many instrumentation applications there is frequently a need for an amplifier with a high-impedance differential input and a single ended output. Obvious uses for this are amplifiers for bridge-type signal sources such as strain gages, temperature sensors or pressure transducers. General purpose op amps have satisfactory input characteristics, but feedback must be added to determine the effective gain. And the addition of feedback can drastically reduce the input resistance and degrade common mode rejection.

Figure 20 shows the classical op amp circuit for a differential amplifier. This circuit has three main disadvantages. First, the input resistance on the inverting input is relatively low, being equal to R_1. Second, there usually is a large difference in the input resistance of the two inputs, as is indicated by the equations on the schematic. Third, the common mode rejection is greatly affected by resistor matching and by balancing of the source resistances. A 1-percent deviation in any one of the resistor values reduces the common mode rejection to 46 dB for a closed loop gain of 1, to 60 dB for a gain of 10 and to 80 dB for a gain of 100.

Clearly, the only way to get high input impedance is to use very large resistors in the feedback network. The op amp must operate from a source resistance which is orders of magnitude larger than the resistance of the signal source. Older IC op amps introduced excessive offset and drift when operating from higher resistances and could not be used successfully. The LM108, however, is relatively unaffected by the large resistors, so this approach can sometimes be employed.

With large input resistors, the feedback resistors, R_3 and R_4, can get quite large for higher closed loop gains. For example, if R_1 and R_2 are 1 MΩ, R_3 and R_4 must be 100 MΩ for a gain of 100. It is difficult to accurately match resistors that are this high in value, so common mode rejection may suffer. Nonetheless, any one of the resistors can be trimmed to take out common mode feedthrough caused either by resistor mismatches or the amplifier itself.

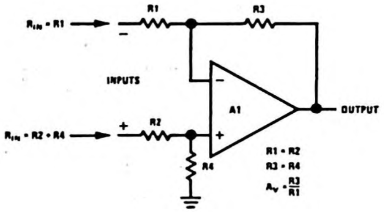


FIGURE 20. Feedback Connection For a Differential Amplifier

Another problem caused by large feedback resistors is that stray capacitance can seriously affect the high frequency common mode rejection. With 1 MΩ input resistors, a 1 pF mismatch in stray capacitance from either input to ground can drop the common mode rejection to 40 dB at 1500 Hz. The high frequency rejection can be improved at the expense of frequency response by shunting R_3 and R_4 with matched capacitors.

With high impedance bridges, the feedback resistances become prohibitively large even for the LM108, so the circuit in Figure 20 cannot be used. One possible alternative is shown in Figure 21. R_2 and R_3 are chosen so that their equivalent parallel resistance is equal to R_1. Hence, the output of the amplifier will be zero when the bridge is balanced.

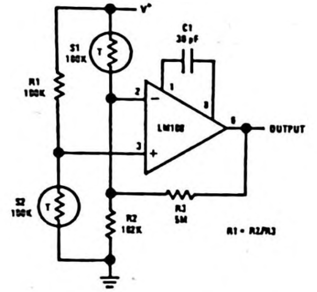


FIGURE 21. Amplifier For Bridge Transducers

When the bridge goes off balance, the op amp maintains the voltage between its input terminals at zero with current fed back from the output through R_3. This circuit does not act like a true differential amplifier for large imbalances in the bridge. The voltage drops across the two sensor resistors, S_1 and S_2, become unequal as the bridge goes off balance, causing some non-linearity in the transfer function. However, this is not usually objectionable for small signal swings.

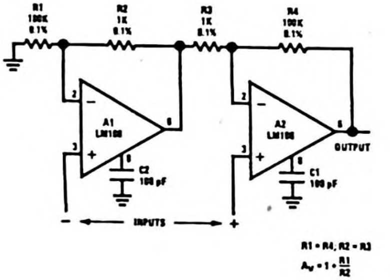


FIGURE 22. Differential Input Instrumentation Amplifier

Figure 22 shows a true differential connection that has few of the problems mentioned previously. It has an input resistance greater than $10^{10}\Omega$, yet it does not need large resistors in the feedback circuitry. With the component values shown, A_1 is connected as a non-inverting amplifier with a gain of 1.01; and it feeds into A_2 which has an inverting gain of 100. Hence, the total gain from the input of A_1 to the output of A_2 is 101, which is equal to the non-inverting gain of A_2. If all the resistors are matched, the circuit responds only to the differential input signal—not the common mode voltage.

This circuit has the same sensitivity to resistor matching as the previous circuits, with a 1 percent mismatch between two resistors lowering the common mode rejection to 80 dB. However, matching is more easily accomplished because of the lower resistor values. Further, the high frequency common mode rejection is less affected by stray capacitances. The high frequency rejection is limited, though, by the response of A_1.

LOGARITHMIC CONVERTER

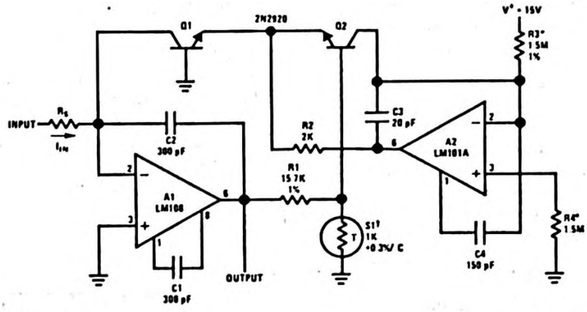
A logarithmic amplifier is another circuit that can take advantage of the low input current of an op amp to increase dynamic range. Most practical log converters make use of the logarithmic relationship between the emitter-base voltage of standard double-diffused transistors and their collector current. This logarithmic characteristic has been proven true for over 9 decades of collector current. The only problem involved in using transistors as logging elements is that the scale factor has a temperature sensitivity of 0.3 percent/°C. However, temperature compensating resistors have been developed to compensate for this characteristic, making possible log converters that are accurate over a wide temperature range.

Figure 23 gives a circuit that uses these techniques. Q_1 is the logging transistor, while Q_2 provides a fixed offset to temperature compensate the emitter-base turn on voltage of Q_1. Q_2 is operated at a fixed collector current of 10 μA by A_2, and its emitter-base voltage is subtracted from that of Q_1 in determining the output voltage of the circuit. The collector current of Q_2 is established by R_3 and V^+ through A_2.

The collector current of Q_1 is proportional to the input current through R_s and, therefore, proportional to the input voltage. The emitter-base voltage of Q_1 varies as the log of the input voltage. The fixed emitter-base voltage of Q_2 subtracts from the voltage on the emitter of Q_1 in determining the voltage on the top end of the temperature-compensating resistor, S_1.

The signal on the top of S_1 will be zero when the input current is equal to the current through R_3 at any temperature. Further, this voltage will vary logarithmically for changes in input current, although the scale factor will have a temperature coefficient of −0.3%/°C. The output of the converter is essentially multiplied by the ratio of R_1 to S_1. Since S_1 has a positive temperature coefficient of 0.3 percent/°C, it compensates for the change in scale factor with temperature.

In this circuit, an LM101A with feedforward compensation is used for A_2 since it is much faster than the LM108 used for A_1. Since both amplifiers are cascaded in the overall feedback loop, the reduced phase shift through A_2 insures stability.



10 nA < I_{IN} < 1 mA
Sensitivity is 1V per decade.

†Available from Tel Labs, Inc., Manchester, N.H., Type Q81.

*Determines current for zero crossing on output: 10 μA as shown.

FIGURE 23. Temperature Compensated One-Quadrant Logarithmic Converter

Certain things must be considered in designing this circuit. For one, the sensitivity can be changed by varying R_1. But R_1 must be made considerably larger than the resistance of S_1 for effective temperature compensation of the scale factor. Q_1 and Q_2 should also be matched devices in the same package, and S_1 should be at the same temperature as these transistors. Accuracy for low input currents is determined by the error caused by the bias current of A_1. At high currents, the behavior of Q_1 and Q_2 limits accuracy. For input currents approaching 1 mA, the 2N2920 develops logging errors in excess of 1 percent. If larger input currents are anticipated, bigger transistors must be used; and R_2 should be reduced to insure that A_2 does not saturate.

TRANSDUCER AMPLIFIERS

With certain transducers, accuracy depends on the choice of the circuit configuration as much as it does on the quality of the components. The amplifier for photodiode sensors, shown in Figure 24, illustrates this point. Normally, photodiodes are operated with reverse voltage across the junction. At high temperatures, the leakage currents can approach the signal current. However, photodiodes deliver a short-circuit output current, unaffected by leakage currents, which is not significantly lower than the output current with reverse bias.

The circuit shown in Figure 24 responds to the short-circuit output current of the photodiode. Since the voltage across the diode is only the offset voltage of the amplifier, inherent leakage is reduced by at least two orders of magnitude. Neglecting the offset current of the amplifier, the output current of the sensor is multiplied by R_1 plus R_2 in determining the output voltage.

Figure 25 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The LM108 can provide input resistances in the range of 10 to 100 MΩ, using conventional circuitry. However, conventional designs are sometimes ruled out either because

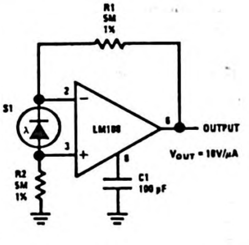


FIGURE 24. Amplifier For Photodiode Sensor

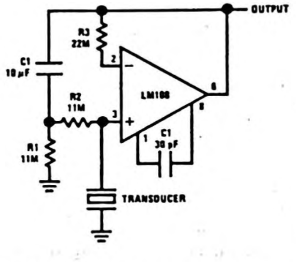


FIGURE 25. Amplifier For Piezoelectric Transducers

large resistors cannot be used or because prohibitively large input resistances are needed.

Using the circuit in Figure 25, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency of a capacitive transducer is determined more by the RC product of R_1 and C_1 than it is by resistor values and the equivalent capacitance of the transducer.

RESISTANCE MULTIPLICATION

When an inverting operational amplifier must have high input resistance, the resistor values required can get out of hand. For example, if a 2 MΩ input resistance is needed for an amplifier with a gain of 100, a 200 MΩ feedback resistor is called for. This resistance can, however, be reduced using the circuit in Figure 26. A divider with a ratio of 100 to 1 (R_3 and R_4) is added to the output of the amplifier: Unity-gain feedback is applied from the output of the divider, giving an overall gain of 100 using only 2 MΩ resistors.

This circuit does increase the offset voltage somewhat. The output offset voltage is given by

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_2}\right) A_V V_{os}.$$

The offset voltage is only multiplied by $A_V + 1$ in a conventional inverter. Therefore, the circuit in Figure 26 multiplies the offset by 200, instead of 101. This multiplication factor can be reduced to 110 by increasing R_2 to 20 MΩ and R_3 to 5.55k.

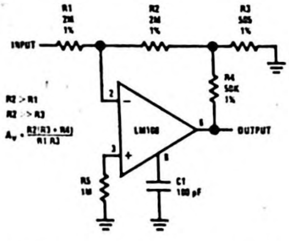


FIGURE 26. Inverting Amplifier With High Input Resistance

Another disadvantage of the circuit is that four resistors determine the gain, instead of two. Hence, for a given resistor tolerance, the worst-case gain deviation is greater, although this is probably more than offset by the ease of getting better tolerances in the low resistor values.

CURRENT SOURCES

Although there are numerous ways to make current sources with op amps, most have limitations as far as their application is concerned. Figure 27, however, shows a current source which is fairly flexible and has few restrictions as far as its use is concerned. It supplies a current that is proportional to the input voltage and drives a load referred to ground or any voltage within the output-swing capability of the amplifier.

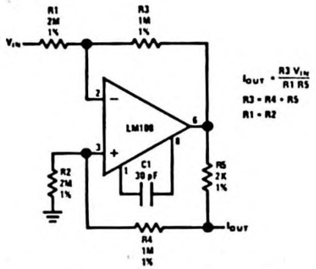


FIGURE 27. Bilateral Current Source

With the output grounded, it is relatively obvious that the output current will be determined by R_5 and the gain setting of the op amp, yielding

$$I_{OUT} = -\frac{R_3 V_{IN}}{R_1 R_5}.$$

When the output is not at zero, it would seem that the current through R_2 and R_4 would reduce accuracy. Nonetheless, if $R_1 = R_2$ and $R_3 = R_4 + R_5$, the output current will be independent of the output voltage. For $R_1 + R_3 >> R_5$, the output resistance of the circuit is given by

$$R_{OUT} \cong R_5 \left(\frac{R}{\Delta R}\right)$$

where R is any one of the feedback resistors (R_1, R_2, R_3 or R_4) and ΔR is the incremental change in the resistor value from design center. Hence, for the circuit in Figure 27, a 1 percent deviation in one of the resistor values will drop the output resistance of 200 kΩ. Such errors can be trimmed out by adjusting one of the feedback resistors. In design, it is advisable to make the feedback resistors as large as possible. Otherwise, resistor tolerances become even more critical.

The circuit must be driven from a source resistance which is low by comparison to R_1, since this resistance will imbalance the circuit and affect both gain and output resistance. As shown, the circuit gives a negative output current for a positive input voltage. This can be reversed by grounding the input and driving the ground end of R_2. The magnitude of the scale factor will be unchanged as long as $R_4 >> R_5$.

VOLTAGE COMPARATORS

Like most op amps, it is possible to use the LM108 as a voltage comparator. Figure 28 shows the device used as a simple zero-crossing detector. The inputs of the IC are protected internally by back-to-back diodes connected between them, therefore, voltages in excess of 1V cannot be impressed directly across the inputs. This problem is taken care of by R_1 which limits the current so that input voltages in excess of 1 kV can be tolerated. If absolute accuracy is required or if R_1 is made much larger than 1 MΩ, a compensating resistor of equal value should be inserted in series with the other input.

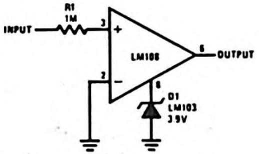


FIGURE 28. Zero Crossing Detector

In Figure 28, the output of the op amp is clamped so that it can drive DTL or TTL directly. This is accomplished with a clamp diode on pin 8. When the output swings positive, it is clamped at the breakdown voltage of the zener. When it swings negative, it is clamped at a diode drop below ground. If the 5V logic supply is used as a positive supply for the amplifier, the zener can be replaced with an ordinary silicon diode. The maximum fan out that can be handled by the device is one for standard DTL or TTL under worst case conditions.

As might be expected, the LM108 is not very fast when used as a comparator. The response time is up in the tens of microseconds. An LM103[11] is recommended for D_1, rather than a conventional alloy zener, because it has lower capacitance and will not slow the circuit further. The sharp breakdown of the LM103 at low currents is also an advantage as the current through the diode in clamp is only 10 µA.

Figure 29 shows a comparator for voltages of opposite polarity. The output changes state when the voltage on the junction of R_1 and R_2 is equal to V_{TH}. Mathematically, this is expressed by

$$V_{TH} = V_2 + \frac{R_2 \, (V_1 - V_2)}{R_1 + R_2}.$$

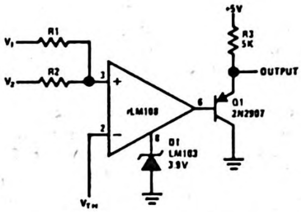


FIGURE 29. Voltage Comparator With Output Buffer

The LM108 can also be used as a differential comparator, going through a transition when two input voltages are equal. However, resistors must be inserted in series with the inputs to limit current and minimize loading on the signal sources when the input-protection diodes conduct. Figure 29 also shows how a PNP transistor can be added on the output to increase the fan out to about 20 with standard DTL or TTL.

POWER BOOSTER

The LM108, which was designed for low power consumption, is not able to drive heavy loads. However, a relatively simple booster can be added to the output to increase the output current to ±50 mA. This circuit, shown in Figure 30, has the added advantage that it swings the output up to the supplies, within a fraction of a volt. The increased voltage swing is particularly helpful in low voltage circuits.

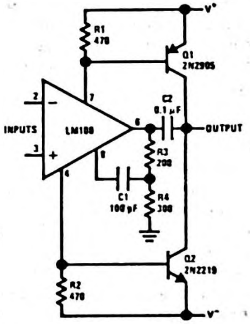


FIGURE 30. Power Booster

In Figure 30, the output transistors are driven from the supply leads of the op amp. It is important that R_1 and R_2 be made low enough so Q_1 and Q_2 are not turned on by the *worst case* quiescent current of the amplifier. The output of the op amp is loaded heavily to ground with R_3 and R_4.

When the output swings about 0.5V positive, the increasing positive supply current will turn on Q_1 which pulls up the load. A similar situation occurs with Q_2 for negative output swings.

The bootstrapped shunt compensation shown in the figure is the only one that seems to work for all loading conditions. This capacitor, C_1, can be made inversely proportional to the closed loop gain to optimize frequency response. The value given is for a unity-gain follower connection. C_2 is also required for loop stability.

The circuit does have a dead zone in the open loop transfer characteristic. However, the low frequency gain is high enough so that it can be neglected. Around 1 kHz, though, the dead zone becomes quite noticeable.

Current limiting can be incorporated into the circuit by adding resistors in series with the emitters of Q_1 and Q_2 because the short circuit protection of the LM108 limits the maximum voltage drop across R_1 and R_2.

BOARD CONSTRUCTION

As indicated previously, certain precautions must be observed when building circuits that are sensitive to very low currents. If proper care is not taken, board leakage currents can easily become much larger than the error currents of the op amp. To prevent this, it is necessary to thoroughly clean printed circuit boards. Even experimental breadboards must be cleaned with trichloroethlene or alcohol to remove solder fluxes, and blown dry with compressed air. These fluxes may be insulators at low impedance levels—like in electric motors—but they certainly are not in high impedance circuits. In addition to causing gross errors, their presence can make the circuit behave erratically, especially as the temperature is changed.

At elevated temperatures, even the leakage of clean boards can be a headache. At 125°C the leakage resistance between adjacent runs on a printed circuit board is about $10^{11}\Omega$ (0.05-inch separation parallel for 1 inch) for high quality epoxy-glass boards that have been properly cleaned. Therefore, the boards can easily produce error currents in the order of 200 pA and much more if they become contaminated. Conservative practice dictates that the boards be coated with epoxy or silicone rubber after cleaning to prevent contamination. Silicone rubber is the easiest to use. However, if the better durability of epoxy is needed, care must be taken to make sure that it gets thoroughly cured. Otherwise, the epoxy will make high temperature leakage much worse.

Care must also be exercised to insure that the circuit board is protected from condensed water vapor when operating in the vicinity of 0°C. This can usually be accomplished by coating the board as mentioned above.

GUARDING

Even with properly cleaned and coated boards, leakage currents are on the verge of causing trouble at 125°C. The standard pin configuration of most IC op amps has the input pins adjacent to pins which are at the supply potentials. Therefore, it is advisable to employ guarding to reduce the voltage difference between the inputs and adjacent metal runs.

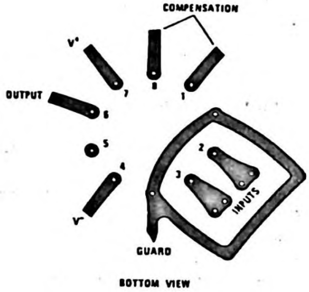
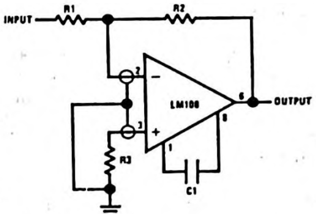


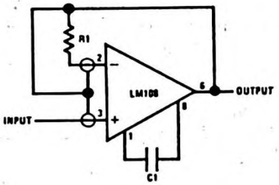
FIGURE 31. Printed Circuit Layout For Input Guarding With TO-5 Package

A board layout that includes input guarding is shown in Figure 31 for the eight lead TO-5 package. A ten-lead pin circle is used, and the leads of the IC are formed so that the holes adjacent to the inputs are vacant when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is then connected to a low impedance point that is at the same potential as the inputs. The leakage currents from the pins at the supply potentials are absorbed by the guard. The voltage difference between the guard and the inputs can be made approximately equal to the offset voltage, reducing the effective leakage by more than three orders of magnitude. If the leads of the integrated circuit, or other components connected to the input, go through the board, it may be necessary to guard both sides.

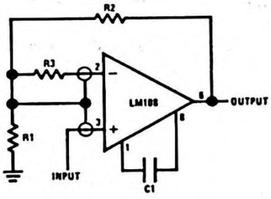
Figure 32 shows how the guard is committed on the more-common op amp circuits. With an integrator or inverting amplifier, where the inputs are close to ground potential, the guard is simply grounded. With the voltage follower, the guard is bootstrapped to the output. If it is desirable to put a resistor in the inverting input to compensate for the source resistance, it is connected as shown in Figure 32b.


INPUT
R1
R2
2
−
LM108
6
OUTPUT
3
+
8
1
R3
C1

a. Inverting Amplifier


R1
2
−
LM108
6
OUTPUT
INPUT
3
+
8
1
C1

b. Follower


R2
R3
2
−
LM108
6
OUTPUT
3
+
8
R1
1
INPUT
C1

c. Non-Inverting Amplifier

FIGURE 32. Connection Of Input Guards

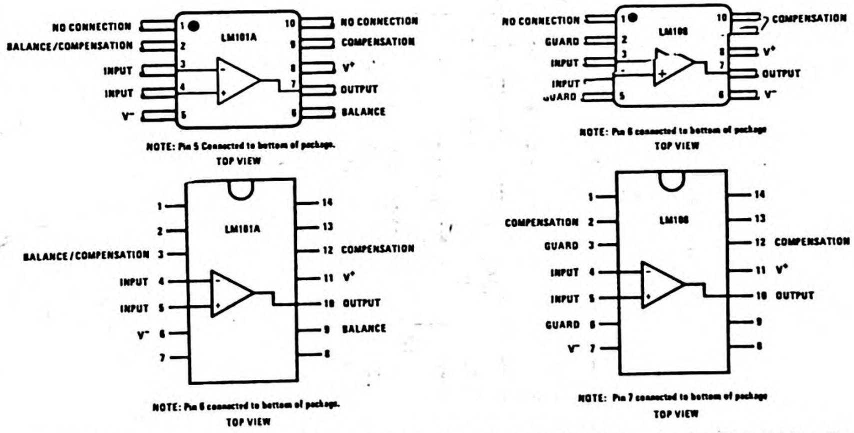
Guarding a non-inverting amplifier is a little more complicated. A low impedance point must be created by using relatively low value feedback resistors to determine the gain (R_1 and R_2 in Figure 32c). The guard is then connected to the junction of the feedback resistors. A resistor, R_3, can be connected as shown in the figure to compensate for large source resistances.

With the dual-in-line and flat packages, it is far more difficult to guard the inputs, if the standard pin configuration of the LM709 or LM101A is used, because the pin spacings on these packages are fixed. Therefore, the pin configuration of the LM108 was changed, as shown in Figure 33.

CONCLUSIONS

IC op amps are now available that equal the input current specifications of FET amplifiers in all but the most restricted temperature range applications. At operating temperatures above 85°C, the IC is clearly superior as it uses bipolar transistors that make it possible to eliminate the leakage currents that plague FETs. Additionally, bipolar transistors match better than FETs, so low offset voltage and drifts can be obtained without expensive adjustments or selection. Further, the bipolar devices lend themselves more readily to low-cost monolithic construction.

These amplifiers open up new application areas and vastly improve performance in others. For example, in analog memories, holding intervals can be extended to minutes, even where −55°C to 125°C operation is involved. Instrumentation amplifiers and low frequency waveform generators also benefit from the low error currents.


NO CONNECTION
BALANCE/COMPENSATION
INPUT
INPUT
V−
LM101A
1
2
3
4
5
10
9
8
7
6
NO CONNECTION
COMPENSATION
V+
OUTPUT
BALANCE
NO CONNECTION
GUARD
INPUT
INPUT
GUARD
LM108
1
2
3
4
5
10
9
8
7
6
COMPENSATION
V+
OUTPUT
V−
1
2
BALANCE/COMPENSATION 3
INPUT 4
INPUT 5
V− 6
7
LM101A
14
13
12 COMPENSATION
11 V+
10 OUTPUT
9 BALANCE
8
1
COMPENSATION 2
GUARD 3
INPUT 4
INPUT 5
GUARD 6
V− 7
LM108
14
13
12 COMPENSATION
11 V+
10 OUTPUT
9
8

NOTE: Pin 5 Connected to bottom of package.
TOP VIEW

NOTE: Pin 5 connected to bottom of package
TOP VIEW

NOTE: Pin 6 connected to bottom of package.
TOP VIEW

NOTE: Pin 7 connected to bottom of package
TOP VIEW

FIGURE 33. Comparing Connection Diagrams Of The LM101A And LM108, Showing Addition Of Guarding

When operating above 85°C, overall performance is frequently limited by components other than the op amp, unless certain precautions are observed. It is generally necessary to redesign circuits using semiconductor switches to reduce the effect of their leakage currents. Further, high quality capacitors must be used, and care must be exercised in selecting large value resistors. Printed circuit board leakages can also be troublesome unless the boards are properly treated. And above 100°C, it is almost mandatory to employ guarding on the boards to protect the inputs, if the full potential of the amplifier is to be realized.

APPENDIX

A complete schematic of the LM108 is given in Figure A1. A description of the basic circuit is presented along with a simplified schematic earlier in the text. The purpose of this Appendix is to explain some of the more subtle features of the design.

The current source supplying the input transistors is Q_{29}. It is designed to supply a total input stage current of 6 μA at 25°C. This current drops to 3 μA at -55°C but increases to only 7.5 μA at 125°C. This temperature characteristic tends to compensate for the current gain falloff of the input transistors at low temperatures without creating stability problems at high temperatures.

The biasing circuitry for the input current source is nearly identical to that in the LM101A, and a complete description is given in Reference 4. However, a brief explanation follows.

A collector FET,[6] Q_{23}, which has a saturation current of about 30 μA, establishes the collector current of Q_{24}. This FET provides the initial turn-on current for the circuit and insures starting under all conditions. The purpose of R_{14} is to compensate for production and temperature variations in the FET current. It is a collector resistor (indicated by the T through it) made of the same semiconductor material as the FET channel. As the FET current varies, the drop across R_{14} tends to compensate for changes in the emitter base voltage of Q_{24}.

The collector-emitter voltage of Q_{24} is equal to the emitter base voltage of Q_{24} plus that of Q_{25}. This voltage is delivered to Q_{26} and Q_{29}. Q_{25} and Q_{24} are operated at substantially higher currents than Q_{26} and Q_{29}. Hence, there is a differential in

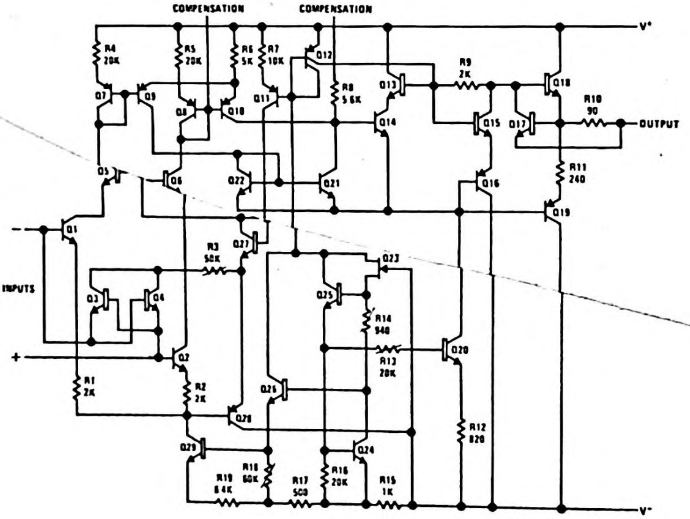

COMPENSATION
COMPENSATION
V+
R4 20K
R5 20K
R6 5K
R7 10K
Q12
R9 2K
Q18
R8 5.6K
Q13
Q7
Q9
Q11
Q8
Q10
Q14
Q15
Q17
R10 90
OUTPUT
R11 240
Q5
Q6
Q22
Q21
Q16
Q19
Q1
R3 50K
Q27
Q23
INPUTS
Q3
Q4
Q25
R14 340
Q20
R13 20K
Q2
R1 2K
R2 2K
Q26
Q28
R12 820
Q29
Q24
R18 60K
R19 6.4K
R17 500
R16 20K
R15 1K
V-

FIGURE A1. Complete Schematic Of The LM108

their emitter base voltages that is dropped across R_{19} to determine the input stage current. R_{18} is a pinched base resistor, as is indicated by the slash bar through it. This resistor, which has a large positive temperature coefficient, operates in conjunction with R_{17} to help shape the temperature characteristics of the input stage current source.

The output currents of Q_{26}, Q_{25} and Q_{23} are fed to Q_{12}, which is a controlled-gain lateral PNP.[6] It delivers one-half of the combined currents to the output stage. Q_{11} is also connected to Q_{12}, with its output current set at approximately 15 μA by R_7. Since this type of current source makes use of the emitter-base voltage differential between similar transistors operating at different collector currents, the output of Q_{11} is relatively independent of the current delivered to Q_{12}.[12] This current is used for the input stage bootstrapping circuitry.

Q_{20} also supplies current to the class-B output stage. Its output current is determined by the ratio of R_{15} to R_{12} and the current through R_{12}. R_{13} is included so that the biasing circuitry is not upset when Q_{20} saturates.

One major departure from the simplified schematic is the bootstrapping of the second stage active loads, Q_{21} and Q_{22}, to the output. This makes the second stage gain dependent only on how well Q_9 and Q_{10} match with variations in output voltage. Hence, the second stage gain is quite high. In fact, the overall gain of the amplifier is typically in excess of 10^6 at dc.

The second stage active loads drive Q_{14}. A high-gain primary transistor is used to prevent loading of the second stage. Its collector is bootstrapped by Q_{13} to operate it at zero collector-base voltage. The class-B output stage is actually driven by the emitter of Q_{14}.

A dead zone in the output stage is prevented by biasing Q_{18} and Q_{19} on the verge of conduction with Q_{15} and Q_{16}. R_9 is used to compensate for the transconductance of Q_{15} and Q_{16}, making the output stage quiescent current relatively independent of the output current of Q_{12}. The drop across this resistor also reduces quiescent current.

For positive-going outputs, short circuit protection is provided by R_{10} and Q_{17}. When the voltage drop across R_{10} turns on Q_{17}, it removes base drive from Q_{18}. For negative-going outputs, current limiting is initiated when the voltage drop across R_{11} becomes large enough for the collector base junction of Q_{17} to become forward biased. When this happens, the base of Q_{19} is clamped so the output current cannot increase further.

Input protection is provided by Q_3 and Q_4 which act as clamp diodes between the inputs. The collectors of these transistors are bootstrapped to the emitter of Q_{28} through R_3. This keeps the collector-isolation leakage of the transistors from showing up on the inputs. R_3 is included so that the bootstrapping is not disrupted when Q_3 or Q_4 saturate with an input overload. Current-limiting resistors were not connected in series with the inputs, since diffused resistors cannot be employed such that they work effectively, without causing high temperature leakages.

Table I. Typical Performance of the LM108 Operational Amplifier ($T_A = 25°C$ and $V_S = ±15V$).

Input Offset Voltage	0.7 mV
Input Offset Current	50 pA
Input Bias Current	0.8 nA
Input Resistance	70 MΩ
Input Common Mode Range	±14V
Common Mode Rejection	100 dB
Offset Voltage Drift	3 μV/°C
Offset Current Drift	0.5 pA/°C
Voltage Gain	300V/mV
Small Signal Bandwidth	1.0 MHz
Slew Rate	0.3V/μs
Output Swing	±14V
Supply Current	300 μA
Power Supply Rejection	100 dB
Operating Voltage Range	±2V to ±20V

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Log Converters

National Semiconductor
Application Note 30
Robert C. Dobkin
November 1969

One of the most predictable non-linear elements commonly available is the bipolar transistor. The relationship between collector current and emitter base voltage is precisely logarithmic from currents below one picoamp to currents above one milliamp. Using a matched pair of transistors and integrated circuit operational amplifiers, it is relatively easy to construct a linear to logarithmic converter with a dynamic range in excess of five decades.

The circuit in Figure 1 generates a logarithmic output voltage for a linear input current. Transistor Q_1 is used as the non-linear feedback element around an LM108 operational amplifier. Negative feedback is applied to the emitter of Q_1 through divider, R_1 and R_2, and the emitter base junction of Q_2. This forces the collector current of Q_1 to be exactly equal to the current through the input resistor. Transistor Q_2 is used as the feedback element of an LM101A operational amplifier. Negative feedback forces the collector current of Q_2 to equal the current through R_3. For the values shown, this current is 10 µA. Since the collector current of Q_2 remains constant, the emitter base voltage also remains constant. Therefore, only the V_{BE} of Q_1 varies with a change of input current. However, the output voltage is a function of the difference in emitter base voltages of Q_1 and Q_2:

$$E_{OUT} = \frac{R_1 + R_2}{R_2} (V_{BE_2} - V_{BE_1}). \qquad (1)$$

For matched transistors operating at different collector currents, the emitter base differential is given by

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C_1}}{I_{C_2}}, \qquad (2)$$

where k is Boltzmann's constant, T is temperature in degrees Kelvin and q is the charge of an electron. Combining these two equations and writing the expression for the output voltage gives

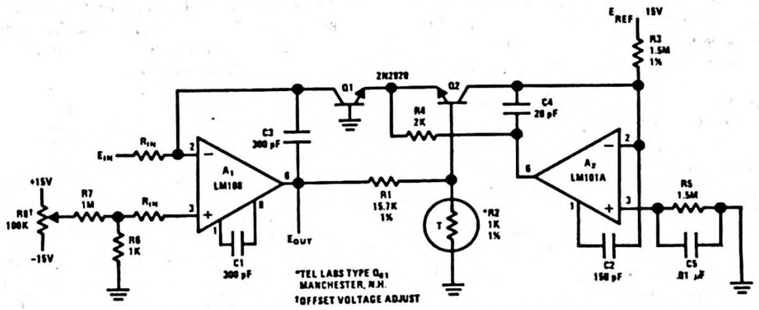
$$E_{OUT} = \frac{-kT}{q} \left[\frac{R_1 + R_2}{R_2}\right] \log_e \left[\frac{E_{IN} R_3}{E_{REF} R_{IN}}\right] \qquad (3)$$

for $E_{IN} \geq 0$. This shows that the output is proportional to the logarithm of the input voltage. The coefficient of the log term is directly proportional to absolute temperature. Without compensation, the scale factor will also vary directly with temperature. However, by making R_2 directly proportional to temperature, constant gain is obtained. The temperature compensation is typically 1% over a temperature range of −25°C to 100°C for the resistor specified. For limited temperature range applications, such as 0°C to 50°C, a 430Ω sensistor in series with a 570Ω resistor may be substituted for the 1K resistor, also with 1% accuracy. The divider, R_1 and R_2, sets the gain while the current through R_3 sets the zero. With the values given, the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10} \left|\frac{E_{IN}}{R_{IN}}\right| + 5\right] \qquad (4)$$

where the absolute value sign indicates that the dimensions of the quantity inside are to be ignored.

Log generator circuits are not limited to inverting operation. In fact, a feature of this circuit is the ease with which non-inverting operation is obtained. Supplying the input signal to A_2 and the reference current to A_1 results in a log output that is not inverted from the input. To achieve the same 100 dB dynamic range in the non-inverting configuration, an LM108 should be used for A_2, and an LM101A for A_1. Since the LM108 cannot use feedforward compensation, it is frequency compensated with the standard 30 pF capacitor.



*TEL LABS TYPE Q81 MANCHESTER, N.H.
†OFFSET VOLTAGE ADJUST

FIGURE 1. Log Generator with 100 dB Dynamic Range

The only other change is the addition of a clamp diode connected from the emitter of Q_1 to ground. This prevents damage to the logging transistors if the input signal should go negative.

The log output is accurate to 1% for any current between 10 nA and 1 mA. This is equivalent to about 3% referred to the input. At currents over 500 μA the transistors used deviate from log characteristics due to resistance in the emitter, while at low currents, the offset current of the LM108 is the major source of error. These errors occur at the ends of the dynamic range, and from 40 nA to 400 μA the log converter is 1% accurate referred to the input. Both of the transistors are used in the grounded base connection, rather than the diode connection, to eliminate errors due to base current. Unfortunately, the grounded base connection increases the loop gain. More frequency compensation is necessary to prevent oscillation, and the log converter is necessarily slow. It may take 1 to 5 ms for the output to settle to 1% of its final value. This is especially true at low currents.

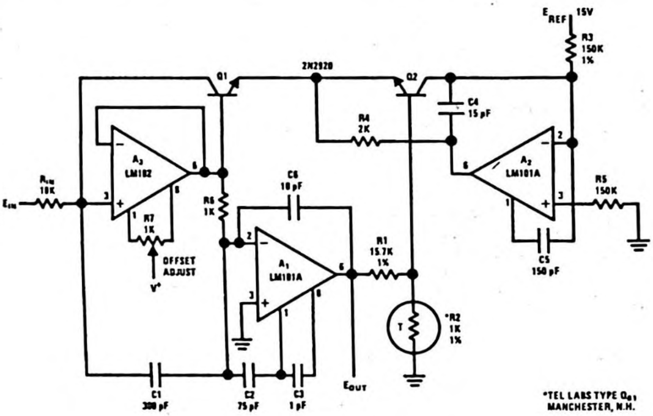


FIGURE 2. Fast Log Generator

The circuit shown in Figure 2 is two orders of magnitude faster than the previous circuit and has a dynamic range of 80 dB. Operation is the same as the circuit in Figure 1, except the configuration optimizes speed rather than dynamic range. Transistor Q_1 is diode connected to allow the use of feedforward compensation[1] on an LM101A operational amplifier. This compensation extends the bandwidth to 10 MHz and increases the slew rate. To prevent errors due to the finite h_{FE} of Q_1 and the bias current of the LM101A, an LM102 voltage follower buffers the base current and input current. Although the log circuit will operate without the LM102, accuracy will degrade at low input currents. Amplifier A_2 is also compensated for maximum bandwidth. As with the previous log converter, R_1 and R_2 control the sensitivity; and R_3 controls the zero crossing of the transfer function. With the values shown the scale factor is 1V/decade and

$$E_{OUT} = -\left[\log_{10}\left|\frac{E_{IN}}{R_{IN}}\right| + 4\right] \qquad (5)$$

from less than 100 nA to 1 mA.

Anti-log or exponential generation is simply a matter of rearranging the circuitry. Figure 3 shows the circuitry of the log converter connected to generate an exponential output from a linear input. Amplifier A_1 in conjunction with transistor Q_1 drives the emitter of Q_2 in proportion to the input voltage. The collector current of Q_2 varies exponentially with the emitter-base voltage. This current is converted to a voltage by amplifier A_2. With the values given

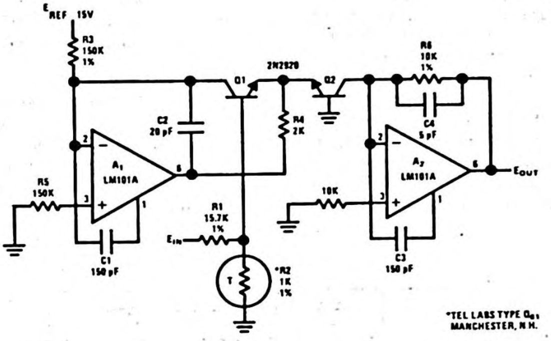
$$E_{OUT} = 10^{-[E_{IN}]}. \qquad (6)$$

Many non-linear functions such as $X^{1/2}$, X^2, X^3, 1/X, XY, and X/Y are easily generated with the use of logs. Multiplication becomes addition, division becomes subtraction and powers become gain coefficients of log terms. Figure 4 shows a circuit whose output is the cube of the input. Actually, any power function is available from this circuit by changing the values of R_9 and R_{10} in accordance with the expression:

$$E_{OUT} = E_{IN}^{\frac{16.7\,R_9}{R_9 + R_{10}}}. \qquad (7)$$

Note that when log and anti-log circuits are used to perform an operation with a linear output, no temperature compensating resistors at all are needed. If the log and anti-log transistors are at the same temperature, gain changes with temperature cancel. It is a good idea to use a heat sink which couples the two transistors to minimize thermal gradients. A 1°C temperature difference between the log and anti-log transistors results in a 0.3% error. Also, in the log converters, a 1°C difference between the log transistors and the compensating resistor results in a 0.3% error.

Either of the circuits in Figures 1 or 2 may be used as dividers or reciprocal generators. Equation 3 shows the outputs of the log generators are actually the ratio of two currents: the input current and the current through R_3. When used as a log generator, the current through R_3 was held constant by connecting R_3 to a fixed voltage. Hence, the output was just the log of the input. If R_3 is driven by an input voltage, rather than the 15V reference, the output of the log generator is the log ratio of the input current to the current through R_3. The anti-log of this voltage is the quotient. Of course, if the divisor is constant, the output is the reciprocal.


E_REF 15V
R3
150K
1%
2N2920
Q1
Q2
R8
10K
1%
C2
20 pF
R4
2K
C4
5 pF
2
A1
LM101A
6
A2
LM101A
6
E_OUT
R5
150K
3
1
R1
15.7K
1%
10K
3
1
E_IN
C1
150 pF
T
*R2
1K
1%
C3
150 pF

*TEL LABS TYPE Q81
MANCHESTER, N.H.

FIGURE 3. Anti-log Generator

A complete one quadrant multiplier/divider is shown in Figure 5. It is basically the log generator shown in Figure 1 driving the anti-log generator shown in Figure 3. The log generator output from A_1 drives the base of Q_3 with a voltage proportional to the log of E_1/E_2. Transistor Q_3 adds a voltage proportional to the log of E_3 and drives the anti-log transistor, Q_4. The collector current of Q_4 is converted to an output voltage by A_4 and R_7, with the scale factor set by R_7 at $E_1\ E_3/10E_2$.

Measurement of transistor current gains over a wide range of operating currents is an application particularly suited to log multiplier/dividers. Using the circuit in Figure 5, PNP current gains can be measured at currents from 0.4 μA to 1 mA. The collector current is the input signal to A_1, the base current is the input signal to A_2, and a fixed voltage to R_5 sets the scale factor. Since A_2 holds the base at ground, a single resistor from the emitter to the positive supply is all that is needed to establish the operating current. The output is proportional to collector current divided by base current, or h_{FE}.

In addition to their application in performing functional operations, log generators can provide a significant increase in the dynamic range of signal processing systems. Also, unlike a linear system, there is no loss in accuracy or resolution when the

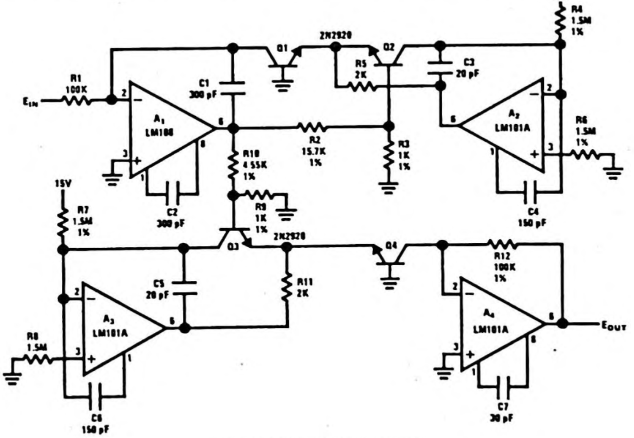

15V
R4
1.5M
1%
2N2920
Q1
Q2
R1
100K
E_IN
C1
300 pF
R5
2K
C3
20 pF
2
A1
LM108
6
8
3
1
A2
LM101A
6
2
3
1
R6
1.5M
1%
R2
15.7K
1%
R3
1K
1%
R10
4.55K
1%
15V
R9
1K
1%
C2
300 pF
C4
150 pF
R7
1.5M
1%
Q3
2N2920
Q4
R12
100K
1%
C5
20 pF
R11
2K
2
A3
LM101A
6
A4
LM101A
6
E_OUT
R8
1.5M
3
1
3
8
1
C6
150 pF
C7
30 pF

FIGURE 4. Cube Generator

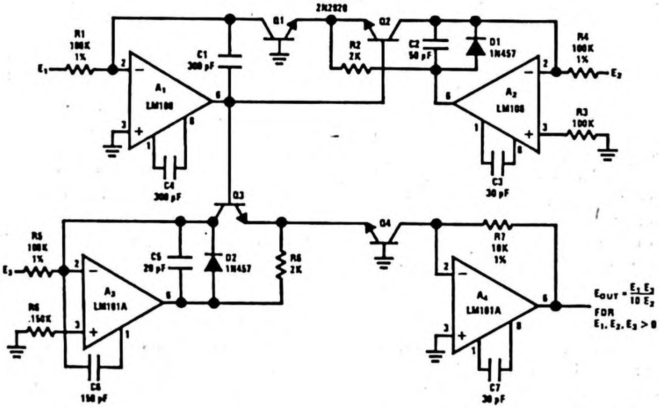
input signal is small compared to full scale. Over most of the dynamic range, the accuracy is a percent-of-signal rather than a percent-of-full-scale. For example, using log generators, a simple meter can display signals with 100 dB dynamic range or an oscilloscope can display a 10 mV and 10V pulse simultaneously. Obviously, without the log generator, the low level signals are completely lost.

To achieve wide dynamic range with high accuracy, the input operational amplifier necessarily must have low offset voltage, bias current and offset current. The LM108 has a maximum bias current of *3 nA* and offset current of *400 pA* over a −55°C to 125°C temperature range. By using equal source resistors, only the offset current of the LM108 causes an error. The offset current of the LM108 is as low as many FET amplifiers. Further, it has a low and constant temperature coefficient rather than doubling every 10°C. This results in greater accuracy over temperature than can be achieved with FET amplifiers. The offset voltage may be zeroed, if necessary, to improve accuracy with low input voltages.

The log converters are low level circuits and some care should be taken during construction. The input leads should be as short as possible and the input circuitry guarded against leakage currents. Solder residues can easily conduct leakage currents, therefore circuit boards should be cleaned before use. High quality glass or mica capacitors should be used on the inputs to minimize leakage currents. Also, when the +15V supply is used as a reference, it must be well regulated.

REFERENCES:

1. R. C. Dobkin, "*Feedforward Compensation Speeds Op Amp*," National Semiconductor Corporation, Linear Brief 2, April, 1969.
2. R. J. Widlar, "*Monolithic Operational Amplifiers—The Universal Linear Component*," National Semiconductor Corporation, AN-4, April, 1968.



2N2920
Q1
Q2
R1 100K 1%
E1
C1 300 pF
R2 2K
C2 50 pF
D1 1N457
R4 100K 1%
E2
A1 LM108
A2 LM108
R3 100K
C4 300 pF
C3 30 pF
Q3
Q4
R5 100K 1%
E3
C5 20 pF
D2 1N457
R8 2K
R6 .150K
A3 LM101A
R7 10K 1%
A4 LM101A
C6 150 pF
C7 30 pF
$E_{OUT} = \frac{E_1 E_3}{10 E_2}$
FOR
$E_1, E_2, E_3 > 0$

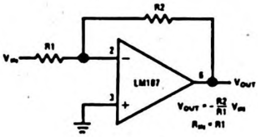
FIGURE 5. Multiplier/Divider

Op Amp Circuit Collection

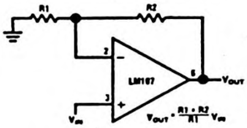
National Semiconductor
Application Note 31
Robert C. Dobkin
February 1978

AN-31 Op Amp Circuit Collection

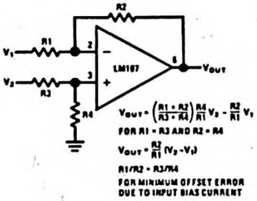
section 1 — basic circuits


R2
R1
V_{IN}
2
3
LM107
6
V_{OUT}
$V_{OUT} = -\frac{R2}{R1} V_{IN}$
$R_{IN} = R1$

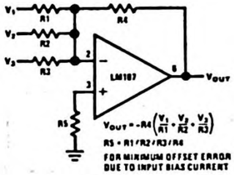
Inverting Amplifier


R1
R2
2
3
LM107
6
V_{OUT}
V_{IN}
$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$

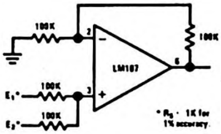
Non-Inverting Amplifier


R2
R1
V_1
V_2
R3
R4
2
3
LM107
6
V_{OUT}
$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1} V_2 - \frac{R2}{R1} V_1$
FOR R1 = R3 AND R2 = R4
$V_{OUT} = \frac{R2}{R1}(V_2 - V_1)$
R1/R2 = R3/R4
FOR MINIMUM OFFSET ERROR
DUE TO INPUT BIAS CURRENT

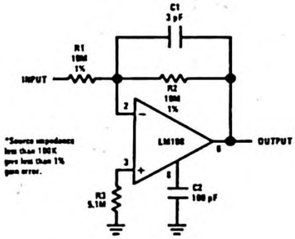
Difference Amplifier


V_1
R1
V_2
R2
V_3
R3
R4
2
3
LM107
6
V_{OUT}
R5
$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$
R5 = R1/R2/R3/R4
FOR MINIMUM OFFSET ERROR
DUE TO INPUT BIAS CURRENT

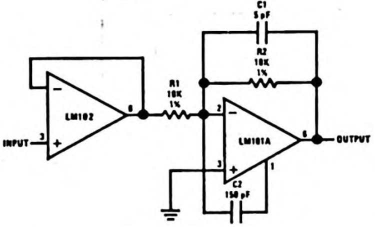
Inverting Summing Amplifier


100K
100K
2
3
LM107
6
E_1*
100K
E_2*
100K
* R_S = 1K for
1% accuracy.

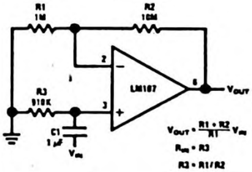
Non-Inverting Summing Amplifier


C1
3 pF
R1
10M
1%
INPUT
R2
10M
1%
2
3
LM108
6
8
OUTPUT
*Source impedance
less than 100K
gives less than 1%
gain error.
R3
5.1M
C2
100 pF

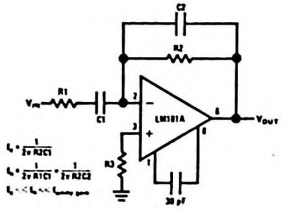
Inverting Amplifier with High Input Impedance


C1
5 pF
R2
10K
1%
LM102
6
INPUT
3
R1
10K
1%
2
3
LM101A
6
1
OUTPUT
C2
150 pF

Fast Inverting Amplifier With High Input Impedance


R1
1M
R2
10M
2
3
LM107
6
V_{OUT}
R3
910K
C1
1 µF
V_{IN}
$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$
$R_{IN} = R3$
R3 = R1/R2

Non-Inverting AC Amplifier

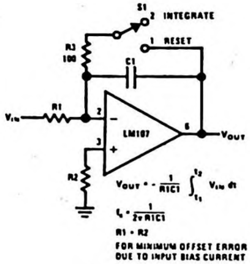

C2
R2
R1
V_{IN}
C1
2
3
LM101A
6
8
1
R3
30 pF
V_{OUT}

$f_c = \frac{1}{2\pi R2C1}$

$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$

$f_c << f_h << f_{unity\ gain}$

Practical Differentiator


S1
2 INTEGRATE
1 RESET
R3
100
C1
R1
V_{IN}
2
3
LM107
6
V_{OUT}
R2

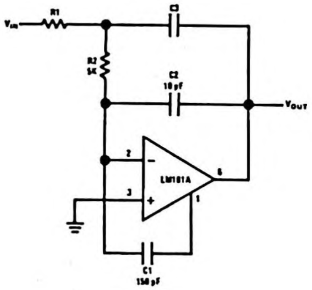
$V_{OUT} = -\frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$

$f_c = \frac{1}{2\pi R1C1}$

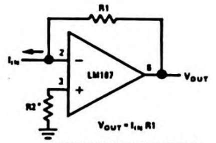
R1 = R2

FOR MINIMUM OFFSET ERROR
DUE TO INPUT BIAS CURRENT

Integrator


V_{IN}
R1
C3
R2
5K
C2
10 pF
V_{OUT}
2
3
LM101A
6
1
C1
150 pF

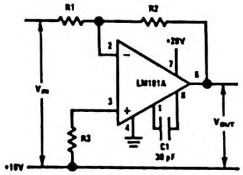
Fast Integrator


R1
I_{IN}
2
3
LM107
6
V_{OUT}
R2*

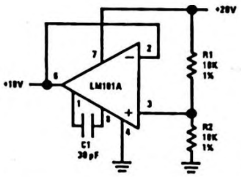
$V_{OUT} = I_{IN}\,R1$

*FOR MINIMUM ERROR DUE TO
BIAS CURRENT R2 = R1

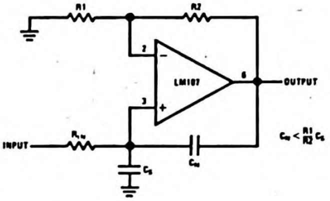
Current to Voltage Converter


R1
R2
+20V
7
2
LM101A
6
3
8
1
4
V_{IN}
R3
C1
30 pF
V_{OUT}
+10V

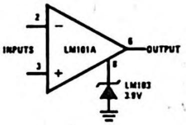
Circuit for Operating the LM101
without a Negative Supply


+20V
7
2
+10V
6
LM101A
R1
10K
1%
3
1
8
4
C1
30 pF
R2
10K
1%

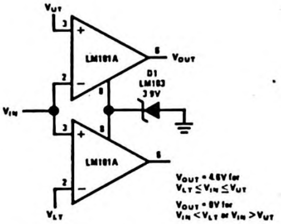
Circuit for Generating the
Second Positive Voltage


R1
R2
2
3
LM107
6
OUTPUT
INPUT
R_{IN}
C_S
C_N
$C_N < \frac{R1}{R2} C_S$

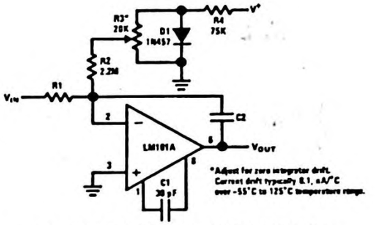
Neutralizing Input Capacitance to Optimize Response Time


2
INPUTS
LM101A
3
6
OUTPUT
8
LM103
3.9V

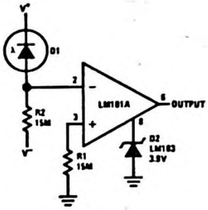
Voltage Comparator for Driving DTL or TTL Integrated Circuits


V_{UT}
3
LM101A
6
V_{OUT}
2
D1
LM103
3.9V
V_{IN}
8
3
8
LM101A
6
2
V_{LT}
$V_{OUT} = 4.6V$ for
$V_{LT} \leq V_{IN} \leq V_{UT}$
$V_{OUT} = 0V$ for
$V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

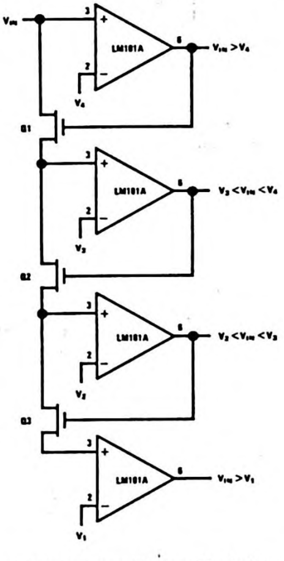
Double-Ended Limit Detector


R3*
20K
D1
1N457
R4
75K
V^+
R2
2.2M
R1
V_{IN}
2
C2
LM101A
6
V_{OUT}
3
8
C1
30 pF
1
*Adjust for zero integrator drift.
Current drift typically 0.1, nA/°C
over −55°C to 125°C temperature range.

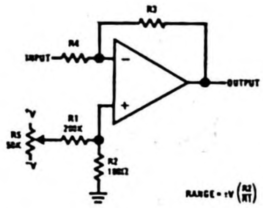
Integrator with Bias Current Compensation


V^+
λ
D1
2
LM101A
6
OUTPUT
R2
15M
3
8
V^-
R1
15M
D2
LM103
3.9V

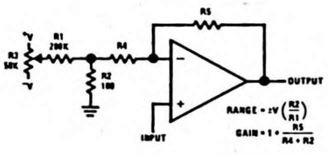
Threshold Detector for Photodiodes


V_{IN}
3
LM101A
6
$V_{IN} > V_4$
2
V_4
Q1
3
LM101A
6
$V_3 < V_{IN} < V_4$
2
V_3
Q2
3
LM101A
6
$V_2 < V_{IN} < V_3$
2
V_2
Q3
3
LM101A
6
$V_{IN} > V_1$
2
V_1

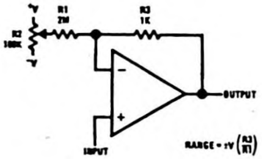
Multiple Aperture Window Discriminator


R3
R4
INPUT
OUTPUT
+V
R5
50K
R1
200K
-V
R2
100Ω
$RANGE = \pm V\left(\frac{R2}{R1}\right)$

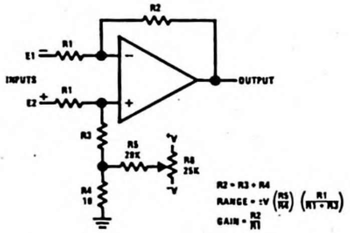
Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element


R5
+V
R3
50K
-V
R1
200K
R4
R2
100
OUTPUT
INPUT
$RANGE = \pm V\left(\frac{R2}{R1}\right)$
$GAIN = 1 + \frac{R5}{R4 + R2}$

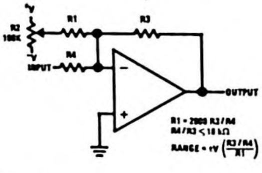
Offset Voltage Adjustment for Non-Inverting Amplifiers


+V
R2
100K
-V
R1
2M
R3
1K
OUTPUT
INPUT
$RANGE = \pm V\left(\frac{R3}{R1}\right)$

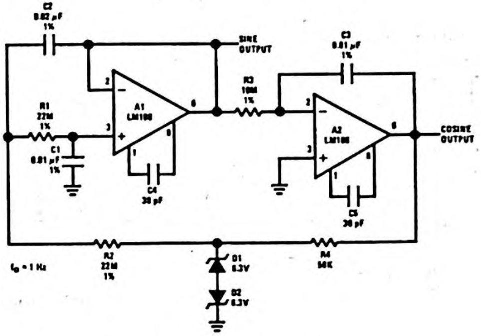
Offset Voltage Adjustment for Voltage Followers


R2
E1
R1
INPUTS
E2
R1
OUTPUT
R3
R5
20K
+V
R6
25K
-V
R4
10
$R2 = R3 + R4$
$RANGE = \pm V\left(\frac{R5}{R4}\right)\left(\frac{R1}{R1 + R3}\right)$
$GAIN = \frac{R2}{R1}$

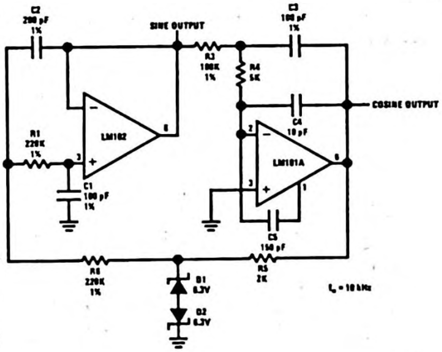
Offset Voltage Adjustment for Differential Amplifiers


+V
R2
100K
-V
R1
R3
R4
INPUT
OUTPUT
$R1 = 2000\ R3/R4$
$R4/R3 < 10\ k\Omega$
$RANGE = \pm V\left(\frac{R3/R4}{R1}\right)$

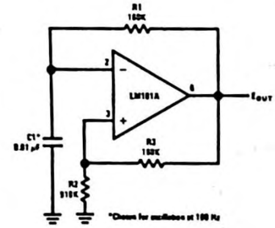
Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less


C2
0.02 μF
1%
SINE
OUTPUT
C3
0.01 μF
1%
R3
10M
1%
2
3
6
8
1
A1
LM108
R1
22M
1%
C1
0.01 μF
1%
C4
30 pF
A2
LM108
COSINE
OUTPUT
C5
30 pF
f_O = 1 Hz
R2
22M
1%
D1
6.3V
D2
6.3V
R4
56K

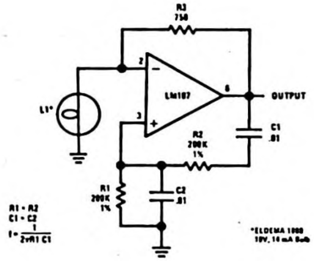
Low Frequency Sine Wave Generator with Quadrature Output


C2
200 pF
1%
SINE OUTPUT
C3
100 pF
1%
R3
100K
1%
R4
5K
COSINE OUTPUT
C4
10 pF
LM102
R1
220K
1%
C1
100 pF
1%
LM101A
2
3
6
1
C5
150 pF
R6
220K
1%
R5
2K
D1
6.3V
D2
6.3V
f_o = 10 kHz

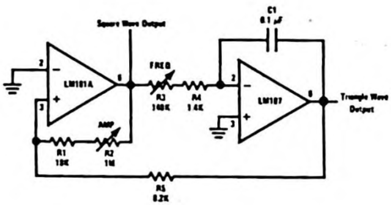
High Frequency Sine Wave Generator with Quadrature Output


R1
100K
2
3
6
LM101A
E_{OUT}
C1*
0.01 µF
R3
100K
R2
910K
*Chosen for oscillation at 100 Hz

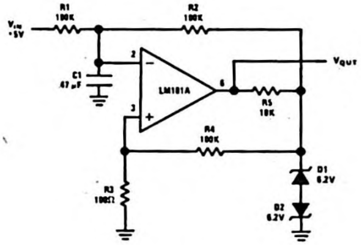
Free-Running Multivibrator


R3
750
2
3
6
LM107
OUTPUT
L1*
C1
.01
R2
200K
1%
R1
200K
1%
C2
.01
R1 = R2
C1 = C2
$f = \frac{1}{2\pi R1\ C1}$
*ELDEMA 1869
10V, 14 mA Bulb

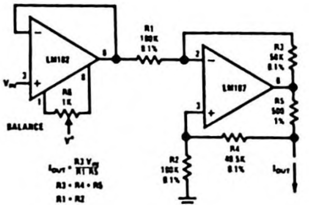
Wein Bridge Sine Wave Oscillator


Square Wave Output
C1
0.1 µF
2
3
6
LM101A
FREQ
R3
100K
R4
1.4K
LM107
Triangle Wave Output
AMP
R1
10K
R2
1M
R5
8.2K

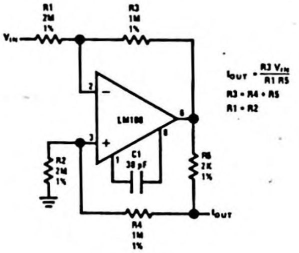
Function Generator


V_{IN}
±5V
R1
100K
R2
100K
C1
.47 µF
2
3
6
LM101A
V_{OUT}
R5
10K
R4
100K
R3
100Ω
D1
6.2V
D2
6.2V

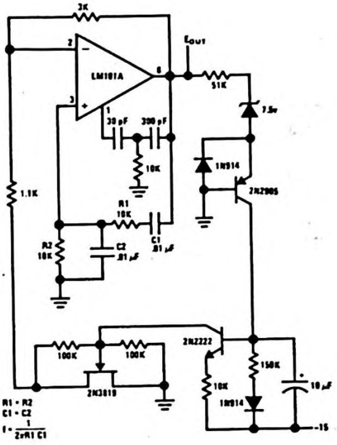
Pulse Width Modulator


LM102
V_{IN}
3
1
8
6
R6
1K
BALANCE
V^-
R1
100K
0.1%
2
LM107
R3
50K
0.1%
R5
500
1%
R4
49.5K
0.1%
R2
100K
0.1%
I_{OUT}
$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$
R3 = R4 + R5
R1 = R2

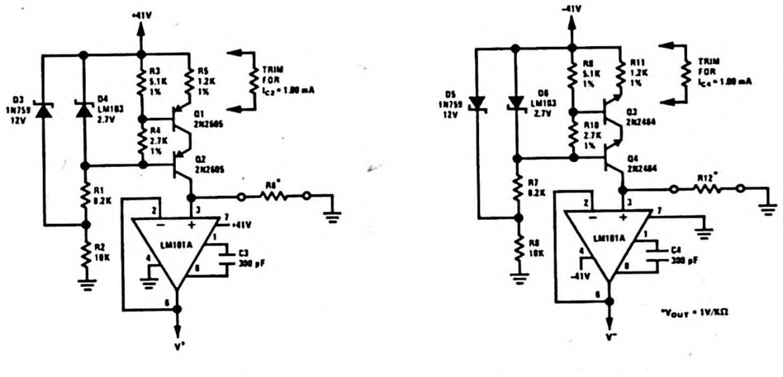
Bilateral Current Source


R1
2M
1%
R3
1M
1%
V_{IN}
2
3
6
8
1
LM108
C1
30 pF
R2
2M
1%
R5
2K
1%
R4
1M
1%
I_{OUT}
$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$
R3 = R4 + R5
R1 = R2

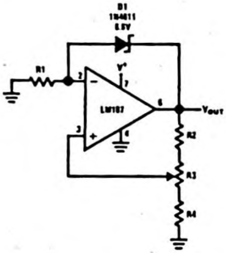
Bilateral Current Source


3K
EOUT
2
LM101A
6
3
1
30 pF
300 pF
51K
7.5v
10K
1N914
2N2905
1.1K
R1
10K
C1
.01 μF
R2
10K
C2
.01 μF
2N2222
100K
100K
150K
2N3819
10K
10 μF
1N914
-15
R1 = R2
C1 = C2
f = 1/(2πR1 C1)

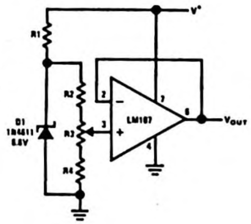
Wein Bridge Oscillator with FET Amplitude Stabilization


+41V
R3
5.1K
1%
R5
1.2K
1%
TRIM
FOR
IC2 = 1.00 mA
D3
1N759
12V
D4
LM103
2.7V
Q1
2N2605
R4
2.7K
1%
Q2
2N2605
R8*
R1
8.2K
2
3
7
+41V
1
LM101A
C3
300 pF
R2
10K
4
8
6
V+
-41V
R9
5.1K
1%
R11
1.2K
1%
TRIM
FOR
IC4 = 1.00 mA
D5
1N759
12V
D6
LM103
2.7V
Q3
2N2484
R10
2.7K
1%
Q4
2N2484
R12*
R7
8.2K
2
3
7
LM101A
1
C4
300 pF
R8
10K
4
-41V
8
6
*VOUT = 1V/KΩ
V-

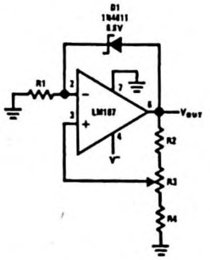
Low Power Supply for Integrated Circuit Testing


D1
1N4611
6.6V
R1
V+
2
7
LM107
3
4
6
VOUT
R2
R3
R4

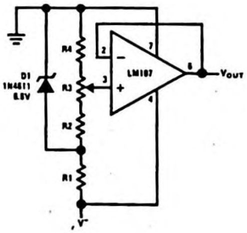
Positive Voltage Reference


V+
R1
R2
D1
1N4611
6.6V
R3
R4
2
3
7
LM107
6
4
VOUT

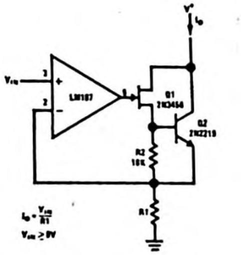
Positive Voltage Reference


D1
1N4611
6.6V
R1
2
3
7
LM107
6
4
V−
VOUT
R2
R3
R4

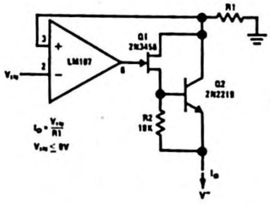
Negative Voltage Reference


R4
D1
1N4611
6.6V
R3
R2
R1
2
3
7
LM107
6
4
VOUT
V−

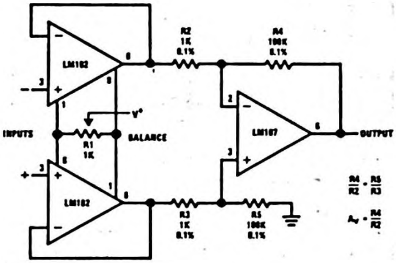
Negative Voltage Reference


V+
IO
VIN
3
2
LM107
6
Q1
2N3458
Q2
2N2219
R2
10K
R1
IO = VIN/R1
VIN ≥ 0V

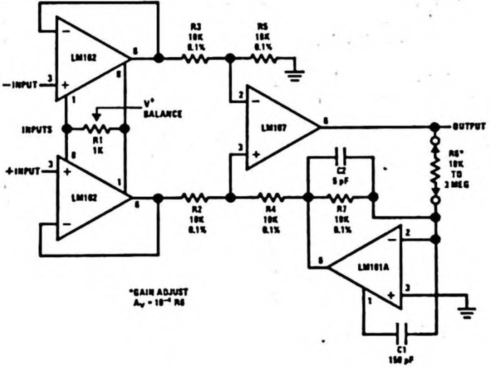
Precision Current Sink


R1
3
2
VIN
LM107
6
Q1
2N3458
Q2
2N2219
R2
10K
IO = VIN/R1
VIN ≤ 0V
IO
V−

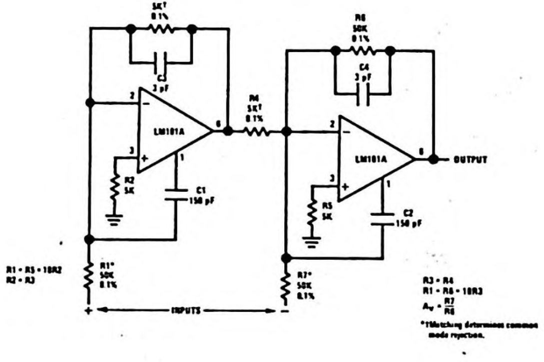
Precision Current Source


R2
1K
0.1%
R4
100K
0.1%
LM102
6
3
8
1
V⁺
INPUTS
R1
1K
BALANCE
2
LM107
6
OUTPUT
3
8
1
LM102
6
R3
1K
0.1%
R5
100K
0.1%
$\frac{R4}{R2} = \frac{R5}{R3}$
$A_V = \frac{R4}{R2}$

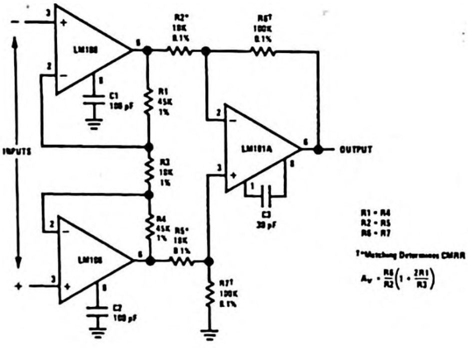
Differential-Input Instrumentation Amplifier


R3
10K
0.1%
R5
10K
0.1%
LM102
6
8
−INPUT
3
1
V⁺
BALANCE
INPUTS
R1
1K
8
+INPUT
3
1
LM102
6
2
LM107
6
OUTPUT
3
C2
5 pF
R6*
10K
TO
3 MEG
R2
10K
0.1%
R4
10K
0.1%
R7
10K
0.1%
2
6
LM101A
3
1
C1
150 pF
*GAIN ADJUST
$A_V = 10^{-4}$ R6

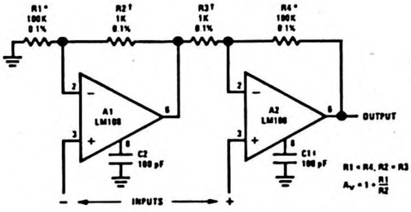
Variable Gain, Differential-Input Instrumentation Amplifier


R3
5K†
0.1%
C3
3 pF
2
3
LM101A
6
1
R2
5K
C1
150 pF
R4
5K†
0.1%
R6
50K
0.1%
C4
3 pF
2
3
LM101A
6
1
OUTPUT
R5
5K
C2
150 pF
R1 = R5 = 10R2
R2 = R3
R1*
50K
0.1%
R7*
50K
0.1%
+
INPUTS
−
R3 = R4
R1 = R6 = 10R3
$A_V = \frac{R7}{R6}$
*†Matching determines common mode rejection.

Instrumentation Amplifier with ±100 Volt Common Mode Range


3
−
+
LM108
2
8
C1
100 pF
6
R2*
10K
0.1%
R6†
100K
0.1%
R1
45K
1%
INPUTS
R3
10K
1%
2
3
LM101A
6
8
1
OUTPUT
C3
30 pF
2
LM108
6
R4
45K
1%
R5*
10K
0.1%
3
+
8
C2
100 pF
R7†
100K
0.1%
R1 = R4
R2 = R5
R6 = R7
†*Matching Determines CMRR
$A_V = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right)$

Differential Input Instrumentation Amplifier with High Common Mode Rejection


R1*
100K
0.1%
R2†
1K
0.1%
R3†
1K
0.1%
R4*
100K
0.1%
2
3
6
8
A1
LM108
A2
LM108
C2
100 pF
C1‡
100 pF
OUTPUT
− INPUTS +

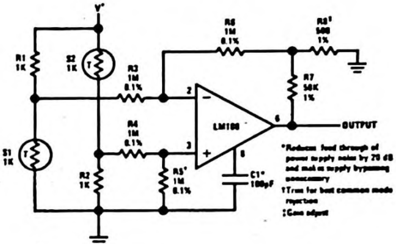
R1 = R4, R2 = R3

$A_V = 1 + \frac{R1}{R2}$

*†Matching determines CMRR

‡May be deleted to maximize bandwidth

High Input Impedance Instrumentation Amplifier

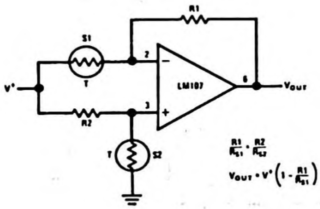

V+
R1
1K
S2
1K
T
R3
1M
0.1%
R6
1M
0.1%
R8‡
500
1%
R7
50K
1%
R4
1M
0.1%
S1
1K
R2
1K
R5†
1M
0.1%
LM108
2
3
6
8
C1*
100pF
OUTPUT

*Reduces feed through of power supply noise by 20 dB and makes supply bypassing unnecessary

†Trim for best common mode rejection

‡Gain adjust

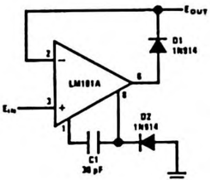
Bridge Amplifier with Low Noise Compensation


R1
S1
T
V+
R2
2
3
6
LM107
VOUT
T
S2

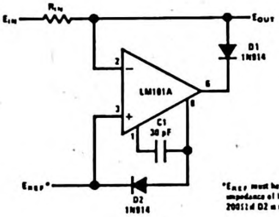
$\frac{R1}{R_{S1}} = \frac{R2}{R_{S2}}$

$V_{OUT} = V^+\left(1 - \frac{R1}{R_{S1}}\right)$

Bridge Amplifier

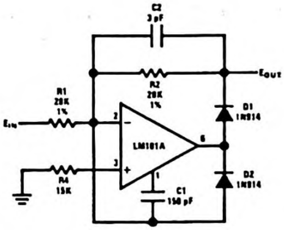

EOUT
D1
1N914
2
3
6
8
1
LM101A
EIN
D2
1N914
C1
30 pF

Precision Diode

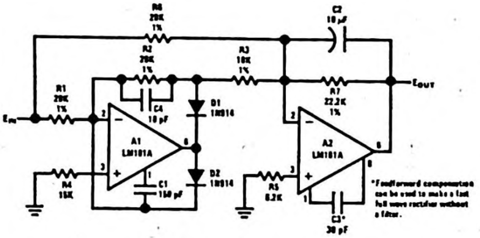

EIN
RIN
EOUT
D1
1N914
2
3
6
8
1
LM101A
C1
30 pF
EREF*
D2
1N914

*E_{REF} must have a source impedance of less than 200Ω if D2 is used.

Precision Clamp

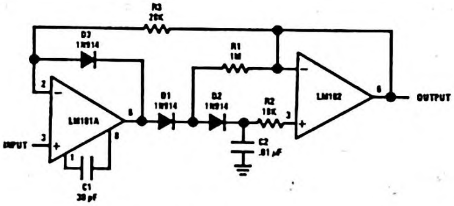

C2
3 pF
R2
20K
1%
EOUT
R1
20K
1%
EIN
2
3
6
1
8
LM101A
D1
1N914
D2
1N914
R4
15K
C1
150 pF

Fast Half Wave Rectifier

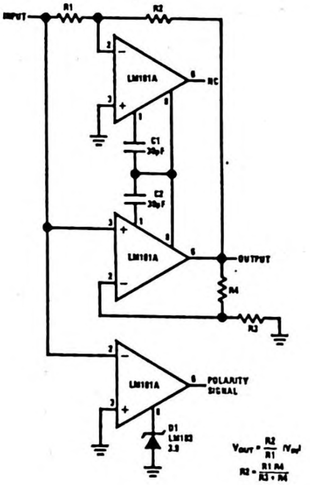

R6
20K
1%
C2
10 µF
R2
20K
1%
R3
10K
1%
R1
20K
1%
E_IN
C4
10 pF
D1
1N914
R7
22.2K
1%
E_OUT
A1
LM101A
A2
LM101A
R4
15K
C1
150 pF
D2
1N914
R5
6.2K
C3*
30 pF
2
3
6
1
8

*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Precision AC to DC Converter


R3
20K
D3
1N914
R1
1M
LM101A
LM102
D1
1N914
D2
1N914
R2
10K
INPUT
OUTPUT
C2
.01 µF
C1
30 pF
2
3
6
1
8

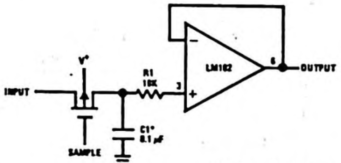
Low Drift Peak Detector


INPUT
R1
R2
LM101A
NC
C1
30pF
C2
30pF
LM101A
OUTPUT
R4
R3
LM101A
POLARITY SIGNAL
D1
LM103
3.9
2
3
6
1
8

$V_{OUT} = \frac{R2}{R1} |V_{IN}|$

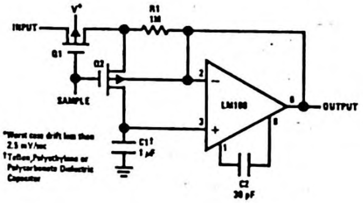
$R2 = \frac{R1\ R4}{R3 + R4}$

Absolute Value Amplifier with Polarity Detector


V+
INPUT
R1
10K
LM102
OUTPUT
C1*
0.1 µF
SAMPLE
3
6

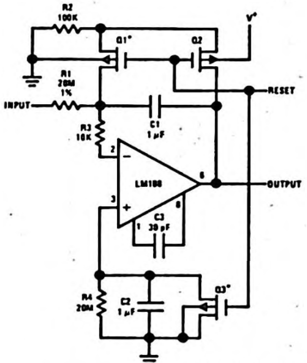
*Polycarbonate-dielectric capacitor

Sample and Hold


V+
INPUT
R1
1M
Q1
Q2
SAMPLE
LM108
OUTPUT
C1†
1 µF
C2
30 pF
2
3
6
1
8

*Worst case drift less than 2.5 mV/sec
†Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

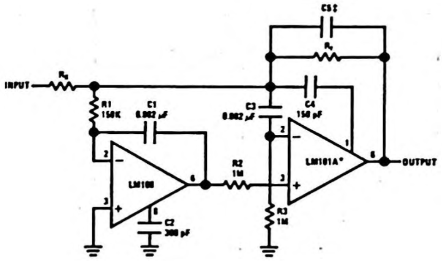
Sample and Hold


R2
100K
V+
Q1*
Q2
R1
20M
1%
INPUT
RESET
C1
1 μF
R3
10K
LM108
OUTPUT
C3
30 pF
R4
20M
C2
1 μF
Q3*

*Q1 and Q3 should not have internal gate-protection diodes.

Worst case drift less than 500 μV/sec over -55°C to +125°C.

Low Drift Integrator

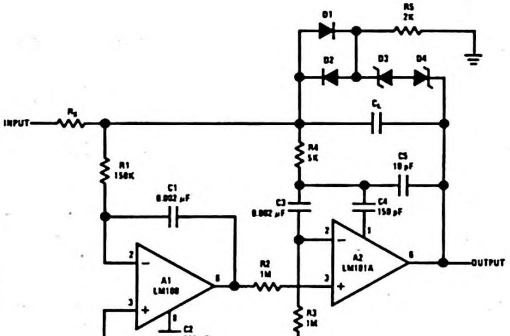

CS‡
Rf
INPUT
RS
R1
150K
C1
0.002 μF
C3
0.002 μF
C4
150 pF
LM108
LM101A*
R2
1M
R3
1M
C2
300 pF
OUTPUT

* In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

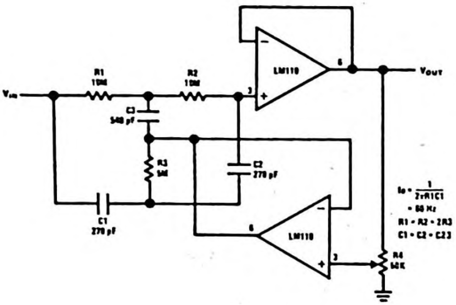
† Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

‡ $CS = \frac{6 \times 10^{-8}}{R_f}$

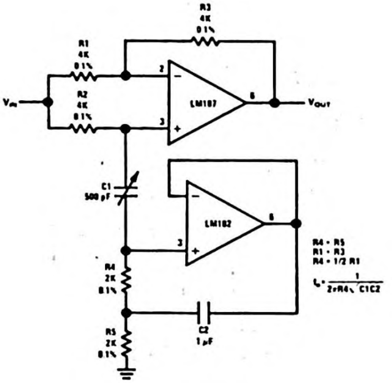
Fast† Summing Amplifier with Low Input Current


D1
R5
2K
D2
D3
D4
CL
INPUT
RS
R1
150K
R4
5K
C5
10 pF
C1
0.002 μF
C3
0.002 μF
C4
150 pF
A1
LM108
A2
LM101A
R2
1M
R3
1M
C2
300 pF
OUTPUT

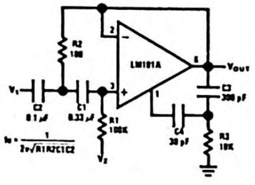
Fast Integrator with Low Input Current


R1
10M
R2
10M
LM110
6
V_{OUT}
V_{IN}
3
C3
540 pF
R3
5M
C2
270 pF
C1
270 pF
6
LM110
3
R4
50K
$f_O = \frac{1}{2\pi R1C1}$
$= 60$ Hz
R1 = R2 = 2R3
C1 = C2 = C3/2

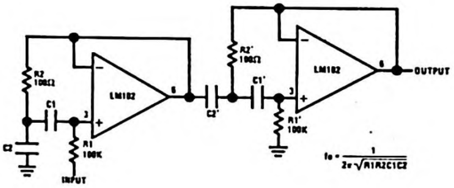
Adjustable Q Notch Filter


R3
4K
0.1%
R1
4K
0.1%
2
LM107
6
V_{OUT}
V_{IN}
R2
4K
0.1%
3
C1
500 pF
LM102
6
3
R4
2K
0.1%
R5
2K
0.1%
C2
1 µF
R4 = R5
R1 = R3
R4 = 1/2 R1
$f_O = \frac{1}{2\pi R4\sqrt{C1C2}}$

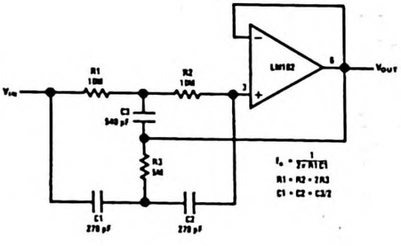
Easily Tuned Notch Filter


R2
100
2
LM101A
6
V_{OUT}
V_1
C2
0.1 µF
C1
0.33 µF
3
1
C3
300 pF
R1
100K
C4
30 pF
R3
10K
V_2
$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$

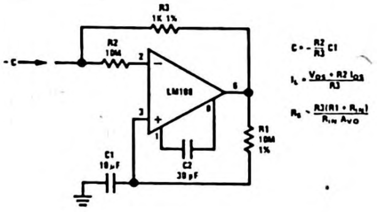
Tuned Circuit


R2
100Ω
LM102
6
C1
3
C2
R1
100K
INPUT
C2'
R2'
100Ω
C1'
3
LM102
6
OUTPUT
R1'
100K
$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$

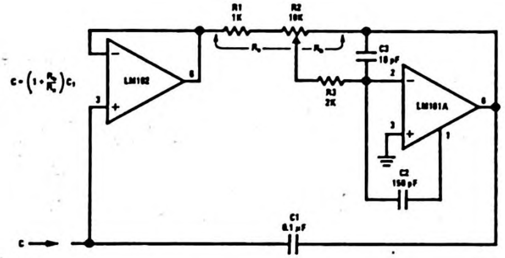
Two-Stage Tuned Circuit


V_{IN}
R1
10M
R2
10M
LM102
6
V_{OUT}
3
C3
540 pF
R3
5M
C1
270 pF
C2
270 pF
$f_o = \frac{1}{2\pi R1C1}$
R1 = R2 = 2R3
C1 = C2 = C3/2

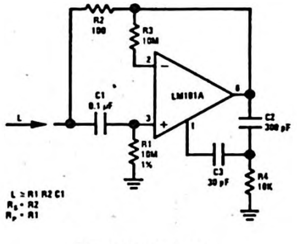
High Q Notch Filter


R3
1K 1%
R2
10M
-C
2
LM108
6
3
8
1
R1
10M
1%
C1
10 µF
C2
30 pF
$C = -\frac{R2}{R3}C1$
$I_L = \frac{V_{OS} + R2\,I_{OS}}{R3}$
$R_S = \frac{R3(R1 + R_{IN})}{R_{IN}\,A_{VO}}$

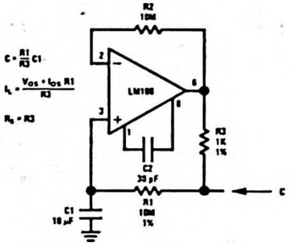
Negative Capacitance Multiplier


C = (1 + Rb/Ra) C1
R1
1K
R2
10K
Ra
Rb
C3
10 pF
LM102
6
3
2
R3
2K
LM101A
6
3
1
C2
150 pF
C1
0.1 μF
C

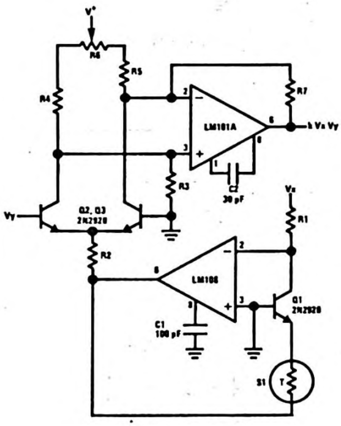
Variable Capacitance Multiplier


R2
100
R3
10M
2
LM101A
6
L
C1
0.1 μF
3
1
C2
300 pF
R1
10M
1%
C3
30 pF
R4
10K
L ≥ R1 R2 C1
RS = R2
RP = R1

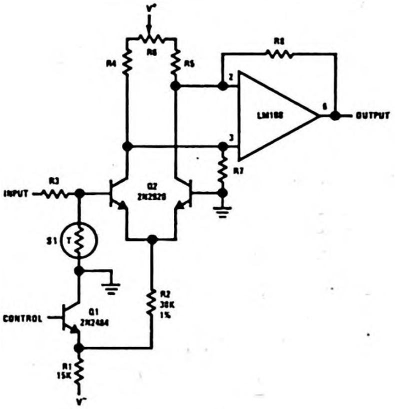
Simulated Inductor


R2
10M
C = R1/R3 C1
IL = (VOS + IOS R1)/R3
RS = R3
2
LM108
6
3
8
1
R3
1K
1%
C2
30 pF
R1
10M
1%
C1
10 μF
C

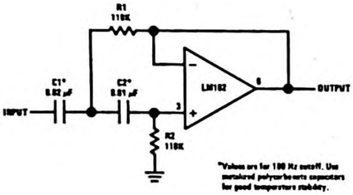
Capacitance Multiplier


V+
R6
R5
R4
2
LM101A
6
R7
k Vx Vy
3
8
1
R3
C2
30 pF
Vx
Vy
Q2, Q3
2N2920
R1
R2
2
6
LM108
8
3
Q1
2N2920
C1
100 pF
S1
T

Two Quadrant Multiplier

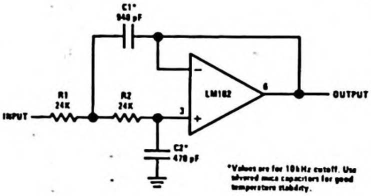

V+
R8
R4
R6
R5
2
LM108
6
OUTPUT
3
R7
R3
INPUT
Q2
2N2920
S1
T
R2
30K
1%
CONTROL
Q1
2N2484
R1
15K
V−

Voltage Controlled Gain Circuit


R1
110K
C1*
0.02 µF
C2*
0.01 µF
INPUT
R2
110K
LM102
3
6
OUTPUT

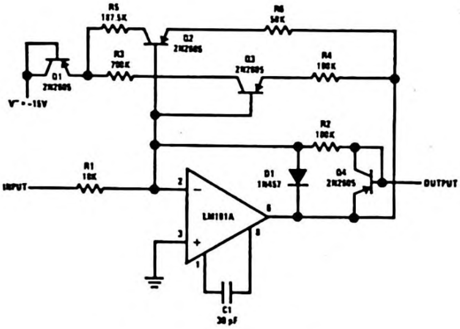
*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

High Pass Active Filter

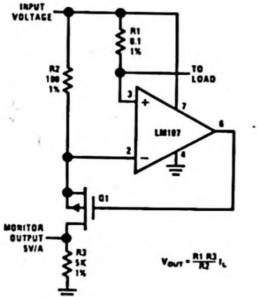

C1*
940 pF
R1
24K
R2
24K
INPUT
C2*
470 pF
LM102
3
6
OUTPUT

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

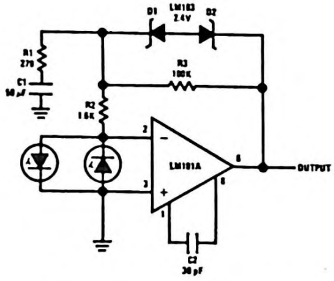
Low Pass Active Filter


R5
187.5K
R6
50K
Q2
2N2905
R3
700K
Q3
2N2905
R4
100K
Q1
2N2905
V⁻ = -15V
R2
100K
R1
10K
INPUT
D1
1N457
Q4
2N2905
OUTPUT
LM101A
2
3
6
8
1
C1
30 pF

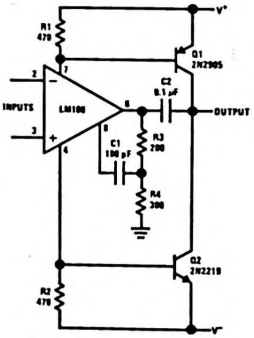
Nonlinear Operational Amplifier with Temperature Compensated Breakpoints


INPUT
VOLTAGE
R1
0.1
1%
TO
LOAD
R2
100
1%
LM107
3
2
7
6
4
Q1
MONITOR
OUTPUT
5V/A
R3
5K
1%
$V_{OUT} = \frac{R1\,R3}{R2} I_L$

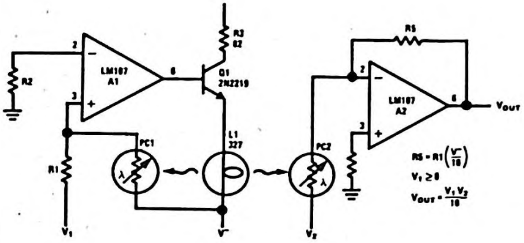
Current Monitor


D1
LM103
2.4V
D2
R1
270
C1
50 µF
R3
100K
R2
15K
LM101A
2
3
6
8
1
OUTPUT
C2
30 pF

Saturating Servo Preamplifier with Rate Feedback


V⁺
R1
470
Q1
2N2905
C2
0.1 µF
INPUTS
LM108
2
3
7
6
8
4
OUTPUT
C1
100 pF
R3
200
R4
300
Q2
2N2219
R2
470
V⁻

Power Booster

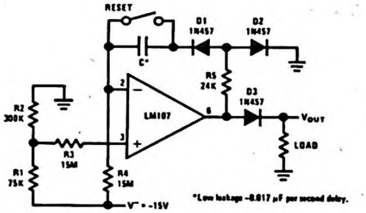

V+
R3
82
R5
2
LM107
A1
6
Q1
2N2219
LM107
A2
6
VOUT
R2
3
3
L1
327
PC1
PC2
R1
λ
λ
V1
V−
V2

$R5 = R1\left(\frac{V^-}{10}\right)$

$V_1 \geq 0$

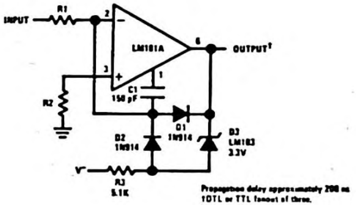
$V_{OUT} = \frac{V_1 V_2}{10}$

Analog Multiplier


RESET
D1
1N457
D2
1N457
C*
R5
24K
2
D3
1N457
R2
300K
LM107
6
VOUT
3
R3
15M
LOAD
R1
75K
R4
15M
V− = −15V

*Low leakage –0.017 µF per second delay.

Long Interval Timer


INPUT
R1
2
LM101A
6
OUTPUT†
3
1
C1
150 pF
R2
D1
1N914
D2
1N914
D3
LM103
3.3V
V−
R3
5.1K

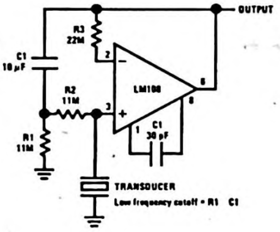
Propagation delay approximately 200 ns

†DTL or TTL fanout of three.

Minimize stray capacitance

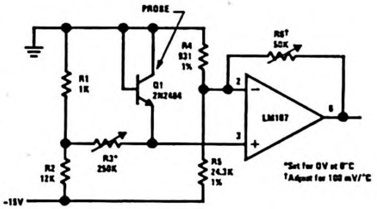
Pin 8

Fast Zero Crossing Detector


OUTPUT
R3
22M
C1
10 µF
2
LM108
6
R2
11M
3
8
1
C1
30 pF
R1
11M
TRANSDUCER

Low frequency cutoff = R1 C1

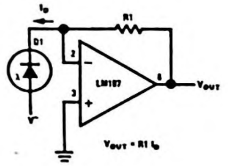
Amplifier for Piezoelectric Transducer


PROBE
R4
831
1%
R6†
50K
R1
1K
Q1
2N2484
2
LM107
6
3
R3*
250K
R2
12K
R5
24.3K
1%
−15V

*Set for 0V at 0°C

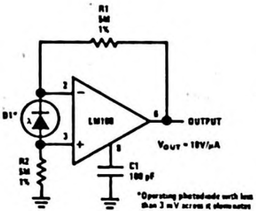
†Adjust for 100 mV/°C

Temperature Probe



I_D
R1
D1
2
3
6
LM107
V_{OUT}
V^-
$V_{OUT} = R1\ I_D$

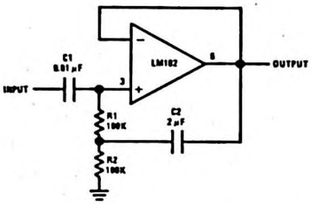
Photodiode Amplifier



R1
5M
1%
2
3
6
8
D1*
LM108
OUTPUT
$V_{OUT} = 10V/\mu A$
R2
5M
1%
C1
100 pF

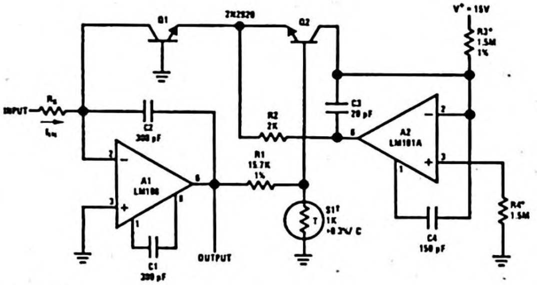
*Operating photodiode with less than 3 mV across it eliminates leakage currents.

Photodiode Amplifier



LM102
6
3
OUTPUT
INPUT
C1
0.01 µF
R1
100K
R2
100K
C2
2 µF

High Input Impedance AC Follower



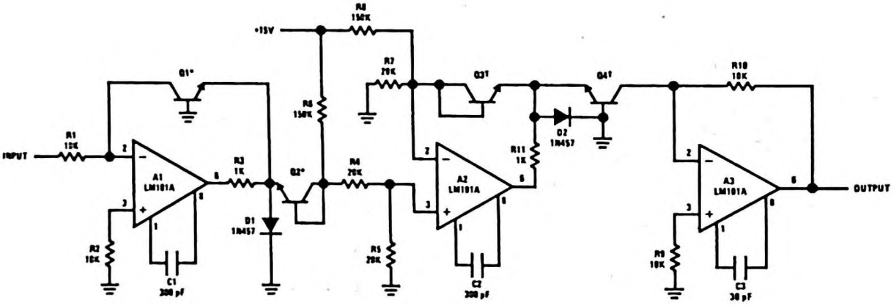
Q1
2N2920
Q2
$V^+ = 15V$
R3*
1.5M
1%
INPUT
R_S
I_{IN}
C2
300 pF
C3
20 pF
R2
2K
A2
LM101A
2
6
3
1
A1
LM108
6
8
3
2
1
R1
15.7K
1%
S1†
1K
+0.3%/°C
R4*
1.5M
C4
150 pF
C1
300 pF
OUTPUT

$10\ nA < I_{IN} < 1\ mA$
Sensitivity is 1V per decade.

†Available from Tel Labs, Inc., Manchester, N.H., Type Q81.

*Determines current for zero crossing on output. 10 µA as shown.

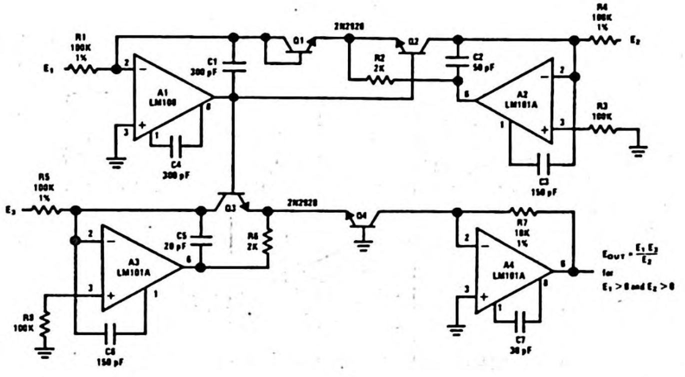
Temperature Compensated Logarithmic Converter



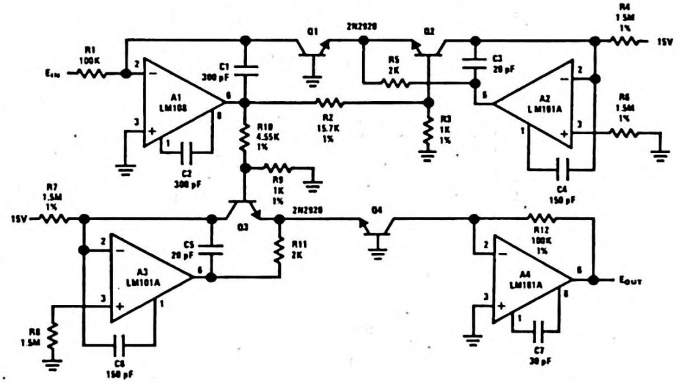
+15V
R8
150K
R7
20K
Q3†
Q4†
R10
10K
Q1*
R6
150K
INPUT
R1
10K
A1
LM101A
R3
1K
Q2*
R4
20K
D1
1N457
R2
10K
C1
300 pF
R5
20K
A2
LM101A
C2
300 pF
R11
1K
D2
1N457
A3
LM101A
R9
10K
C3
30 pF
OUTPUT

*†2N3728 matched pairs

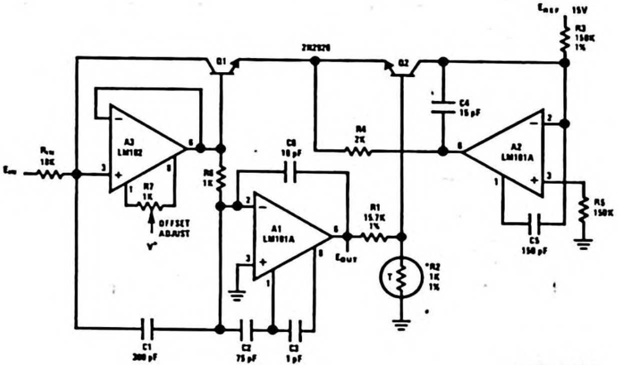
Root Extractor


R1
100K
1%
E_1
2
3
A1
LM108
C1
300 pF
6
8
1
C4
300 pF
Q1
2N2920
Q2
R2
2K
C2
50 pF
R4
100K
1%
E_2
A2
LM101A
2
6
1
3
R3
100K
C3
150 pF
R5
100K
1%
E_3
2
3
A3
LM101A
C5
20 pF
6
1
R8
100K
C6
150 pF
Q3
2N2920
R6
2K
Q4
R7
10K
1%
2
3
A4
LM101A
6
8
1
C7
30 pF
$E_{OUT} = \frac{E_1 E_3}{E_2}$
for
$E_1 > 0$ and $E_2 > 0$

Multiplier/Divider


R1
100K
E_{IN}
2
3
A1
LM108
C1
300 pF
6
8
1
C2
300 pF
Q1
2N2920
Q2
R5
2K
R2
15.7K
1%
R3
1K
1%
R10
4.55K
1%
R9
1K
1%
C3
20 pF
R4
1.5M
1%
15V
A2
LM101A
2
5
1
3
R6
1.5M
1%
C4
150 pF
R7
1.5M
1%
15V
2
3
A3
LM101A
C5
20 pF
6
1
R8
1.5M
C6
150 pF
Q3
2N2920
R11
2K
Q4
R12
100K
1%
2
3
A4
LM101A
6
8
1
C7
30 pF
E_{OUT}

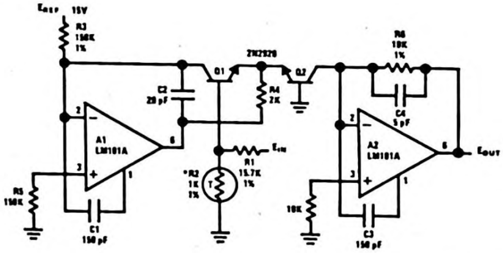
Cube Generator



E_{REF} 15V
R3 150K 1%
2N2920
Q1
Q2
C4 15 pF
A3 LM102
R_{IN} 10K
E_{IN}
R7 1K
OFFSET ADJUST
V⁺
R6 1K
C6 10 pF
R4 2K
A2 LM101A
A1 LM101A
R1 15.7K 1%
E_{OUT}
*R2 1K 1%
T
R5 150K
C5 150 pF
C1 300 pF
C2 75 pF
C3 1 pF
1
2
3
6
8

*Tel Labs Type Q81
Manchester, N.H.

Fast Log Generator



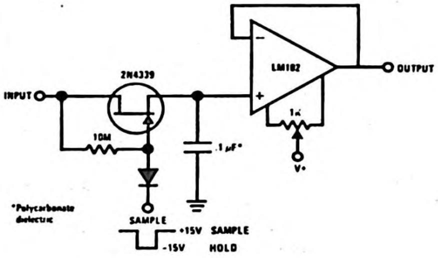
E_{REF} 15V
R3 150K 1%
2N2920
Q1
Q2
C2 20 pF
R4 2K
R6 10K 1%
C4 5 pF
A1 LM101A
A2 LM101A
E_{IN}
R1 15.7K 1%
*R2 1K 1%
T
E_{OUT}
R5 150K
10K
C1 150 pF
C3 150 pF
1
2
3
6

*Tel Labs Type Q81
Manchester, N.H.

Anti-log Generator

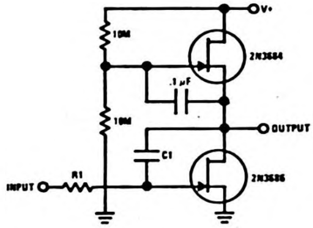
FET Circuit Applications

National Semiconductor
Application Note 32
February 1970


INPUT
2N4339
10M
LM102
OUTPUT
1k
V+
.1 µF*
*Polycarbonate dielectric
SAMPLE
+15V SAMPLE
-15V HOLD

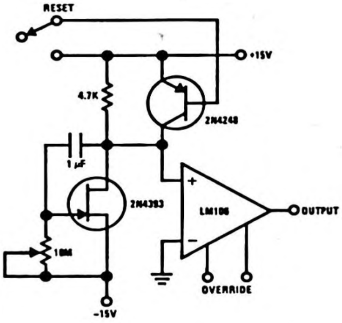
Sample and Hold With Offset Adjustment

The 2N4339 JFET was selected because of its low I_{GSS} (<100 pA), very-low $I_{D(OFF)}$ (<50 pA) and low pinchoff voltage. Leakages of this level put the burden of circuit performance on clean, solder-resin free, low leakage circuit layout.


V+
10M
2N3684
.1 µF
10M
OUTPUT
C1
R1
INPUT
2N3686

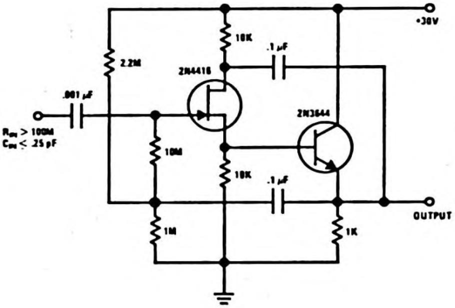
JFET AC Coupled Integrator

This circuit utilizes the "µ-amp" technique to achieve very high voltage gain. Using C_1 in the circuit as a Miller integrator, or capacitance multiplier, allows this simple circuit to handle very long time constants.


RESET
+15V
4.7K
2N4248
1 µF
2N4393
LM106
OUTPUT
10M
-15V
OVERRIDE

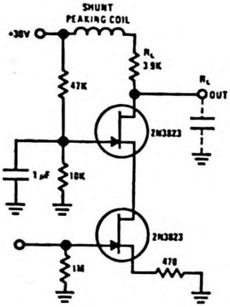
Long Time Comparator

The 2N4393 is operated as a Miller integrator. The high Y_{fs} of the 2N4393 (over 12,000 µmhos @ 5 mA) yields a stage gain of about 60. Since the equivalent capacitance looking into the gate is C times gain and the gate source resistance can be as high as 10 MΩ, time constants as long as a minute can be achieved.


+30V
10K
.1 µF
2.2M
2N4416
.001 µF
Rin > 100M
Cin ≤ .25 pF
2N3644
10M
10K
.1 µF
OUTPUT
1M
1K

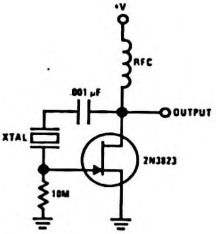
Ultra-High Z_{IN} AC Unity Gain Amplifier

Nothing is left to chance in reducing input capacitance. The 2N4416, which has low capacitance in the first place, is operated as a source follower with bootstrapped gate bias resistor and drain. Any input capacitance you get with this circuit is due to poor layout techniques.


SHUNT
PEAKING COIL
+30V
R_L
3.9K
47K
R_L
OUT
2N3823
1 µF
10K
2N3823
470
1M

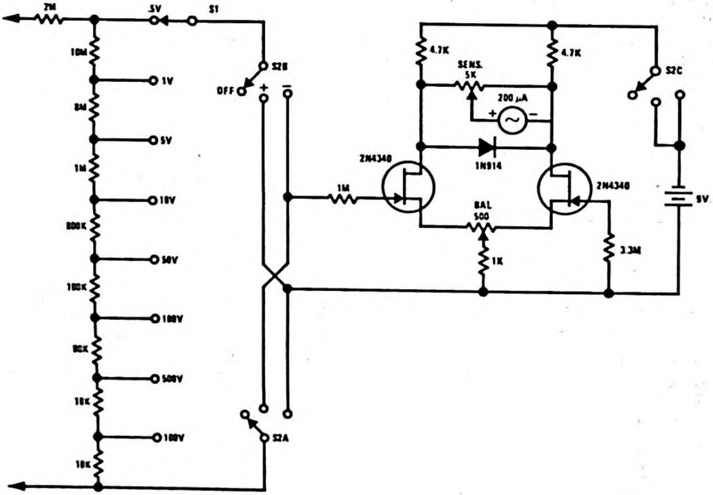
FET Cascode Video Amplifier

The FET cascode video amplifier features very low input loading and reduction of feedback to almost zero. The 2N3823 is used because of its low capacitance and high Y_{fs}. Bandwidth of this amplifier is limited by R_L and load capacitance.


+V
RFC
.001 µF
OUTPUT
XTAL
2N3823
10M

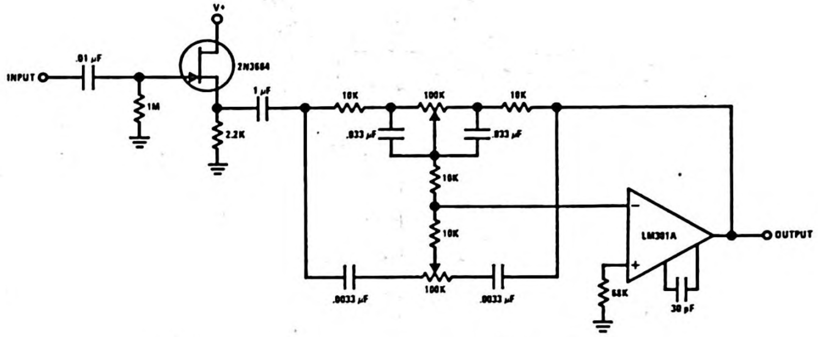
JFET Pierce Crystal Oscillator

The JFET Pierce crystal oscillator allows a wide frequency range of crystals to be used without circuit modification. Since the JFET gate does not load the crystal, good Q is maintained thus insuring good frequency stability.


2M
.5V
S1
10M
1V
8M
5V
1M
10V
800K
50V
100K
100V
80K
500V
10K
1000V
10K
S2B
OFF
+
−
S2A
4.7K
4.7K
SENS.
5K
200 µA
+
−
1N914
2N4340
2N4340
1M
BAL
500
1K
3.3M
S2C
5V

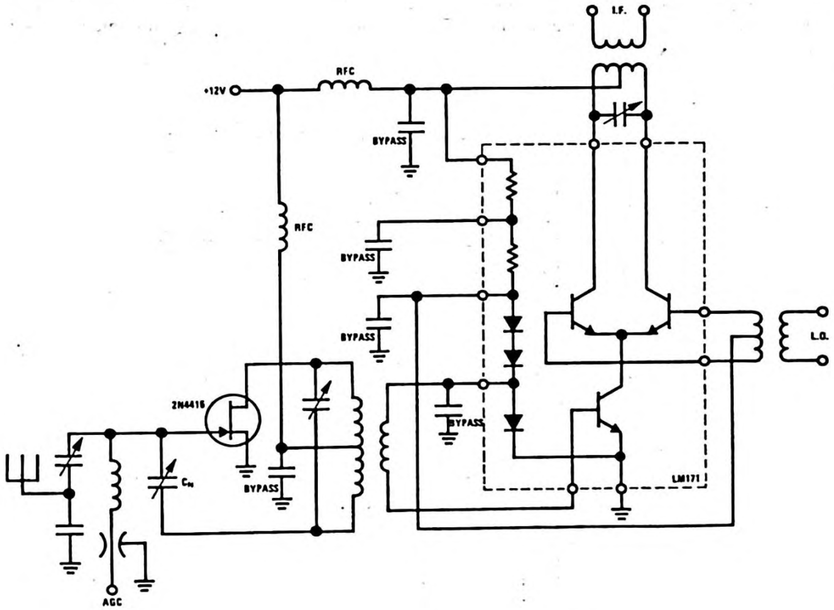
FETVM—FET Voltmeter

This FETVM replaces the function of the VTVM while at the same time ridding the instrument of the usual line cord. In addition, drift rates are far superior to vacuum tube circuits allowing a 0.5 volt full scale range which is impractical with most vacuum tubes. The low-leakage, low-noise 2N4340 is an ideal device for this application.


V+
INPUT
.01 µF
1M
2N3684
1 µF
2.2K
10K
100K
10K
.033 µF
.033 µF
10K
10K
LM301A
OUTPUT
.0033 µF
100K
.0033 µF
68K
30 pF

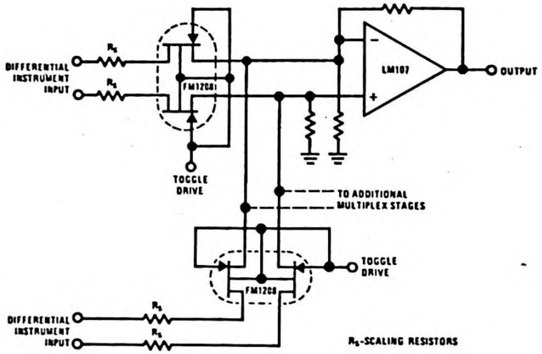
HI-FI Tone Control Circuit (High Z Input)

The 2N3684 JFET provides the function of a high input impedance and low noise characteristics to buffer an op amp-operated feedback type tone control circuit.


I.F.
RFC
+12V
BYPASS
RFC
BYPASS
BYPASS
L.O.
2N4416
BYPASS
C_N
BYPASS
LM171
AGC

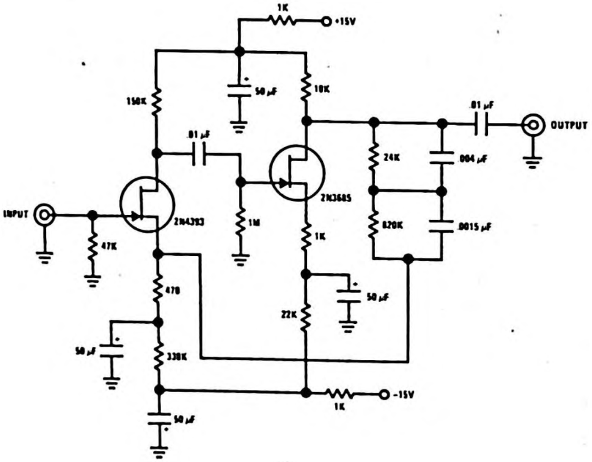
100 MHz Converter

The 2N4416 JFET will provide noise figures of less than 3 dB and power gain of greater than 20 dB. The JFETs outstanding low crossmodulation and low intermodulation distortion provides an ideal characteristic for an input stage. The output feeds into an LM171 used as a balanced mixer. This configuration greatly reduces L.O. radiation both into the antenna and into the I.F. strip and also reduces RF signal feedthrough.


DIFFERENTIAL INSTRUMENT INPUT
R_s
R_s
FM1208
TOGGLE DRIVE
LM107
OUTPUT
TO ADDITIONAL MULTIPLEX STAGES
TOGGLE DRIVE
FM1208
DIFFERENTIAL INSTRUMENT INPUT
R_s
R_s
R_s-SCALING RESISTORS

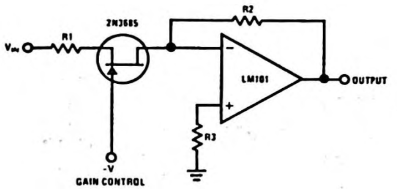
Differential Analog Switch

The FM1208 monolithic dual is used in a differential multiplexer application where $R_{DS(ON)}$ should be closely matched. Since $R_{DS(ON)}$ for the monolithic dual tracks at better than ±1% over wide temperature ranges (–25 to +125°C), this makes it an unusual but ideal choice for an accurate multiplexer. This close tracking greatly reduces errors due to common mode signals.


1K
+15V
150K
50 µF
10K
.01 µF
.01 µF
OUTPUT
24K
.004 µF
2N3685
INPUT
2N4393
1M
820K
.0015 µF
47K
1K
470
50 µF
22K
50 µF
330K
-15V
1K
50 µF

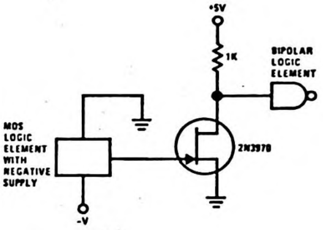
Magnetic-Pickup Phono Preamplifier

This preamplifier provides proper loading to a reluctance phono cartridge. It provides approximately 35 dB of gain at 1 kHz (2.2 mV input for 100 mV output), it features S + N/N ratio of better than –70 dB (referenced to 10 mV input at 1 kHz) and has a dynamic range of 84 dB (referenced to 1 kHz). The feedback provides for RIAA equalization.


2N3685
R1
R2
V_IN
LM101
OUTPUT
R3
-V
GAIN CONTROL

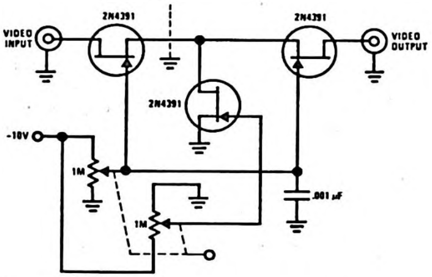
Variable Attenuator

The 2N3685 acts as a voltage variable resistor with an $R_{DS(ON)}$ of 800Ω max. The 2N3685 JFET will have linear resistance over several decades of resistance providing an excellent electronic gain control.


+5V
1K
BIPOLAR LOGIC ELEMENT
MOS LOGIC ELEMENT WITH NEGATIVE SUPPLY
2N3970
-V

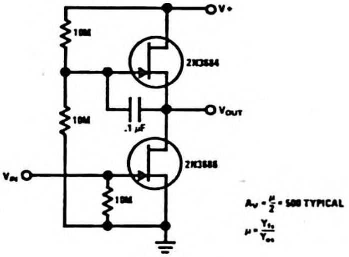
Negative to Positive Supply Logic Level Shifter

This simple circuit provides for level shifting from any logic function (such as MOS) operating from minus to ground supply to any logic level (such as TTL) operating from a plus to ground supply. The 2N3970 provides a low $r_{ds(ON)}$ and fast switching times.


2N4391
2N4391
2N4391
VIDEO INPUT
VIDEO OUTPUT
-10V
1M
1M
.001 μF

Voltage Controlled Variable Gain Amplifier

The 2N4391 provides a low $R_{DS(ON)}$ (less than 30Ω). The tee attenuator provides for optimum dynamic linear range for attenuation and if complete turnoff is desired, attenuation of greater than 100 dB can be obtained at 10 MHz providing proper RF construction techniques are employed.

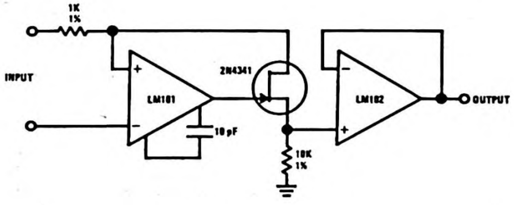

V+
10M
2N3684
V_OUT
10M
.1 μF
2N3686
V_IN
10M

$A_V = \frac{\mu}{2} = 500$ TYPICAL

$\mu = \frac{Y_{fs}}{Y_{os}}$

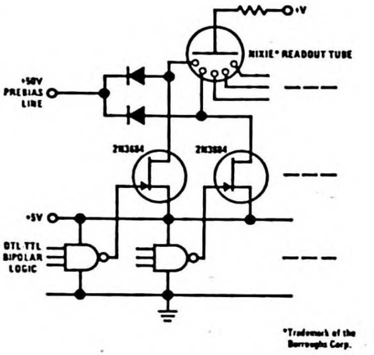
Ultra-High Gain Audio Amplifier

Sometimes called the "JFET μ amp," this circuit provides a very low power, high gain amplifying function. Since μ of a JFET increases as drain current decreases, the lower drain current is, the more gain you get. You do sacrifice input dynamic range with increasing gain, however.


1K
1%
INPUT
LM101
2N4341
10 pF
10K
1%
LM102
OUTPUT

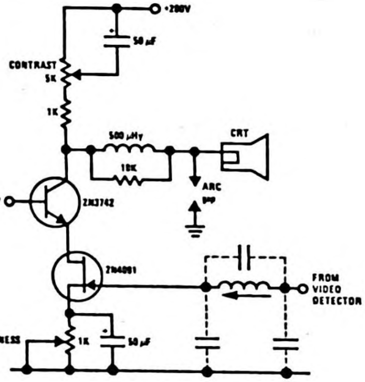
Level-Shifting-Isolation Amplifier

The 2N4341 JFET is used as a level shifter between two op amps operated at different power supply voltages. The JFET is ideally suited for this type of application because $I_D = I_S$.


+V
NIXIE* READOUT TUBE
+50V PREBIAS LINE
2N3684
2N3684
+5V
DTL-TTL BIPOLAR LOGIC
*Trademark of the Burroughs Corp.

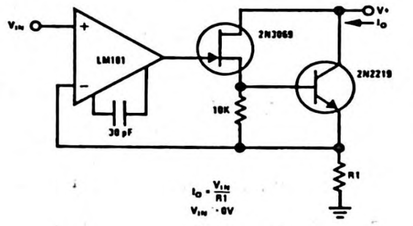
FET Nixie* Drivers

The 2N3684 JFETs are used as Nixie tube drivers. Their V_P of 2-5 volts ideally matches DTL-TTL logic levels. Diodes are used to a +50 volt prebias line to prevent breakdown of the JFETs. Since the 2N3684 is in a TO-72 (4 lead TO-18) package, none of the circuit voltages appear on the can. The JFET is immune to almost all of the failure mechanisms found in bipolar transistors used for this application.


+200V
50 μF
CONTRAST 5K
1K
500 μHy
10K
CRT
ARC GAP
+30V
2N3742
2N4091
FROM VIDEO DETECTOR
BRIGHTNESS
1K
50 μF

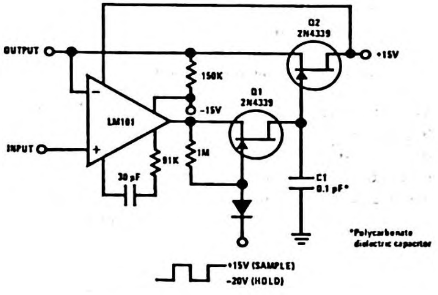
JFET–Bipolar Cascode Circuit

The JFET-Bipolar cascode circuit will provide full video output for the CRT cathode drive. Gain is about 90. The cascode configuration eliminates Miller capacitance problems with the 2N4091 JFET, thus allowing direct drive from the video detector. An m derived filter using stray capacitance and a variable inductor prevents 4.5 MHz sound frequency from being amplified by the video amplifier.


V_{IN}
LM101
30 pF
2N3069
10K
2N2219
V+
I_O
R1
$I_O = \frac{V_{IN}}{R1}$
$V_{IN} \geq 0V$

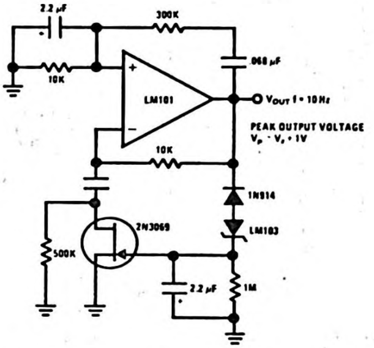
Precision Current Sink

The 2N3069 JFET and 2N2219 bipolar have inherently high output impedance. Using R_1 as a current sensing resistor to provide feedback to the LM101 op amp provides a large amount of loop gain for negative feedback to enhance the true current sink nature of this circuit. For small current values, the 10k resistor and 2N2219 may be eliminated if the source of the JFET is connected to R_1.

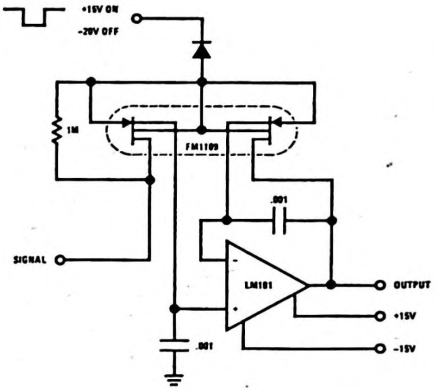

OUTPUT
INPUT
LM101
150K
-15V
1M
91K
30 pF
Q2 2N4339
Q1 2N4339
+15V
C1 0.1 pF*
*Polycarbonate dielectric capacitor
+15V (SAMPLE)
-20V (HOLD)

Low Drift Sample and Hold

The JFETs, Q_1 and Q_2, provide complete buffering to C_1, the sample and hold capacitor. During sample, Q_1 is turned on and provides a path, $r_{ds(ON)}$, for charging C_1. During hold, Q_1 is turned off thus leaving Q_1 $I_{D(OFF)}$ (<50 pA) and Q_2 I_{GSS} (<100 pA) as the only discharge paths. Q_2 serves a buffering function so feedback to the LM101 and output current are supplied from its source.


2.2 µF
300K
10K
.068 µF
LM101
V_{OUT} f = 10 Hz
PEAK OUTPUT VOLTAGE
V_P = V_Z + 1V
10K
1N914
LM103
2N3069
500K
2.2 µF
1M

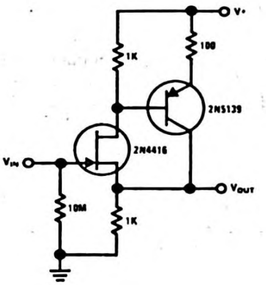
Wein Bridge Sine Wave Oscillator


+15V ON
-20V OFF
1M
FM1109
.001
SIGNAL
LM101
OUTPUT
+15V
-15V
.001

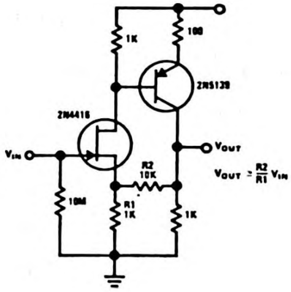
JFET Sample and Hold Circuit

The major problem in producing a low distortion, constant amplitude sine wave is getting the amplifier loop gain just right. By using the 2N3069 JFET as a voltage variable resistor in the amplifier feedback loop, this can be easily achieved. The LM103 zener diode provides the voltage reference for the peak sine wave amplitude; this is rectified and fed to the gate of the 2N3069, thus varying its channel resistance and, hence, loop gain.

The logic voltage is applied simultaneously to the sample and hold JFETs. By matching input impedance and feedback resistance and capacitance, errors due to $r_{ds(ON)}$ of the JFETs is minimized. The inherent matched $r_{ds(ON)}$ and matched leakage currents of the FM1109 monolithic dual greatly improve circuit performance.


V+
1K
100
2N5139
2N4416
V_{IN}
V_{OUT}
10M
1K

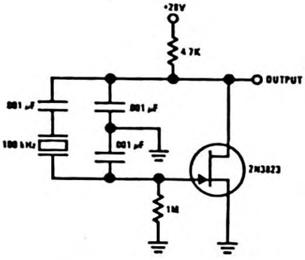
High Impedance Low Capacitance Wideband Buffer


1K
100
2N5139
2N4416
V_{IN}
V_{OUT}
R2
10K
$V_{OUT} \approx \frac{R2}{R1} V_{IN}$
10M
R1
1K
1K

High Impedance Low Capacitance Amplifier

The 2N4416 features low input capacitance which makes this compound-series feedback buffer a wide-band unity gain amplifier.

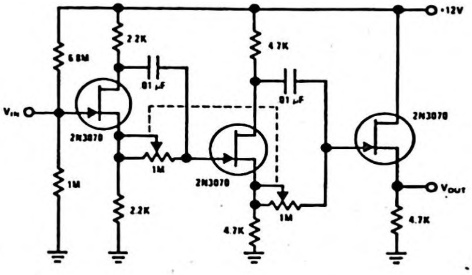
This compound series-feedback circuit provides high input impedance and stable, wide-band gain for general purpose video amplifier applications.



+28V
4.7K
OUTPUT
.001 μF
100 kHz
.001 μF
.001 μF
2N3823
1M

Stable Low Frequency Crystal Oscillator

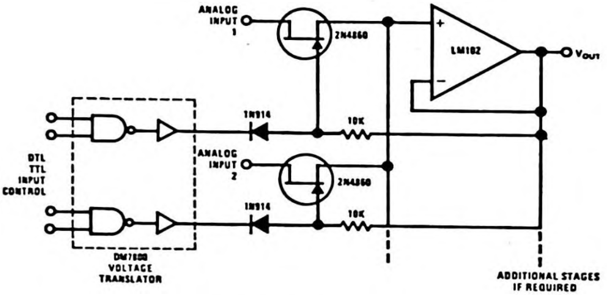
This Colpitts-Crystal oscillator is ideal for low frequency crystal oscillator circuits. Excellent stability is assured because the 2N3823 JFET circuit loading does not vary with temperature.



+12V
6.8M
2.2K
.01 μF
4.7K
.01 μF
V_{IN}
2N3070
1M
2N3070
2N3070
V_{OUT}
1M
2.2K
1M
4.7K
4.7K

0 to 360° Phase Shifter

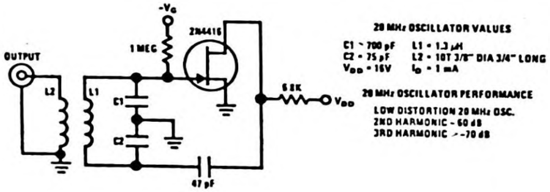
Each stage provides 0° to 180° phase shift. By ganging the two stages, 0° to 360° phase shift is achieved. The 2N3070 JFETs are ideal since they do not load the phase shift networks.



ANALOG INPUT 1
2N4860
LM102
V_{OUT}
1N914
10K
ANALOG INPUT 2
2N4860
DTL TTL INPUT CONTROL
1N914
10K
DM7800 VOLTAGE TRANSLATOR
ADDITIONAL STAGES IF REQUIRED

DTL-TTL Controlled Buffered Analog Switch

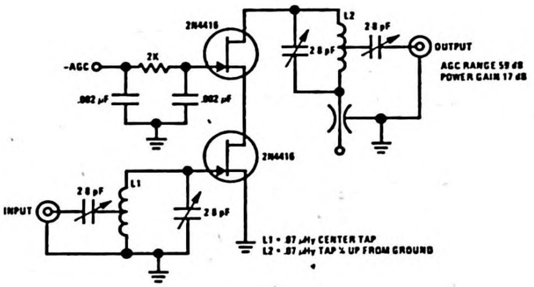
This analog switch uses the 2N4860 JFET for its 25 ohm r_{ON} and low leakage. The LM102 serves as a voltage buffer. This circuit can be adapted to a dual trace oscilloscope chopper. The DM7800 monolithic I.C. provides adequate switch drive controlled by DTL-TTL logic levels.



$-V_G$
2N4416
1 MEG
OUTPUT
L2
L1
C1
C2
6.8K
V_{DD}
47 pF
20 MHz OSCILLATOR VALUES
C1 ~ 700 pF
L1 = 1.3 μH
C2 = 75 pF
L2 = 10T 3/8" DIA 3/4" LONG
V_{DD} = 15V
I_D = 1 mA
20 MHz OSCILLATOR PERFORMANCE
LOW DISTORTION 20 MHz OSC.
2ND HARMONIC - 60 dB
3RD HARMONIC > -70 dB

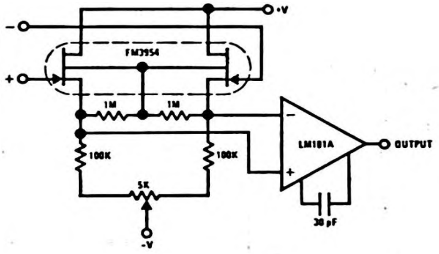
Low Distortion Oscillator

The 2N4416 JFET is capable of oscillating in a circuit where harmonic distortion is very low. The JFET local oscillator is excellent when a low harmonic content is required for a good mixer circuit.


2N4416
-AGC
2K
.002 µF
.002 µF
2N4416
INPUT
2.8 pF
L1
2.8 pF
L2
2.8 pF
2.8 pF
OUTPUT
AGC RANGE 59 dB
POWER GAIN 17 dB
L1 • .07 µHy CENTER TAP
L2 • .07 µHy TAP ¼ UP FROM GROUND

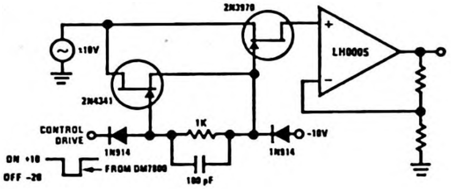
200 MHz Cascode Amplifier

This 200 MHz JFET cascode circuit features low crossmodulation, large-signal handling ability, no neutralization, and AGC controlled by biasing the upper cascode JFET. The only special requirement of this circuit is that I_{DSS} of the upper unit must be greater than that of the lower unit.


+V
−
+
FM3954
1M
1M
100K
100K
5K
-V
LM101A
OUTPUT
30 pF

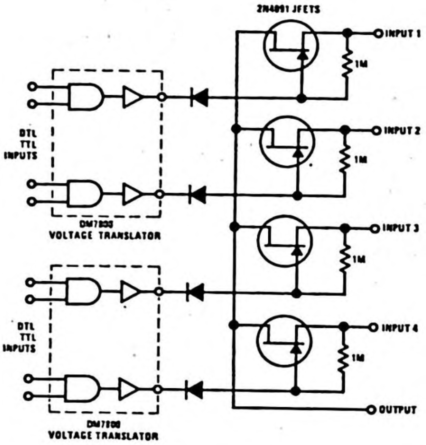
FET Op Amp

The FM3954 monolithic-dual provides an ideal low-offset, low-drift buffer function for the LM101A op amp. The excellent matching characteristics of the FM3954 track well over its bias current range thus improving common mode rejection.


2N3970
±10V
2N4341
LH0005
+
−
CONTROL DRIVE
1N914
1K
1N914
-10V
ON +10
OFF -20
FROM DM7800
100 pF

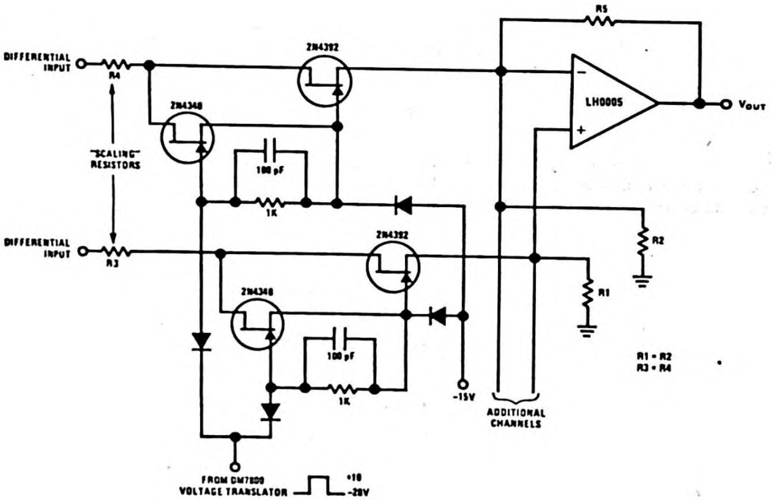
High Toggle Rate High Frequency Analog Switch

This commutator circuit provides low impedance gate drive to the 2N3970 analog switch for both on and off drive conditions. This circuit also approaches the ideal gate drive conditions for high frequency signal handling by providing a low ac impedance for off drive and high ac impedance for on drive to the 2N3970. The LH0005 op amp does the job of amplifying megahertz signals.


2N4091 JFETS
INPUT 1
1M
INPUT 2
1M
INPUT 3
1M
INPUT 4
1M
OUTPUT
DTL
TTL
INPUTS
DM7800
VOLTAGE TRANSLATOR
DTL
TTL
INPUTS
DM7800
VOLTAGE TRANSLATOR

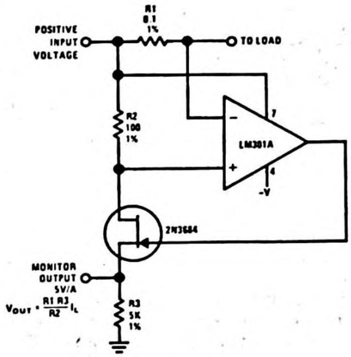
4-Channel Commutator

This 4-channel commutator uses the 2N4091 to achieve low channel ON resistance (<30Ω) and low OFF current leakage. The DM7800 voltage translator is a monolithic device which provides from +10V to −20V gate drive to the JFETs while at the same time providing DTL-TTL logic compatability.


R5
DIFFERENTIAL
INPUT
R4
2N4392
2N4348
"SCALING"
RESISTORS
100 pF
1K
LH0005
VOUT
R2
DIFFERENTIAL
INPUT
R3
2N4392
2N4348
R1
100 pF
1K
-15V
ADDITIONAL
CHANNELS
R1 = R2
R3 = R4
FROM DM7800
VOLTAGE TRANSLATOR
+10
-20V

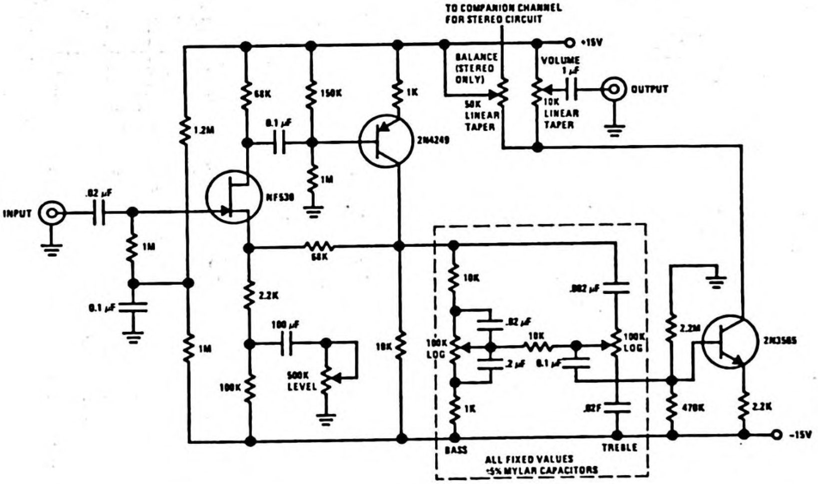
Wide Band Differential Multiplexer

This design allows high frequency signal handling and high toggle rates simultaneously. Toggle rates up to 1 MHz and MHz signals are possible with this circuit.


R1
0.1
1%
POSITIVE
INPUT
VOLTAGE
TO LOAD
R2
100
1%
7
LM301A
4
-V
2N3684
MONITOR
OUTPUT
5V/A
$V_{OUT} = \frac{R1\,R3}{R2} I_L$
R3
5K
1%

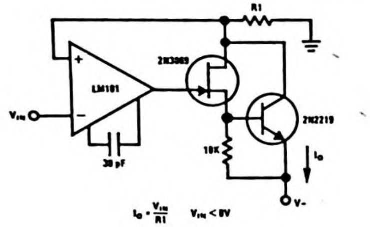
Current Monitor

R_1 senses current flow of a power supply. The JFET is used as a buffer because $I_D = I_S$, therefore the output monitor voltage accurately reflects the power supply current flow.


TO COMPANION CHANNEL
FOR STEREO CIRCUIT
+15V
BALANCE
(STEREO
ONLY)
50K
LINEAR
TAPER
VOLUME
1 µF
10K
LINEAR
TAPER
OUTPUT
68K
150K
1K
1.2M
0.1 µF
2N4249
1M
NF530
INPUT
.02 µF
1M
0.1 µF
68K
2.2K
100 µF
500K
LEVEL
100K
1M
10K
10K
.002 µF
.02 µF
10K
100K
LOG
100K
LOG
.2 µF
0.1 µF
1K
.02F
2.2M
2N3565
470K
2.2K
-15V
BASS
TREBLE
ALL FIXED VALUES
±5% MYLAR CAPACITORS

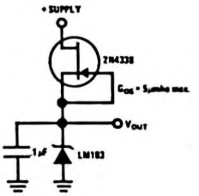
Low Cost High Level Preamp and Tone Control Circuit

This preamp and tone control uses the JFET to its best advantage; as a low noise high input impedance device. All device parameters are non-critical yet the circuit achieves harmonic distortion levels of less than .05% with a S/N ratio of over 85 dB. The tone controls allow 18 dB of cut and boost; the amplifier has a 1 volt output for 100 mV input at maximum level.


R1
2N3069
LM101
V_{IN}
30 pF
2N2219
10K
I_O
V-
$I_O = \frac{V_{IN}}{R1}$
$V_{IN} < 0V$

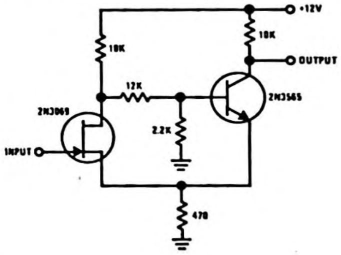
Precision Current Source

The 2N3069 JFET and 2N2219 bipolar serve as voltage isolation devices between the output and the current sensing resistor, R_1. The LM101 provides a large amount of loop gain to assure that the circuit acts as a current source. For small values of current, the 2N2219 and 10k resistor may be eliminated with the output appearing at the source of the 2N3069.


+SUPPLY
2N4338
G_{OS} = 5μmho max.
V_{OUT}
1μF
LM103

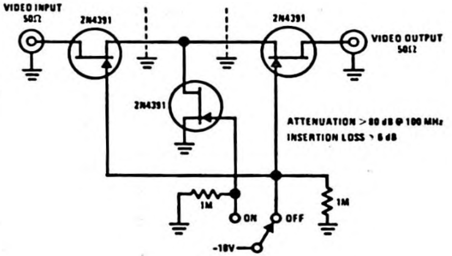
Low Power Regulator Reference

This simple reference circuit provides a stable voltage reference almost totally free of supply voltage hash. Typical power supply rejection exceeds 100 dB.


+12V
10K
OUTPUT
10K
12K
2N3565
2N3069
2.2K
INPUT
470

Schmitt Trigger

This Schmitt trigger circuit is "emitter coupled" and provides a simple comparator action. The 2N3069 JFET places very little loading on the measured input. The 2N3565 bipolar is a high h_{FE} transistor so the circuit has fast transition action and a distinct hysteresis loop.


VIDEO INPUT
50Ω
2N4391
2N4391
VIDEO OUTPUT
50Ω
2N4391
ATTENUATION > 80 dB @ 100 MHz
INSERTION LOSS > 6 dB
1M
ON
OFF
1M
-10V

High Frequency Switch

The 2N4391 provides a low on-resistance of 30 ohms and a high off-impedance (<.2 pF) when off. With proper layout and an "ideal" switch, the performance stated above can be readily achieved.

Precision IC Comparator Runs from +5V Logic Supply

National Semiconductor
Application Note 41
October 1970

INTRODUCTION

In digital systems, it is sometimes necessary to convert low level analog signals into digital information. An example of this might be a detector for the illumination level of a photodiode. Another would be a zero crossing detector for a magnetic transducer such as a magnetometer or a shaft-position pickoff. These transducers have low-level outputs, with currents in the low microamperes or voltages in the low millivolts. Therefore, low level circuitry is required to condition these signals before they can drive logic circuits.

A voltage comparator can perform many of these precision functions. A comparator is essentially a high-gain op amp designed for open loop operation. The function of a comparator is to produce a logic "one" on the output with a positive signal between its two inputs or a logic "zero" with a negative signal between the inputs. Threshold detection is accomplished by putting a reference voltage on one input and the signal on the other. Clearly, an op amp can be used as a comparator, except that its response time is in the tens of microseconds which is often too slow for many applications.

A unique comparator design will be described here along with some of its applications in digital systems. Unlike older IC comparators or op amps, it will operate from the same 5V supply as DTL or TTL logic circuits. It will also operate with the single negative supply used with MOS logic. Hence, low level functions can be performed without the extra supply voltages previously required.

The versatility of the comparator along with the minimal circuit loading and considerable precision recommend it for many uses, in digital systems, other than the detection of low level signals. It can be used as an oscillator or multivibrator, in digital interface circuitry and even for low voltage analog circuitry. Some of these applications will also be discussed.

CIRCUIT DESCRIPTION

In order to understand how to use this comparator, it is necessary to look briefly at the circuit configuration. Figure 1 shows a simplified schematic of the device. PNP transistors buffer the differential input stage to get low input currents without sacrificing speed. The PNP's drive a standard NPN differential stage, Q_3 and Q_4. The output of this stage is further amplified by the Q_5-Q_6 pair. This feeds Q_9 which provides additional gain and drives the output stage. Current sources are used to determine the bias currents, so that performance is not greatly affected by supply voltages.

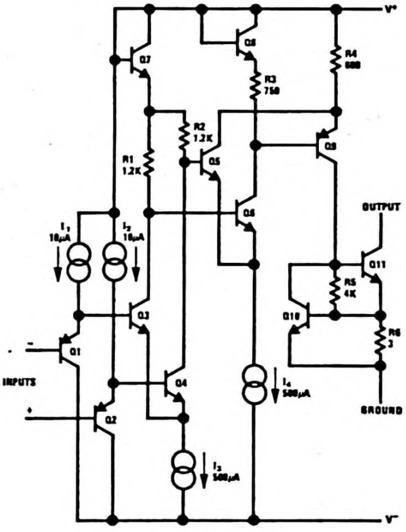


FIGURE 1. Simplified Schematic of the Comparator

The output transistor is Q_{11}, and it is protected by Q_{10} and R_6 which limit the peak output current. The output lead, since it is not connected to any other point in the circuit, can either be returned to the positive supply through a pull-up resistor or switch loads that are connected to a voltage higher than the positive supply voltage. The circuit will operate from a single supply if the negative supply lead is connected to ground. However, if a negative supply is available, it can be used to increase the input common mode range.

Table 1 summarizes the performance of the comparator when operating from a 5V supply. The circuit will work with supply voltages up to ±15V with a corresponding increase in the input voltage range. Other characteristics are essentially unchanged at the higher voltages.

Table 1. Important Electrical Characteristics of the LM111 Comparator when Operating from Single, 5V Supply ($T_A = 25°C$).

Parameter	Limits			Units
	Min	Typ	Max	
Input Offset Voltage		0.7	3	mV
Input Offset Current		4	10	nA
Input Bias Current		60	100	nA
Voltage Gain		100		V/mV
Response Time		200		ns
Common Mode Range	0.3		3.8	V
Output Voltage Swing			50	V
Output Current			50	mA
Fan Out (DTL/TTL)	8			
Supply Current		3	5	mA

LOW LEVEL APPLICATIONS

A circuit that will detect zero crossing in the output of a magnetic transducer within a fraction of a millivolt is shown in Figure 2. The magnetic pickup is connected between the two inputs of the comparator. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the IC. The output will directly drive DTL or TTL. The exact value of the pull up resistor, R_5, is determined by the speed required from the circuit since it must drive any capacitive loading for positive-going output signals. An optional offset-balancing circuit using R_3 and R_4 is included in the schematic.

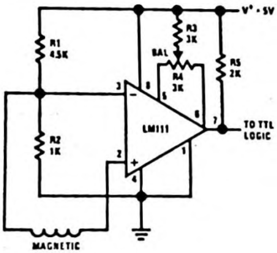


FIGURE 2. Zero Crossing Detector for Magnetic Transducer

Figure 3 shows a connection for operating with MOS logic. This is a level detector for a photodiode that operates off a −10V supply. The output changes state when the diode current reaches 1 μA. Even at this low current, the error contributed by the comparator is less than 1%.

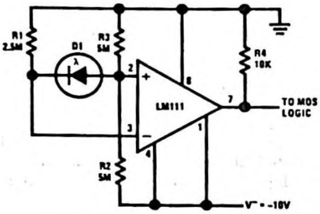


FIGURE 3. Level Detector for Photodiode

Higher threshold currents can be obtained by reducing R_1, R_2 and R_3 proportionally. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

The circuit in Figure 3 can, of course, be adapted to work with a 5V supply. At any rate, the accuracy of the circuit will depend on the supply-voltage regulation, since the reference is derived from the supply. Figure 4 shows a method of making performance independent of supply voltage. D_1 is a temperature-compensated reference diode with a 1.23V breakdown voltage. It acts as a shunt regulator and delivers a stable voltage to the comparator. When the diode current is large enough (about 10 μA) to make the voltage drop across R_3 equal to the breakdown voltage

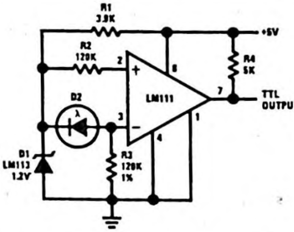


FIGURE 4. Precision Level Detector for Photodiode

of D_1, the output will change state. R_2 has been added to make the threshold error proportional to the offset current of the comparator, rather than the bias current. It can be eliminated if the bias current error is not considered significant.

A zero crossing detector that drives the data input of MOS logic is shown in Figure 5. Here, both a positive supply and the −10V supply for MOS circuits are used. Both supplies are required for the circuit to work with zero common-mode voltage. An alternate balancing scheme is also shown in the schematic. It differs from the circuit in Figure 2 in that it raises the input-stage current by a factor of three. This increases the rate at which the input voltage follows rapidly-changing signals from 7V/μs to 18V/μs. This increased common-mode slew can be obtained without the balancing potentiometer by shorting both balance terminals to the positive-supply terminal. Increased input bias current is the price that must be paid for the faster operation.

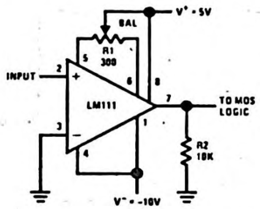


FIGURE 5. Zero Crossing Detector Driving MOS Logic

DIGITAL INTERFACE CIRCUITS

Figure 6 shows an interface between high-level logic and DTL or TTL. The input signal, with 0V and 30V logic states is attenuated to 0V and 5V by R_1 and R_2. R_3 and R_4 set up a 2.5V threshold level for the comparator so that it switches when the input goes through 15V. The response time of the circuit can be controlled with C_1, if desired, to make it insensitive to fast noise spikes. Because of the low error currents of the LM111, it is possible to get input impedances even higher than the 300 kΩ obtained with the indicated resistor values.

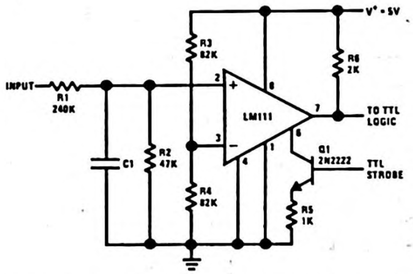


FIGURE 6. Circuit for Transmitting Data Between High-Level Logic and TTL

The comparator can be strobed, as shown in Figure 6, by the addition of Q_1 and R_5. With a logic one on the base of Q_1, approximately 2.5 mA is drawn out of the strobe terminal of the LM111, making the output high independent of the input signal.

Sometimes it is necessary to transmit data between digital equipments, yet maintain a high degree of electrical isolation. Normally, this is done with a transformer. However, transformers have problems with low-duty-cycle pulses since they do not preserve the dc level.

The circuit in Figure 7 is a more satisfactory method of obtaining isolation. At the transmitting end, a TTL gate drives a gallium-arsenide light-emitting diode. The light output is optically coupled to a silicon photodiode, and the comparator detects the photodiode output. The optical coupling makes possible electrical isolation in the thousands of megohms at potentials in the thousands of volts.

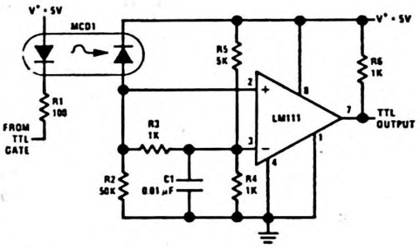


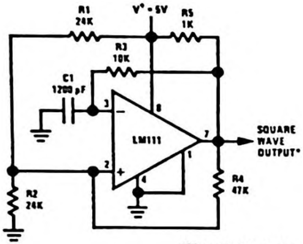
FIGURE 7. Data Transmission System with Near-Infinite Ground Isolation

The maximum data rate of this circuit is 1 MHz. At lower rates (~200 kHz) R_3 and C_1 can be eliminated.

MULTIVIBRATORS AND OSCILLATORS

The free-running multivibrator in Figure 8 is another example of the versatility of the comparator. The inputs are biased within the common mode range by R_1 and R_2. DC stability, which insures starting, is provided by negative feedback through R_3. The negative feedback is reduced at high frequencies by C_1. At some frequency, the positive feedback through R_4 will be greater than the negative feedback; and the circuit will oscillate. For the component values shown, the circuit delivers a 100 kHz square wave output. The frequency can be changed by varying C_1 or by adjusting R_1 through R_4, while keeping their ratios constant.

Because of the low input current of the comparator, large circuit impedances can be used. Therefore, low frequencies can be obtained with relatively-small capacitor values: it is no problem to get down to 1 Hz using a 1 μF capacitor. The speed of the comparator also permits operation at frequencies above 100 kHz.


R1
24K
V⁺ = 5V
R5
1K
R3
10K
C1
1200 pF
LM111
3
2
8
7
1
4
SQUARE
WAVE
OUTPUT*
R2
24K
R4
47K

*TTL or DTL Fanout of two.

FIGURE 8. Free-Running Multivibrator

The frequency of oscillation depends almost entirely on the resistance and capacitor values because of the precision of the comparator. Further, the frequency changes by only 1% for a 10% change in supply voltage. Waveform symmetry is also good, but the symmetry can be varied by changing the ratio of R_1 to R_2.

A crystal-controlled oscillator that can be used to generate the clock in slower digital systems is shown in Figure 9. It is similar to the free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when transmission through the crystal is at a maximum, so the crystal operates in its series-resonant mode. The high input impedance of the comparator and the isolating capacitor, C_2, minimize loading of the crystal and contribute to frequency stability. As shown, the oscillator delivers a 100 kHz square-wave output.

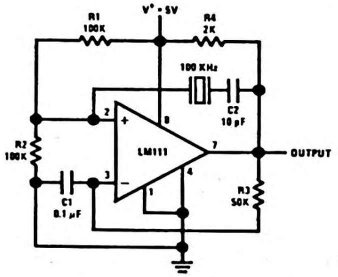
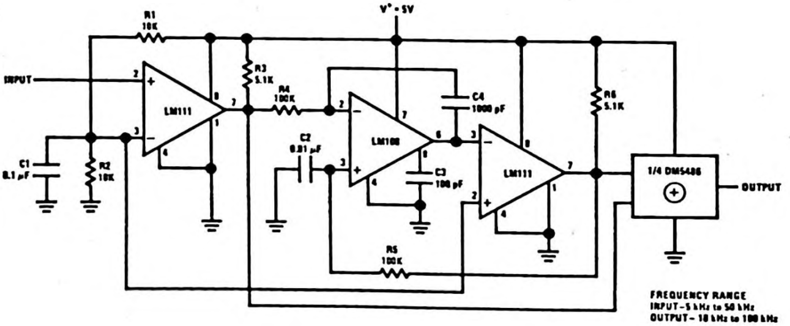

R1
100K
V⁺ = 5V
R4
2K
100 KHz
C2
10 pF
R2
100K
LM111
2
3
8
7
4
1
OUTPUT
C1
0.1 μF
R3
50K

FIGURE 9. Crystal-Controlled Oscillator

FREQUENCY DOUBLER

In a digital system, it is a relatively simple matter to divide by any integer. However, multiplying by an integer is quite another story especially if operation over a wide frequency range and waveform symmetry are required.

A frequency doubler that satisfies the above requirements is shown in Figure 10. A compar-


R1
10K
V⁺ = 5V
INPUT
LM111
R3
5.1K
R4
100K
C4
1000 pF
R6
5.1K
LM108
C2
0.01 μF
C3
100 pF
LM111
1/4 DM5486
OUTPUT
C1
0.1 μF
R2
10K
R5
100K
2
3
8
7
1
4
6

FREQUENCY RANGE
INPUT – 5 kHz to 50 kHz
OUTPUT – 10 kHz to 100 kHz

FIGURE 10. Frequency Doubler

ator is used to shape the input signal and feed it to an integrator. The shaping is required because the input to the integrator must swing between the supply voltage and ground to preserve symmetry in the output waveform. An LM108 op amp, that works from the 5V logic supply, serves as the integrator. This feeds a triangular waveform to a second comparator that detects when the waveform goes through a voltage equal to its average value. Hence, as shown in Figure 11, the output of the second comparator is delayed by half the duration of the input pulse. The two comparator outputs can then be combined through an exclusive-OR gate to produce the double-frequency output.

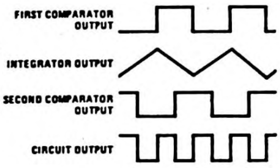


FIGURE 11. Waveforms for the Frequency Doubler

With the component values shown, the circuit operates at frequencies from 5 kHz to 50 kHz. Lower frequency operation can be secured by increasing both C_1 and C_2.

APPLICATION HINTS

One of the problems encountered in using earlier IC comparators like the LM710 or LM106 was that they were prone to erratic operation caused by oscillations. This was a direct result of the high speed of the devices, which made it mandatory to provide good input-output isolation and low-inductance bypassing on the supplies. These oscillations could be particularly puzzling when they occurred internally, showing up at the external terminals only as erratic dc characteristics.

In general, the LM111 is less susceptible to spurious oscillations both because of its lower speed (200 ns response time vs 40 ns) and because of its better power supply rejection. Feedback between the output and the input is a lesser problem with a given source resistance. However, the LM111 can operate with source resistances that are orders of magnitude higher than the earlier devices, so stray coupling between the input and output should be minimized. With source resistances between 1 kΩ and 10 kΩ, the impedance (both capacitive and resistive) on both inputs should be made equal, as this tends to reject the signal fed back. Even so, it is difficult to completely eliminate oscillations in the linear region with source resistances above 10 kΩ, because the 1 MHz open loop gain of the comparator is about 80 dB. However, this does not affect the dc characteristics and is not a problem unless the input signal dwells within 200 μV of the transition level. But if the oscillation does cause difficulties, it can be eliminated with a small amount of positive feedback around the comparator to give a 1 mV hysteresis.

Stray coupling between the output and the balance terminals can also cause oscillations, so an attempt should be made to keep these leads apart. It is usually advisable to tie the balance pins together to minimize the effect of this feedback. If balancing is used, the same result can be accomplished by connecting a 0.1 μF capacitor between these pins.

Normally, individual supply bypasses on every device are unnecessary, although long leads between the comparator and the bypass capacitors are definitely not recommended. If large current spikes are injected into the supplies in switching the output, bypass capacitors should be included at these points.

When driving the inputs from a low impedance source, a limiting resistor should be placed in series with the input lead to limit the peak current to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Low impedance sources do not cause a problem unless their output voltage exceeds the negative supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. A charged capacitor can hold the inputs outside the supply voltage if the supplies are abruptly shut off.

Precautions should be taken to insure that the power supplies for this or any other IC never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC can conduct excessive current, fuzing internal aluminum interconnects. This usually takes more than 0.5A. If there is a possibility of reversal, clamp diodes with an adequate peak current rating should be installed across the supply bus.

No attempt should be made to operate the circuit with the ground terminal at a voltage exceeding either supply voltage. Further, the 50V output-voltage rating applies to the potential between the output and the V^- terminal. Therefore, if the comparator is operated from a negative supply, the maximum output voltage must be reduced by an amount equal to the voltage on the V^- terminal.

The output circuitry is protected for shorts across the load. It will not, for example, withstand a short to a voltage more negative than the ground terminal. Additionally, with a sustained short, power dissipation can become excessive if the voltage across the output transistor exceeds about 10V.

The input terminals can exceed the positive supply voltage without causing damage. However, the 30V maximum rating between the inputs and the V^- terminal must be observed. As mentioned earlier, the inputs should not be driven more negative than the V^- terminal.

CONCLUSIONS

A versatile voltage comparator that can perform many of the precision functions required in digital systems has been produced. Unlike older comparators, the IC can operate from the same supply voltage as the digital circuits. The comparator is particularly useful in circuits requiring considerable sensitivity and accuracy, such as threshold detectors for low level sensors, data transmission circuits or stable oscillators and multivibrators.

The comparator can also be used in many analog systems. It operates from standard ±15V op amp supplies, and its dc accuracy equals some of the best op amps. It is also an order of magnitude faster than op amps used as comparators.

The new comparator is considerably more flexible than older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic or deliver ±15V to FET analog switches. The output can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. Further, a unique output stage enables it to drive loads referred to either supply or to ground and provide ground isolation between the comparator inputs and the load.

The LM111 is a plug-in replacement for comparators like the LM710 and LM106 in applications where speed is not of prime concern. Compared to its predecessors in other respects, it has many improved electrical specifications, more design flexibility and fewer application problems.

IC Provides On-Card Regulation for Logic Circuits

National Semiconductor
Application Note 42
February 1971

INTRODUCTION

Because of the relatively high current requirements of digital systems, there are a number of problems associated with using one centrally-located regulator. Heavy power busses must be used to distribute the regulated voltage. With low voltages and currents of many amperes, voltage drops in connectors and conductors can cause an appreciable percentage change in the voltage delivered to the load. This is aggravated further with TTL logic, as it draws transient currents many times the steady-state current when it switches.

These problems have created a considerable interest in on-card regulation, that is, to provide local regulation for the subsystems of the computer. Rough preregulation can be used, and the power distributed without excessive concern for line drops. The local regulators then smooth out the voltage variations due to line drops and absorb transients.

A monolithic regulator is now available to perform this function. It is quite simple to use in that it requires no external components. The integrated circuit has three active leads—input, output and ground—and can be supplied in standard transistor power packages. Output currents in excess of 1A can be obtained. Further, no adjustments are required to set up the output voltage, and overload protection is provided that makes it virtually impossible to destroy the regulator. The simplicity of the regulator, coupled with low-cost fabrication and improved reliability of monolithic circuits, now makes on-card regulation quite attractive.

DESIGN CONCEPTS

A useful on-card regulator should include everything within one package—including the power-control element, or pass transistor. The author has previously advanced arguments against including the pass transistor in an integrated circuit regulator.[1] First, there are no standard multi-lead power packages. Second, integrated circuits necessarily have a lower maximum operating temperature, because they contain low-level circuitry. This means that an IC regulator needs a more massive heat sink. Third, the gross variations in chip temperature due to dissipation in the pass transistors worsen load and line regulation. However, for a logic-card regulator, these arguments can be answered effectively.

For one, if the series pass transistor is put on the chip, the integrated circuit need only have three terminals. Hence, an ordinary transistor power package can be used. The practicality of this approach depends on eliminating the adjustments usually required to set up the output voltage and limiting current for the particular application, as external adjustments require extra pins. A new solid-state reference, to be described later, has sufficiently-tight manufacturing tolerances that output voltages do not always have to be individually trimmed. Further, thermal overload protection can protect an IC regulator for virtually any set of operating conditions, making current-limit adjustments unnecessary.

Thermal protection limits the maximum junction temperature and protects the regulator regardless of input voltage, type of overload or degree of heat sinking. With an external pass transistor, there is no convenient way to sense junction temperature so it is much more difficult to provide thermal limiting. Thermal protection is, in itself, a very good reason for putting the pass transistor on the chip.

When a regulator is protected by current limiting alone, it is necessary to limit the output current to a value substantially lower than is dictated by dissipation under normal operating conditions to prevent excessive heating when a fault occurs. Thermal limiting provides virtually absolute protection for any overload condition. Hence, the maximum output current under normal operating conditions can be increased. This tends to make up for the fact that an IC has a lower maximum junction temperature than discrete transistors.

Additionally, the 5V regulator works with relatively low voltage across the integrated circuit. Because of the low voltage, the internal circuitry can be operated at comparatively high currents without causing excessive dissipation. Both the low voltage and the larger internal currents permit higher junction temperatures. This can also reduce the heat sinking required—especially for commercial-temperature-range parts.

Lastly, the variations in chip temperature caused by dissipation in the pass transistor do not cause serious problems for a logic-card regulator. The tolerance in output voltage is loose enough that it is relatively easy to design an internal reference that is much more stable than required, even for temperature variations as large as 150°C.

CIRCUIT DESCRIPTION

The internal voltage reference for this logic-card regulator is probably the most significant departure from standard design techniques. Temperature-compensated zener diodes are normally used for the reference. However, these have breakdown voltages between 7V and 9V which puts a lower limit on the input voltage to the regulator. For low voltage operation, a different kind of reference is needed.

The reference in the LM109 does not use a zener diode. Instead, it is developed from the highly-predictable emitter-base voltage of the transistors. In its simplest form, the reference developed is equal to the energy-band-gap voltage of the semiconductor material. For silicon, this is 1.205V, so the reference need not impose minimum input voltage limitations on the regulator. An added advantage of this reference is that the output voltage is well determined in a production environment so that individual adjustment of the regulators is frequently unnecessary.

A simplified version of this reference is shown in Figure 1. In this circuit, Q_1 is operated at a relatively high current density. The current density of Q_2 is about ten times lower, and the emitter-base voltage differential (ΔV_{BE}) between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter base voltage plus the drop across R_2. The emitter base voltage of Q_3 has a negative temperature coefficient while the ΔV_{BE} component across R_2 has a positive temperature coefficient. It will be shown that the output voltage will be temperature compensated when the sum of the two voltages is equal to the energy-band-gap voltage.

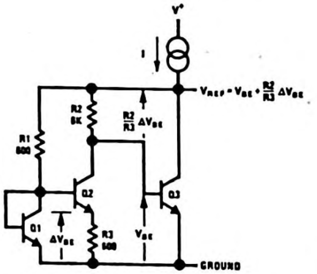

V+
I
$V_{REF} = V_{BE} + \frac{R2}{R3} \Delta V_{BE}$
R2
6K
$\frac{R2}{R3} \Delta V_{BE}$
R1
600
Q2
Q3
Q1
ΔV_{BE}
R3
600
V_{BE}
GROUND

Figure 1. The Low Voltage Reference in One of Its Simpler Forms.

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor which is[2]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q}\log_e\frac{T_0}{T} + \frac{kT}{q}\log_e\frac{I_C}{I_{C0}}, \qquad (1)$$

Where V_{g0} is the extrapolated energy-band-gap voltage for the semiconductor material at absolute zero, q is the charge of an electron, n is a constant which depends on how the transistor is made (approximately 1.5 for double-diffused, NPN transistors), k is Boltzmann's constant, T is absolute temperature, I_C is collector current and V_{BE0} is the emitter-base voltage at T_0 and I_{C0}.

The emitter-base voltage differential between two transistors operated at different current densities is given by[3]

$$\Delta V_{BE} = \frac{kT}{q}\log_e\frac{J_1}{J_2}, \qquad (2)$$

where J is current density.

Referring to Equation (1), the last two terms are quite small and are made even smaller by making I_C vary as absolute temperature. At any rate, they can be ignored for now because they are of the same order as errors caused by nontheoretical behavior of the transistors that must be determined empirically.

If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE}, the output voltage is obtained by adding (1) in its simplified form to (2):

$$V_{ref} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{kT}{q}\log_e\frac{J_1}{J_2}. \qquad (3)$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BE0}}{T_0} + \frac{k}{q}\log_e\frac{J_1}{J_2}. \qquad (4)$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BE0} + \frac{kT_0}{q}\log_e\frac{J_1}{J_2}. \qquad (5)$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy-band-gap voltage of the semiconductor, the reference will be temperature-compensated.

A simplified schematic for a 5V regulator is given in Figure 2. The circuitry produces an output voltage that is approximately four times the basic reference voltage. The emitter-base voltage of Q_3, Q_4, Q_5 and Q_8 provide the negative-temperature-coefficient component of the output voltage. The voltage dropped across R_3 provides the positive-temperature-coefficient component. Q_6 is operated at a considerably higher current density than Q_7, producing a voltage drop across R_4 that is proportional to the emitter-base voltage differential of the two transistors. Assuming large current gain in the transistors, the voltage drop across R_3 will be proportional to this differential, so a temperature-compensated-output voltage can be obtained.

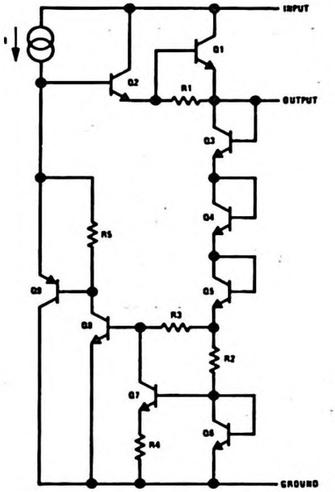


Figure 2. Schematic Showing Essential Details of The 5V Regulator.

In this circuit, Q_8 is the gain stage providing regulation. Its effective gain is increased by using a vertical PNP, Q_9, as a buffer driving the active collector load represented by the current source. Q_9 drives a modified Darlington output stage (Q_1 and Q_2) which acts as the series pass element. With this circuit, the minimum input voltage is not limited by the voltage needed to supply the reference. Instead, it is determined by the output voltage and the saturation voltage of the Darlington output stage.

Figure 3 shows a complete schematic of the LM109, 5V regulator. The ΔV_{BE} component of the output voltage is developed across R_8 by the collector current of Q_7. The emitter-base voltage differential is produced by operating Q_4 and Q_5 at high current densities while operating Q_6 and Q_7 at much lower current levels. The extra transistors improve tolerances by making the emitter-base voltage differential larger. R_3 serves to compensate the transconductance[4] of Q_5, so that the ΔV_{BE} component is not affected by changes in the regulator output voltage or the absolute value of components.

The voltage gain for the regulating loop is provided by Q_{10}, with Q_9 buffering its input and Q_{11} its output. The emitter base voltage of Q_9 and Q_{10} is added to that of Q_{12} and Q_{13} and the drop across R_8 to give a temperature-compensated, 5V output. An emitter-base-junction capacitor, C_1, frequency compensates the circuit so that it is stable even without a bypass capacitor on the output.

The active collector load for the error amplifier is Q_{17}. It is a multiple-collector lateral PNP[4]. The output current is essentially equal to the collector current of Q_2, with current being supplied to the zener diode controlling the thermal shutdown, D_2, by an auxiliary collector. Q_1 is a collector FET[4] that, along with R_1, insures starting of the regulator under worst-case conditions.

The output current of the regulator is limited when the voltage across R_{14} becomes large enough to turn on Q_{14}. This insures that the output current cannot get high enough to cause the pass transistor to go into secondary breakdown or damage the aluminum conductors on the chip. Further, when the voltage across the pass transistor exceeds 7V, current through R_{15} and D_3 reduces the limiting current, again to minimize the

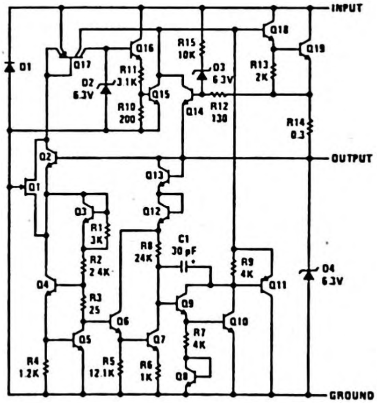


Figure 3. Detailed Schematic of The Regulator.

chance of secondary breakdown. The performance of this protection circuitry is illustrated in Figure 4.

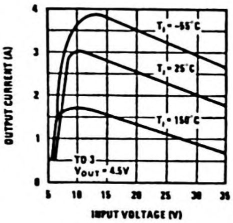


Figure 4. Current-Limiting Characteristics.

Even though the current is limited, excessive dissipation can cause the chip to overheat. In fact, the dominant failure mechanism of solid state regulators is excessive heating of the semiconductors, particularly the pass transistor. Thermal protection attacks the problem directly by putting a temperature regulator on the IC chip. Normally, this regulator is biased below its activation threshold; so it does not affect circuit operation. However, if the chip approaches its maximum operating temperature, for any reason, the temperature regulator turns on and reduces internal dissipation to prevent any further increase in chip temperature.

The thermal protection circuitry develops its reference voltage with a conventional zener diode, D_2. Q_{16} is a buffer that feeds a voltage divider, delivering about 300 mV to the base of Q_{15} at 175°C. The emitter-base voltage, Q_{15}, is the actual temperature sensor because, with a constant voltage applied across the junction, the collector current rises rapidly with increasing temperature.

Although some form of thermal protection can be incorporated in a discrete regulator, IC's have a distinct advantage: the temperature sensing device detects increases in junction temperature within milliseconds. Schemes that sense case or heat-sink temperature take several seconds, or longer. With the longer response times, the pass transistor usually blows out before thermal limiting comes into effect.

Another protective feature of the regulator is the crowbar clamp on the output. If the output voltage tries to rise for some reason, D_4 will break down and limit the voltage to a safe value. If this rise is caused by failure of the pass transistor such that the current is not limited, the aluminum conductors on the chip will fuse, disconnecting the load. Although this destroys the regulator, it does protect the load from damage. The regulator is also designed so that it is not damaged in the event the unregulated input is shorted to ground when there is a large capacitor on the output. Further, if the input voltage tries to reverse, D_1 will clamp this for currents up to 1A.

The internal frequency compensation of the regulator permits it to operate with or without a bypass capacitor on the output. However, an output capacitor does improve the transient response and reduce the high frequency output impedance. A plot of the output impedance in Figure 5 shows that it remains low out to 10 kHz even without a capacitor. The ripple rejection also remains high out to 10 kHz, as shown in Figure 6. The irregularities in this curve around 100 Hz are caused by thermal feedback from the pass transistor to the reference circuitry. Although an output capacitor is not required, it is necessary to bypass the input of the regulator with at least a 0.22 µF capacitor to prevent oscillations under all conditions.

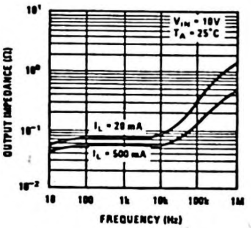


Figure 5. Plot of Output Impedance As A Function of Frequency.

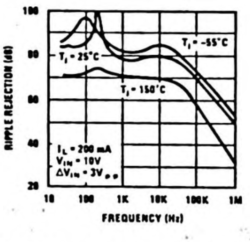


Figure 6. Ripple Rejection of The Regulator.

Figure 7 is a photomicrograph of the regulator chip. It can be seen that the pass transistors, which must handle more than 1A, occupy most of the chip area. The output transistor is actually broken into segments. Uniform current distribution is insured by also breaking the current limit resistor into segments and using them to equalize the currents. The overall electrical performance of this IC is summarized in Table 1.

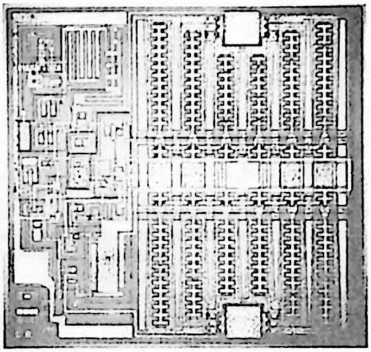


Figure 7. Photomicrograph of The Regulator Shows That High Current Pass Transistor (Right) Takes More Area Than Control Circuitry (Left).

PARAMETER	CONDITIONS	TYP
Output Voltage		5.0V
Output Current		1.5A
Output Resistance		0.03Ω
Line Regulation	$7.0V \leq V_{IN} \leq 35V$	0.005%/V
Temperature Drift	$-55°C \leq T_A \leq 125°C$	0.02%/°C
Minimum Input Voltage	$I_{OUT} = 1A$	6.5V
Output Noise Voltage	$10 Hz \leq f \leq 100 kHz$	40 µV
Thermal Resistance Junction to Case	LM109H (TO-5) LM109K (TO-3)	15°C/W 3°C/W

Table 1. Typical Characteristics of The Logic-Card Regulator: $T_A = 25°C$.

APPLICATIONS

Because it was designed for virtually foolproof operation and because it has a singular purpose, the LM109 does not require a lot of application information, as do most other linear circuits. Only one precaution must be observed: it is necessary to bypass the unregulated supply with a 0.22 µF capacitor, as shown in Figure 8, to prevent oscillations that can cause erratic operation. This, of course, is only necessary if the regulator is located an appreciable distance from the filter capacitors on the output of the dc supply.

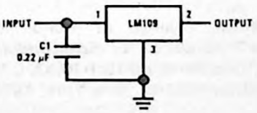


Figure 8. Fixed 5V Regulator

Although the LM109 is designed as a fixed 5V regulator, it is also possible to use it as an adjustable regulator for higher output voltages. One circuit for doing this is shown in Figure 9.

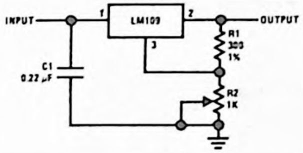


Figure 9. Using The LM109 As An Adjustable-Output Regulator.

The regulated output voltage is impressed across R_1, developing a reference current. The quiescent current of the regulator, coming out of the ground terminal, is added to this. These combined currents produce a voltage drop across R_2 which raises the output voltage. Hence, any voltage above 5V can be obtained as long as the voltage across the integrated circuit is kept within ratings.

The LM109 was designed so that its quiescent current is not greatly affected by variations in input voltage, load or temperature. However, it is not completely insensitive, as shown in Figures 10 and 11, so the changes do affect regulation somewhat. This tendency is minimized by making the reference current through R_1 larger than the quiescent current. Even so, it is difficult to get the regulation tighter than a couple percent.

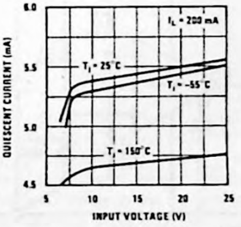


Figure 10. Variation of Quiescent Current With Input Voltage At Various Temperatures.

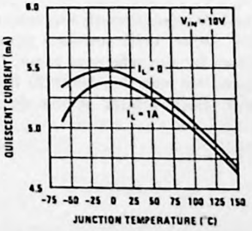


Figure 11. Variation of Quiescent Current With Temperature For Various Load Currents.

The LM109 can also be used as a current regulator as is shown in Figure 12. The regulated output voltage is impressed across R_1, which determines the output current. The quiescent current is added to the current through R_1, and this puts a lower limit of about 10 mA on the available output current.

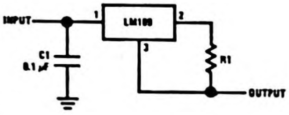


Figure 12. Current Regulator.

The increased failure resistance brought about by thermal overload protection make the LM109 attractive as the pass transistor in other regulator circuits. A precision regulator that employs the IC thusly is shown in Figure 13. An operational amplifier compares the output voltage with the output voltage of a reference zener. The op amp controls the LM109 by driving the ground terminal through an FET.

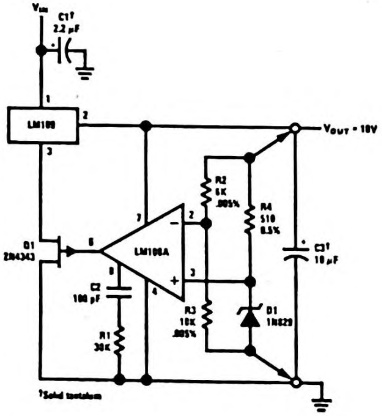


Figure 13. High Stability Regulator.

The load and line regulation of this circuit is better than 0.001%. Noise, drift and long term stability are determined by the reference zener, D_1. Noise can be reduced by inserting 100 kΩ, 1% resistors in series with both inputs of the op amp and bypassing the non-inverting input to ground. A 100 pF capacitor should also be included between the output and the inverting input to prevent frequency instability. Temperature drift can be reduced by adjusting R_4, which determines the zener current, for minimum drift. For best performance, remote sensing directly to the load terminals, as shown in the diagram, should be used.

CONCLUSIONS

The LM109 performs a complete regulation function on a single silicon chip, requiring no external components. It makes use of some unique advantages of monolithic construction to achieve performance advantages that cannot be obtained in discrete-component circuits. Further, the low cost of the device suggests its use in applications where single-point regulation could not be justified previously.

Thermal overload protection significantly improves the reliability of an IC regulator. It even protects the regulator for unforseen fault conditions that may occur in field operation. Although this can be accomplished easily in a monolithic regulator, it is usually not completely effective in a discrete or hybrid device.

The internal reference developed for the LM109 also advances the state of the art for regulators. Not only does it provide a low voltage, temperature-compensated reference for the first time, but also it can be expected to have better long term stability than conventional zeners. Noise is inherently much lower, and it can be manufactured to tighter tolerances.

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The Phase Locked Loop IC as a Communication System Building Block

National Semiconductor
Application Note 46
Thomas B. Mills
June 1971

INTRODUCTION

The phase locked loop has been found to be a useful element in many types of communication systems. It is used in two fundamentally different ways: (1) as a demodulator, where it is used to follow phase or frequency modulation and (2) to track a carrier or synchronizing signal which may vary in frequency with time.

When operating as a demodulator, the phase locked loop may be thought of as a matched filter operating as a coherent detector. When used to track a carrier, it may be thought of as a narrow-band filter for removing noise from a signal.

Recently, a phase locked loop has been built on a monolithic integrated circuit, incorporating the basic elements necessary for operation: a double balanced phase detector and a highly linear voltage controlled oscillator, the frequency of which can be varied with either a resistor or capacitor.

BASIC PHASE LOCK LOOP OPERATION

Figure 1 shows the basic blocks of a phase locked loop. The input signal e_i is a sinusoid of arbitrary frequency, while the VCO output signal, e_o, is a sinsuoid of the same frequency as the input but of arbitrary phase. If

$$e_i = \sqrt{2}\, E_i\, [\sin \omega_o t + \theta_1(t)] \tag{1}$$

$$e_o = \sqrt{2}\, E_o\, [\sin \omega_o t + \theta_2(t)] \tag{2}$$

the output of the multiplier (phase detector) is

$$\begin{aligned} e_d = e_i \cdot e_o &= 2E_iE_o \sin\, [\omega_o t + \theta_1(t)] \\ &\qquad \cos\, [\omega_o t + \theta_2(t)] \\ &= E_iE_o \sin\, [\theta_1(t) - \theta_2(t)] \\ &\qquad + \sin\, [2\, \omega_o t + \theta_1(t) + \theta_2(t)] \end{aligned} \tag{3}$$

the low pass filter of the loop removes the ac components of the multiplier output; the dc term is seen to be a function of the phase angle between the VCO and the input signal.

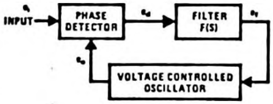


FIGURE 1. Basic Phase Locked Loop

The output of the VCO is related to its input control voltage by

$$\dot{\theta}_2(t) = K_o e_f \tag{4}$$

for $e_f = 0$, let $\dot{\theta}_2 = \omega\theta$, then

$$\theta_2(t) = \int e_f(t)\, dt \tag{5}$$

It can be seen that the action of the VCO is that of an integrator in the feedback loop when the phase locked loop is considered in servo theory.

A better understanding of the operation of the loop may be obtained by considering that initially, the loop is not in lock, but that the frequency of the input signal e_i and VCO e_o are very close in frequency. Under these conditions e_d will be a beat note, the frequency of which is equal to the frequency difference of e_o and e_i. This signal is also applied to the VCO input, since it is low enough to pass through the filter. The instantaneous frequency of the VCO is therefore changing and at some point in time, if the VCO frequency equals the input frequency, lock will result. At this instant, e_f will assume a level sufficient to hold the VCO frequency in lock with the input frequency. If the tuning of the VCO is changed (such as by varying the value of the tuning capacitor) the frequency output of the VCO will attempt to change; however, this will result in an instantaneous change in phase angle between e_i and e_o, resulting in a change in the dc level of e_d which will act to maintain frequency lock: no average frequency change will result.

Similarly, if e_i changes frequency, an instantaneous change will result in a phase change between e_i and e_o and hence a dc level change in e_d. This level shift will change the frequency of the VCO to maintain lock.

The amount of phase error resulting from a given frequency shift can be found by knowing the "dc" loop gain of the system. Considering the phase detector to have a transfer function:

$$E_d = K_D(\theta_1 - \theta_2)$$

and the voltage controlled oscillator to have a transfer function:

$$\theta_2 = K_o\, e_f \tag{6}$$

or taking the Laplace transform

$$\theta_2(s) = \frac{K_o e_f}{s} \tag{7}$$

the phase of the VCO output will be proportional to the integral of the control voltage.

Combining these equations:

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_d F(s)}{s + K_o K_D F(s)} \tag{8}$$

$$\frac{\theta_1(s) - \theta_2(s)}{\theta_1(s)} = \frac{s}{s + K_o K_D F(s)} \tag{9}$$

Application of the final value theorem of Laplace transforms yields

$$\lim_{t \to \infty} \theta_1(s) - \theta_2(s) = \lim_{s \to 0} \frac{s^2 \theta_1(s)}{s + K_o K_D F(s)} \tag{10}$$

With a step change in phase of the input $\Delta\theta_1$, the Laplace transform of the input is

$$\theta_1(s) = \frac{\Delta\theta_1}{s} \text{ which gives } \theta_e(s) = \theta_1(s) - \theta_2(s)$$

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{s\Delta\theta_1}{s + K_o K_D F(s)} = 0 \tag{11}$$

the loop will eventually track out any change of input phase, and there will be no phase error in the steady state solution.

If the input is a step in frequency, of magnitude $\Delta\omega$, the change in input phase will be a ramp:

$$\theta_1(s) = \Delta\omega/s^2$$

substitution of this value θ, into (10) results in

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{\Delta\omega}{s + K_o K_D F(s)} = \frac{\Delta\omega}{K_o K_D F(0)} \tag{12}$$

this result shows the resulting phase error is dependent on the magnitude of the frequency step and the "dc" loop gain $K_o K_D$, which is also called the velocity error coefficient K_v. It should be noted that the dimensions of $K_o K_D$ are 1/sec. This can also be seen by considering K_D = volts/radian, while K_o = radians/sec/volt. The product is

$$\frac{\text{volts}}{\text{radian}} \times \frac{\text{radians/sec}}{\text{volt}} = \frac{1}{\text{sec}}$$

this can be thought of as the "dc" loop gain. (Note that additional dc gain between the phase detector and the voltage controlled oscillator will increase the loop gain and hence reduce the steady state phase error resulting from a change in frequency of the input.)

THE LOOP FILTER

In working with phase locked loops, it is necessary to consider not only the "dc" performance described above, but the "ac" or transient performance which is governed by the components of the loop filter placed between the phase detector and the voltage controlled oscillator. In fact, it is this loop filter that makes the phase locked loop so powerful: only a resistor and capacitor are all that is needed to produce an arbitrarily narrow bandwidth at any selected center frequency.

The simplest filter is a single capacitor, Figure 2, and is used for wide bandwidth applications, such as where wideband data modulation must be followed. The transfer function of the filter is simply:

$$\frac{e_f}{e_d} = \frac{1}{1 + sR_1C_1} \tag{13}$$

substitution into (8) results in

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_D/\tau_1}{s^2 + s/\tau_1 + K_o K_D/\tau_1} \tag{14}$$

$$\tau_1 = R_1C_1$$

In terms of servo theory, the damping factor and natural frequencies are

$$\omega_n = \left[\frac{K_o K_D}{R_1 C_1}\right]^{1/2} \tag{15}$$

$$\zeta = \frac{1}{2}\left[\frac{1}{(R_1 C_1 K_o K_D)}\right]^{1/2} \tag{16}$$

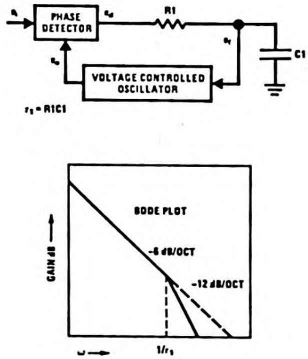


FIGURE 2. Phase Locked Loop with Simple Filter

From this it can be seen that large time constants for R_1C_1 or high loop gain will reduce the damping factor and hence decrease stability. Therefore, if a narrow bandwidth is desired, the damping factor will become very small and instability will result. It is not possible to adjust bandwidth, loop gain, and damping independently with this simple filter.

With the addition of a damping resistor R_2 as shown in Figure 3, it is possible to choose bandwidth, damping factor and loop gain independently; the transfer function of this filter is

$$\frac{e_d}{e_f} = \frac{s\tau_2 + 1}{s(\tau_1 + \tau_2)} \tag{17}$$

the loop transfer function becomes:

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_oK_D(s\tau_2 + 1)(\tau_1 + \tau_2)}{s^2 + s(1 + K_oK_d\tau_2)/(\tau_1 + \tau_2) + K_oK_D/(\tau_1 + \tau_2)} \tag{18}$$

the loop natural frequency is

$$\omega_n = \left[\frac{K_oK_D}{\tau_1 + \tau_2}\right]^{1/2} \tag{19}$$

while the damping factor becomes

$$\delta = \frac{1}{2}\left[\frac{K_oK_D}{\tau_1 + \tau_2}\right]^{1/2}\left[\tau_2 + \frac{1}{K_oK_D}\right] \tag{20}$$

$$\simeq \frac{\omega_n \tau_2}{2} \tag{21}$$

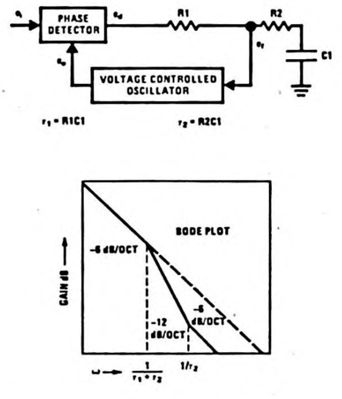


FIGURE 3. Phase Locked Loop with Damping Resistor Added

In practice, for a fixed loop gain K_oK_D, the natural frequency of the loop may be chosen and will be dependent mainly on τ_1, since $\tau_2 << \tau_1$ in most cases. Then, according to (21), damping may be determined by τ_2 and for all practical purposes, will be an independent adjustment. These equations are plotted in Figures 4 and 5 and may be used for design purposes.

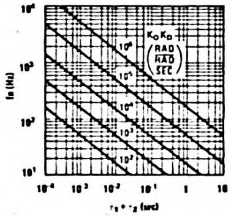


FIGURE 4. Filter Time Constant vs Natural Frequency

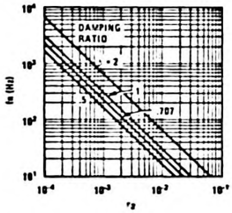


FIGURE 5. Damping Time Constant vs Natural Frequency

DESIGN CONSIDERATIONS

Considering the above discussion, there are really two primary considerations in designing a phase locked loop. The use to which the loop is to be put will affect the design criterion of the loop components. The two primary factors to consider are:

1. Loop gain. As pointed out previously, this affects the phase error between the input signal and the voltage controlled oscillator for a given frequency shift of the input signal. It also determines the "hold in range" of the loop providing no components of the loop go into limiting or saturation. This is because the loop will remain in lock as long as the phase difference between the input and the VCO is less than ±90°. The higher the loop gain, the further the input can change in frequency before the 90° phase error is reached. The hold in range is

   $$\Delta\omega_H = \pm K_oK_D \tag{22}$$

   (providing saturation or limiting does not occur).

2. Natural Frequency. The bandwidth of the loop is determined by the filter components R_1, R_1 and C_1 and the loop gain. Since the loop gain is normally selected by the criterion in 1. above, the filter components are used to select the bandwidth. The selection of loop bandwidth may be governed by several things: noise bandwidth, modulation rates if the loop is to be

used as an FM demodulator, pull-in time and hold-in range. There are two conflicting requirements that will have an affect on loop bandwidth:

(a) Loop bandwidth must be as narrow as possible to minimize output phase jitter due to external noise.

(b) The loop bandwidth should be made as large as possible to minimize transient error due to signal modulation, output jitter due to internal oscillator (VCO) noise, and to obtain best tracking and acquisition properties.

These two principles are in direct opposition and, depending on what it is that the loop is to accomplish, an optimum solution will lie somewhere between the two extremes.

If the phase locked loop is to be used to demodulate frequency modulation, the design should proceed with the criterion of b above. It is necessary to provide sufficient loop bandwidth to accommodate the expected modulation. It must be remembered that at all times, the loop must remain in lock, (peak phase error less than 90°), even under extremes of modulation, such as peaks or step changes in frequency.

For the case of sinusoidal frequency modulation, the peak phase error as a function of frequency deviation and damping factor is shown in Figure 6.

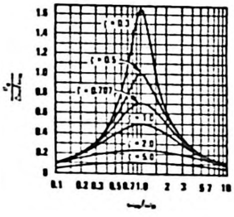


FIGURE 6. Steady-State Peak Phase Error Due to Sinusoidal FM (High-Gain, Second-Order Loop.)

It can be seen that the maximum phase error occurs when the modulating frequency ω_m equals the loop natural frequency ω_n; if the loop has been designed with a damping factor of .707, the peak phase error (in radians) will be .71 $\Delta\omega/\omega_n$ ($\Delta\omega$ = frequency deviation). From this plot, it is possible to choose ω_n for a given deviation and modulation frequency.

If the loop is to demodulate frequency shift keying (FSK), it must follow step changes in frequency. The filter components must then be chosen in accordance with the transient phase error shown in Figure 7. It must be remembered that the loop filter must be wide enough so the loop will not lose lock when a step change in frequency occurs: the greater the frequency step, the wider the loop filter must be to maintain lock.

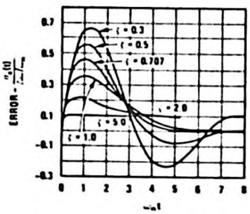


FIGURE 7. Transient Phase Error $\theta_e(t)$ Due to a Step in Frequency $\Delta\omega$. (Steady-State Velocity Error, $\Delta\omega/K_v$, Neglected.)

There is some frequency-step limit below which the loop does not skip cycles, but remains in lock, called the "pull-out frequency" ω_{po}. Viterbi has analyzed this and his results are shown in Figure 8, which plots normalized pull out frequency for various damping factors for high gain second order loops. Peak phase errors for other types of input signals are shown in Figures 8 and 9.

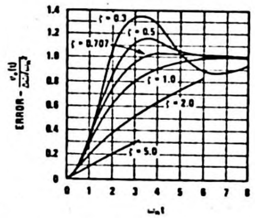


FIGURE 8. Transient Phase Error $\theta_e(t)$ Due to a Ramp in Frequency $\Delta\omega$. (Steady-State Acceleration Error, $\Delta\dot{\omega}/\omega_n^2$, included. Velocity Error, $\Delta\dot{\omega}t/K_v$, Neglected

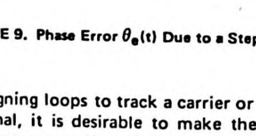


FIGURE 9. Phase Error $\theta_e(t)$ Due to a Step in Phase $\Delta\theta$

In designing loops to track a carrier or synchronizing signal, it is desirable to make the loop bandwidth narrow so that phase error due to external noise will be small. However, it is necessary to make the loop bandwidth wide enough so that any frequency jitter on the input signal will be followed.

NOISE PERFORMANCE

Since one of the main uses of phase locked loops is to demodulate or track signals in noise, it is helpful to look at how noise affects the operation of the phase locked loop.

The phase locked loop, as mentioned earlier, may be thought of as a filter with a fixed, adjustable bandwidth. We have seen how to calculate the loop natural frequency ω_n (15), (19), and the damping factor ζ (16), (20). Without going through a derivation, the loop noise bandwidth B_L may be shown to be

$$B_L = \int_0^{\infty} |H(j\omega)|^2 \, df = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] \text{Hz} \quad (23)$$

for a high gain, second order loop. This equation is plotted in Figure 10. It should be noted that the dimensions of noise bandwidth are cycles per second while the dimensions of ω_n are radians per second.

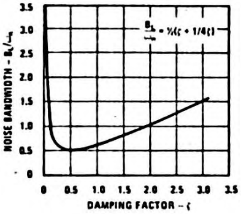


FIGURE 10. Loop-Noise Bandwidth (For High-Gain, Second-Order Loop)

Noise threshold is a difficult thing to analyze in a phase locked loop, since we are talking about a statistical quantity. Noise will show up in the input signal as both amplitude and phase modulation. It can be shown that near optimum performance of a phase locked loop can be obtained if a limiter is used ahead of the phase detector, or if the phase detector is allowed to operate in limiting. With the use of a limiter, amplitude modulation of the input signal by noise is removed, and the noise appears as phase modulation. As the input signal to noise ratio decreases, the phase jitter of the input signal due to noise increases, and the probability of losing lock due to instantaneous phase excersions will increase. In practice it is nearly impossible to acquire lock if the signal to noise ratio in the loop $(SNR)_L$ = 0 dB. In general, $(SNR)_L$ of +6 dB is needed for acquisition. If modulation or transient phase error is present, a higher signal to noise ratio is needed to acquire and hold lock.

A computer simulation performed by Sanneman and Rowbotham has shown the probability of skipping cycles for various loop signal to noise ratios for high gain, second order loops. Their data is shown in Figure 11.

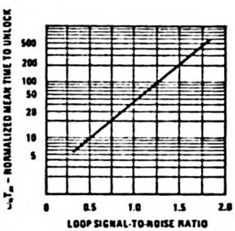


FIGURE 11. Unlock Behavior of High-Gain, Second-Order Loop, $\zeta = 0.707$

When designing the loop filter components, enough bandwidth in the loop must be allowed for instantaneous phase change due to input noise. In the previous section, the filter was selected on the basis that the peak error due to modulation would be less than 90° (so the loop would not loose lock). However, if noise is present, the peak phase error will increase due to the noise. So if the loop is not to lose lock on these noise peaks, the peak allowable error due to modulation must be reduced to something less, on the order of 40° to 50°.

LOCKING

Initially, a loop is unlocked and the VCO is running at some frequency. If a signal is applied to the input, locking may or may not occur depending on several things.

If the signal is within the bandwidth of the loop filter, locking will occur without a beat note being generated or any cycles being skipped. This frequency is given by

$$\Delta\omega_L = \frac{K_o K_D \tau_2}{\tau_1 + \tau_2} \approx 2\zeta\omega_n \quad (24)$$

If the frequency of the input signal is further away from the VCO frequency, locking may still occur, with a beat note being generated. The greatest frequency that can be pulled in is called the "pull in frequency" and is found from the approximation

$$\Delta\omega_P \approx \sqrt{2}\,(2\zeta\omega_n K_o K_D - \omega_n^2)^{1/2} \quad (25)$$

which works well for moderate and high gain loops ($\omega_n/K_oK_D < .4$).

An approximate expression for pull in time (the time required to achieve lock from some frequency offset $\Delta\omega$) is given by:

$$T_P \approx \frac{(\Delta\omega)^2}{2\zeta\omega_n^3}$$

A MONOLITHIC PHASE LOCKED LOOP

A complete phase locked loop has been built on a monolithic integrated circuit. It features a very linear voltage controlled oscillator and a double balanced phase detector.

A simplified schematic of this voltage controlled oscillator is shown in Figure 12. Q_2 is a voltage controlled current source whose collector current is a linear function of the control voltage e_f. Initially Q_5 is OFF and the collector current of Q_2 passes through D_2 and changes C in a linear fashion. The voltage across C is therefore a ramp, and continues to increase until Q_7 is turned ON; this turns OFF Q_8, causing Q_9 and Q_{11} to turn ON. This in turn turns ON Q_5. With Q_5 ON, the anode of D_1 is clamped close to $-V_{CC}$ and D_2 stops conducting, since its cathode is more positive than its anode.

All of the current supplied by Q_2 is diverted through D_1 and Q_3, which sets up an equal current in Q_4. This current is supplied by the charged capacitor C (which now discharges linearly), causing the voltage across it to decrease. This continues until a lower trip point is reached and Q_7 turns OFF and the cycle repeats. Due to the matching of Q_3 and Q_4, the charge current of C is equal to the discharge current and therefore the duty cycle is very nearly 50%. Figure 13 shows the wave forms at (1) and (2).

Figure 14 shows the double balanced phase detector and amplifier used in the microcircuit. Transistors Q_1 through Q_4 are switched with the output

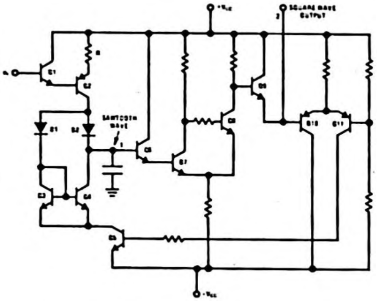


FIGURE 12. Simplified Voltage Controlled Oscillator

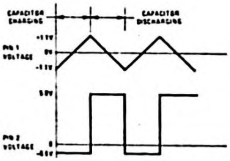


FIGURE 13. VCO Waveforms

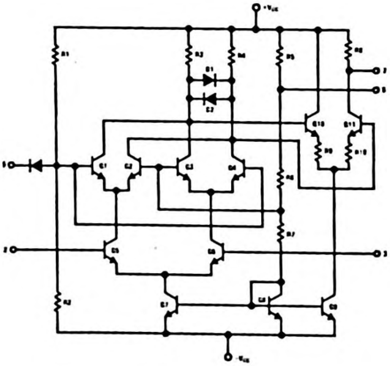


FIGURE 14. Phase Detector and Amplifier

of the VCO, while the input signal is applied to the bases of Q_5 and Q_6. The output current in resistors R_3 and R_4 is then proportional to the difference in phase between the VCO output and the input; the ac component of this current will be at twice the frequency of the VCO due to the full wave switching action transistors Q_1 through Q_4. The waveforms of Figure 15 illustrate how the phase detector works. Diodes D_1 and D_2 serve to limit the peak to peak amplitude of the collector voltage. The output of the phase detector is further amplified by Q_{10} and Q_{11}, and is taken as a voltage at pin 7. R_8 serves as the resistive portion of the loop filter, and additional resistance and capacitance may be added here to fix the loop bandwidth. For use as an FM demodulator, the voltage at pin 7 will be the demodulated output; since the dc level here is fairly high, a reference voltage has been provided so that an operational amplifier with differential input can be used for additional gain and level shifting.

The complete microcircuit, called the LM565, is shown in Figure 16.

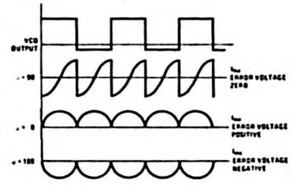


FIGURE 15. Phase Detector Waveforms, Showing Limit Cases for Phase Shift Between Input and VCO Signals

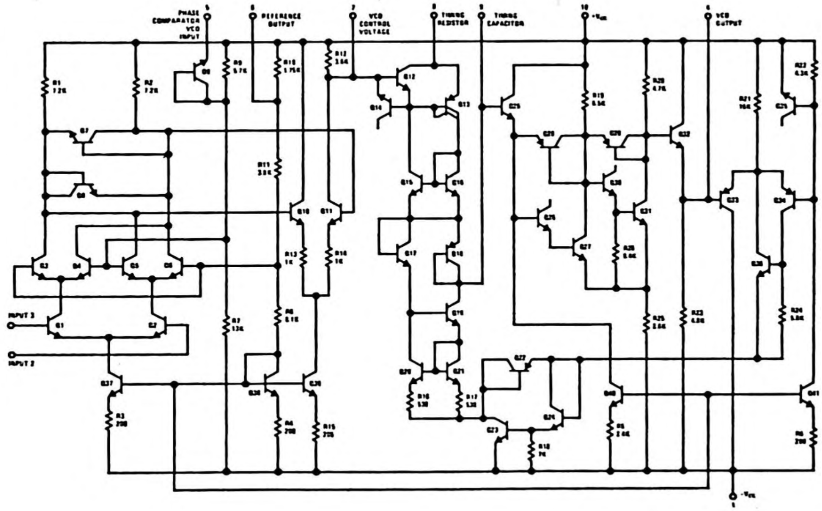

5
PHASE COMPARATOR VCO INPUT
6
REFERENCE OUTPUT
7
VCO CONTROL VOLTAGE
8
TIMING RESISTOR
9
TIMING CAPACITOR
10
+V
4
VCO OUTPUT
INPUT 2
1
-V

FIGURE 16. LM565 Phase Locked Loop

USING THE LM565

Some of the important operating characteristics of the LM565 are shown in the table below. (V_{CC} = ±6V, T_A = 25°C).

Phase Detector	
Input Impedance	5 kΩ
Input Level for Limiting	10 mV
Output Resistance	3.6 kΩ
Output Common Mode Voltage	4.5V
Offset Voltage (Between pins 6 and 7)	100 mV
Sensitivity K_D	.68V/rad
Voltage Controlled Oscillator	
Stability	
Temperature	200 ppm/°C
Supply Voltage	200 ppm/%
Square Wave Output Pin 4	5.4 V_{pp}
Triangle Wave Output Pin 9	2.4 V_{pp}
Maximum Operating Frequency	500 kHz
Sensitivity K_o	4.1 f_o rad/sec/V (f_o: osc. freq in Hz)
Closed Loop Performance	
Loop Gain K_oK_D	2.8 f_o/sec
Demod. Output, ±10% Deviation	300 mV
(A .001 μF capacitor is needed between pins 7 and 8 to stop parasitic oscillations).	

To best illustrate how the LM565 is used, several applications are covered in detail, and should provide insight into the selection of external components for use with the LM565.

IRIG CHANNEL DEMODULATOR

In the field of missile telemetry, it is necessary to send many channels of relatively narrow band data via a radio link. It has been found convenient to frequency modulate this information on a set of subcarriers with center frequencies in the range of 400 Hz to 200 kHz. Standardization of these frequencies was undertaken by the Inter-Range Instrumentation Group (IRIG) and has resulted in several sets of subcarrier channels, some based on deviations that are a fixed percentage of center frequency and other sets that have a constant deviation regardless of center frequency. IRIG channel 13 has been selected as an example of demonstrate the usefulness of the LM565 as an FM demodulator.

IRIG Channel	13
Center Frequency	14.5 kHz
Max Deviation	±7.5%
Frequency Response	220 Hz
Deviation Ratio	5

Since with a deviation of ±10%, the LM565 will produce approximately 300 mV peak to peak output, with a deviation of 7.5%, we can expect an output of 225 mV. It is desirable to amplify and level shift this signal to ground so that plus and minus output voltages can be obtained for frequency shifts above and below center frequency.

An LM107 can be used to provide the necessary additional gain and the level shift. In Figure 17, R_4 is used to set the output at zero volts with no input signal. The frequency of the VCO can be adjusted with R_3 to provide zero output voltage when an input signal is present.

The design of the filter network proceeds as follows:

It is necessary to choose ω_n such that the peak phase error in the loop is less than 90° for all conditions of modulation. Allowing for noise modulation at low levels of signal to noise, a desirable peak phase error might be 1 radian or 57 degrees, leaving a 33 degree margin for noise. Assuming sinusoidal modulation, Figure 6 can be used to estimate the peak normalized phase error. It will be necessary to make several sample calculations, since the normalized phase error is a function of ω_n.

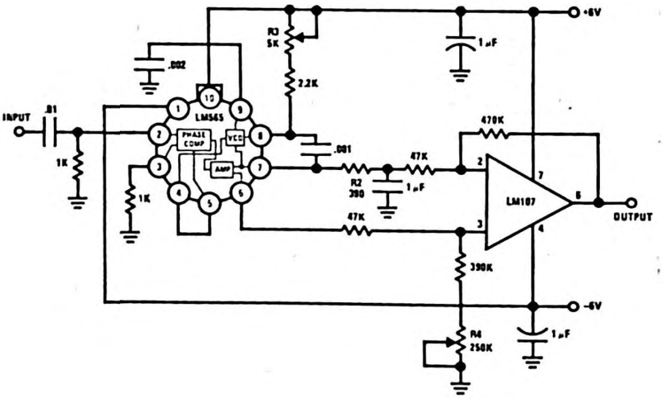


FIGURE 17. IRIG Channel 13 Demodulator

Selecting a worst case of $\omega_n/\omega_m = 1$, $\omega_n = 2\pi \times 220$ Hz; selecting a damping factor of .707,

$$\frac{\theta}{\Delta\omega/\omega_n} = .702$$

or

$$\theta_e = .702\ \frac{\Delta\omega}{\omega_n} = .702\ \frac{2\ \pi \times 1088\ \text{Hz}}{2\ \pi \times 220\ \text{Hz}}$$

$$= 3.45\ \text{radians}$$

this is unacceptable, since it would throw the loop out of lock, so it is necessary to try a higher value of ω_n. Let $\omega_n = 2\pi \times 500$ Hz, then $\omega_m/\omega_n = .44$, and

$$\theta_e = .44\ \frac{\Delta\omega}{\omega_n} = .44 \times \frac{2\ \pi \times 1088}{2\ \pi \times\ 500} = .95\ \text{radians}$$

this should be a good choice, since it is close to radian. Operating at 14.5 kHz, the LM565 has a loop gain K_oK_D of

$$2.8 \times 14.5 \times 10^3 = 33 \times 10^3\ \text{sec}$$

the value of the loop filter capacitor, C_1, can be found from Figure 4:

$$\tau_1 + \tau_2 = 3.5 \times 10^{-3}\ \text{sec}$$

from Figure 5, the value of τ_2 can be found (for a damping factor of .707)

$$\tau_2 = 4.4 \times 10^{-4}\ \text{sec}$$

$$\tau_1 = (35 - 4.4) \times 10^{-4}\ \text{sec} = 31.4 \times 10^{-4}\ \text{sec}$$

$$C_1 = \frac{\tau_1}{R} = \frac{31.4 \times 10^{-4}\ \text{sec}}{3.6\ \text{k}\Omega} \cong 1\ \mu\text{F}$$

$$R_2 = \frac{4.4 \times 10^{-4}\ \text{sec}}{1 \times 10^{-6}\ \mu\text{F}} = 440\ \Omega$$

Looking at Figure 10, the noise bandwidth B_L can be estimated to be

$$B_L = .6\ \omega_n = .6 \times 3150\ \text{rad/sec}$$

$$= 1890\ \text{Hz}$$

the complete circuit is shown in Figure 17. Measured performance of the circuit is summarized below with a fully modulated signal as described above and an input level of 40 mVrms:

f 3 dB	200
ζ	0.8
Output Level	770 mVrms
Distortion	0.4%
Signal to Noise at verge of loss of lock (bandwidth of noise = 100 kHz)	−8.4 dB

It will be noted that the loop is capable of demodulating signals lower in level than the noise; this is not in disagreement with earlier statements that loss of lock occurs at signal to noise ratios of approximately +6 dB because of the bandwidths involved. The above number of −8.4 dB signal to noise for threshold was obtained with a noise spectrum 100 kHz wide. The noise power in the loop will be reduced by the ratio of loop noise bandwidth to input noise bandwidth

$$\frac{B_{LOOP}}{B_{INPUT}} = \frac{1890\ \text{Hz}}{100\ \text{kHz}} = .02\ \text{or} -17\ \text{dB}$$

the equivalent signal to noise in the loop is −8.4 dB +17 dB = +8.6 dB which is close to the above-mentioned limit of +6 dB. It should also be noted that loss of lock was noted with full modulation of the signal which will degrade threshold somewhat (although the measurement is more realistic).

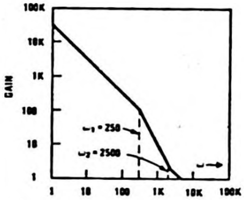


FIGURE 18. Bode Plot for Circuit of Figure 17

FSK DEMODULATOR

Frequency shift keying (FSK) is widely used for the transmission of Teletype information, both in the computer peripheral and communications field. Standards have evolved over the years, and the commonly used frequencies are as follows:

a)	mark	2125	Hz
	space	2975	Hz
b)	mark	1070	Hz
	space	1270	Hz
c)	mark	2025	Hz
	space	2225	Hz

a) is commonly used as subcarrier tones for radio Teletype, while b) and c) are used as carriers for data transmission over telephone and land lines.

As a design example, a demodulator for the 2025 Hz and 2225 Hz mark the space frequencies will be discussed.

Since this is an FM system employing square wave modulation, the natural frequency of the loop must be chosen again so that peak phase errors do not exceed 90° under all conditions. Figure 7 shows peak phase error for a step in frequency; if a damping factor of .707 is selected, the peak phase error is

$$\frac{\theta_e}{\Delta\omega/\omega_n} = .45$$

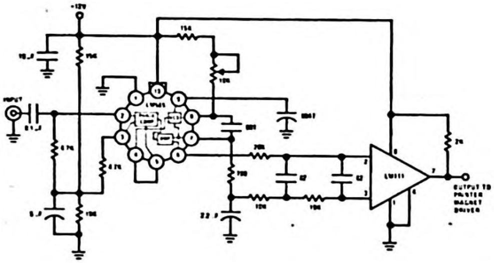


FIGURE 19. FSK Demodulator (2025-2225 cps)

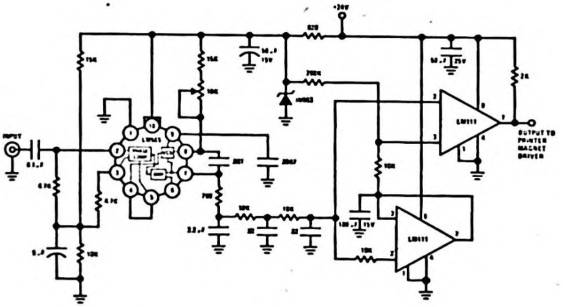


FIGURE 20. FSK Demodulator with DC Restoration

or

$$\theta_e = .45 \frac{\Delta\omega}{\omega_n}$$

$$\omega_n = .45 \frac{\Delta\omega}{\theta_e}$$

in our case, $\Delta\omega = 2\pi \times 200 \text{ Hz} = 1250$, if $\theta_e = 1$ radian,

$$\omega_n = .45 \frac{1250 \text{ rad/sec}}{1 \text{ radian}} = 500 \text{ rad/sec}$$

$$f_n = 80 \text{ Hz}$$

The final circuit is shown in Figure 19. The values of the loop filter components (C_1 = 2.2 μF and R_1 = 700Ω) were changed to accommodate a keying rate of 300 bauds (150 Hz), since the values calculated above caused too much roll off of a square wave modulation signal of 150 Hz. The two 10k resistors and .02 μF capacitors at the input to the LM111 comparator provide further filtering of the carrier, and hence smoother operation of the circuit.

A problem encountered with this simple demodulator is that of dc drift. The frequency must be adjusted to provide zero volts to the input of the comparator so that with modulation, switching occurs. Since the deviation of the signal is small (approximately 10%), the peak to peak demodulated output is only 150 mV. It should be apparent that any drift in frequency of the VCO will cause a dc change and hence may lock the comparator in one state or the other. A circuit to overcome this problem is shown in Figure 20. While using the same basic demodulator configuration, an

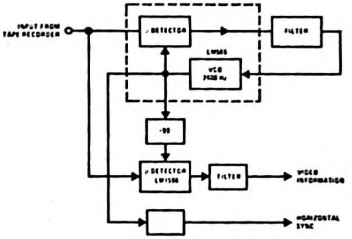

INPUT FROM
TAPE RECORDER
φ DETECTOR
FILTER
LM565
VCO
φ DETECTOR
LM1596
FILTER
VIDEO
INFORMATION
HORIZONTAL
SYNC

FIGURE 21. Block Diagram of Weather Satellite Demodulator

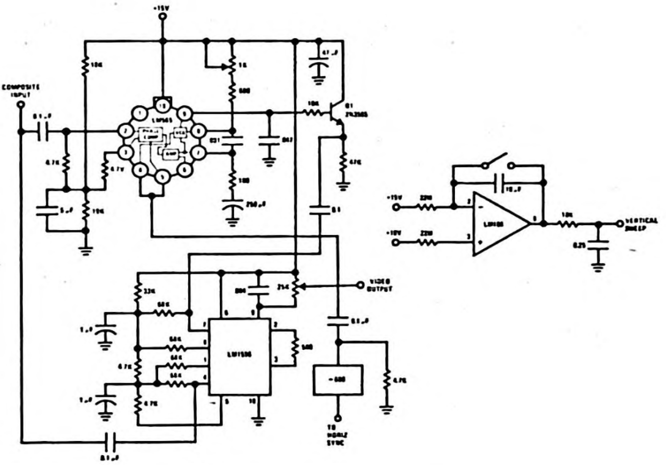

+15V
10k
1k
500
COMPOSITE
INPUT
0.1 μF
LM565
4.7k
10k
100
250 μF
47 μF
Q1
4.7k
0.1
+15V
-15V
LM108
10 μF
10k
0.25
VERTICAL
SWEEP
33k
68k
68k
68k
68k
1 μF
1 μF
4.7k
4.7k
LM1596
500
25k
VIDEO
OUTPUT
0.1 μF
÷600
4.7k
TO
HORIZ
SYNC
0.1 μF

FIGURE 22. Weather Satellite Picture Demodulator

LM111 is used as an accurate peak detector to provide a dc bias for one input to the comparator. When a "space" frequency is transmitted, and the output at pin 7 of the LM565 goes negative and switching occurs, the detected and filtered voltage of pin 3 to the comparator will not follow the change. This is a form of "dc restorer" circuit: it will track changes in drift, making the comparator self compensating for changes in frequency, etc.

WEATHER SATELLITE PICTURE DEMODULATOR

As a last example of how a phase locked loop can be used in communications systems, a weather satellite picture demodulator is shown. Weather satellites of the Nimbus, ESSA, and ITOS series continually photograph the earth from orbits of 100 to 800 miles. The pictures are stored immediately after exposure in an electrostatic storage vidicon, and read out during a succeeding 200 second period. The video information is AM modulated on a 2.4 kHz subcarrier which is frequency modulated on a 137.5 MHz RF carrier. Upon reception, the output from the receiver FM detector will be the 2.4 kHz tone containing AM video information. It is common practice to record the tone on an audio quality tape recorder for subsequent demodulation and display. The 2.4 kHz subcarrier frequency may be divided by 600 to obtain the horizontal sync frequency of 4 Hz.

Due to flutter in the tape recorder, noise during reception, etc., it is desirable to reproduce the 2.4 kHz subcarrier with a phase locked loop, which will track any flutter and instability in the recorder, and effectively filter out noise, in addition to providing a signal large enough for the digital frequency divider. In addition, an in phase component of the VCO signal may be used to drive a synchronous demodulator to detect the video information. A block diagram of the system is shown in Figure 21, and a complete schematic in Figure 22.

The design of the loop parameters was based on the following objectives

$$f_n = 10\text{ Hz}, \omega_n = 75\text{ rad/sec}$$

$$B_L = 40\text{ Hz (from Figure 10)}$$

the complete loop filter, calculated from Figures 4 and 5, is shown in Figure 22. When the loop is in lock and the free running frequency of the VCO is 2.4 kHz, the VCO square wave at pin 4 of the 565 will be in quadrature (90°) from the input signal; however, the zero crossings of the triangle wave across the timing capacitor will be in phase, and if their signal is applied to a double balanced demodulator, such as an LM1596, switching will occur in the demodulator in phase with the 2.4 kHz subcarrier. The double balanced demodulator will produce an output proportional to the amplitude of the subcarrier applied to its signal input. An emitter follower, Q_1, is used to buffer the triangle wave across the timing capacitor so excessive loading does not occur.

The demodulated video signal from the LM1596 is taken across a 25k potentiometer and filtered to a bandwidth of 1.4 kHz, the bandwidth of the transmitted video. Depending on the type of display to be used (oscilloscope, slow scan TV monitor, of facsimile reproducer), it may be necessary to further buffer or amplify the signal obtained. If desired, another load resistor may be used between pin 6 and VCO to obtain a differential output; an operational amp could then be used to provide more gain, level shift, etc.

A vertical sweep circuit is shown using an LM308 low input current op amp as a Miller rundown circuit. The values are chosen to produce an output voltage ramp of −4.5V/220 sec, although this may be adjusted by means of the 22 meg. charging resistor. If an oscilloscope is used as a readout, the horizontal sync can be supplied to the trigger input with the sweep set to provide a total sweep time of something less than 250 ms. A camera is used to photograph the 200 second picture.

SUMMARY AND CONCLUSIONS

A brief review of phase lock techniques has been presented and several useful design tools have been presented that may be useful in predicting the performance of phase locked loops.

A phase locked loop integrated circuit has been described and several applications have been given to illustrate the use of the circuit and the design techniques presented.

REFERENCES

1. Floyd M. Gardner, "Phaselock Techniques", *John Wiley and Sons,* 1966.
2. Elliot L. Greenberg, "Handbook of Telemetry and Remote Control", *McGraw-Hill,* 1967.
3. Andrew Viterbi, "Principles of Coherent Communication", *McGraw-Hill,* 1966.

Applications for a New Ultra-High Speed Buffer

National Semiconductor
Application Note 48
Barry Siegel
Leonard Van Der Gaag
August 1971

INTRODUCTION

Voltage followers have gained in popularity in applications such as sample and hold circuits, general purpose buffers, and active filters since the introduction of IC operational amplifiers. Since they were not specifically designed as followers, these early IC's had limited usage due to low bandwidth, low slew rate and high input current. Usage of voltage followers was expanded in 1967 with the introduction of the LM102, the first IC designed specifically as a voltage follower. With the LM102, engineers were able to obtain an order of magnitude improvement in performance and extend usage into medium speed applications. The LM110, an improved LM102, was introduced in late 1969. However, even higher speeds and lower input currents were needed for very fast sample and holds, A to D and D to A converters, coax cable drivers, and other video applications.

The solution to this application problem was attained by combining technologies into a single package. The result, the LH0033 high speed buffer, utilizes JFET and bipolar technology to produce a ultra-fast voltage follower and buffer whose propagation delay closely approaches speed-of-light delay across its package, while not compromising input impedance or drive characteristics. Table I compares various voltage followers and illustrates the superiority of the LH0033 in both low input current or high speed video applications.

CIRCUIT CONSIDERATIONS

The junction FET makes a nearly ideal input device for a voltage follower, reducing input bias current to the picoamp range. However, FET's exhibit moderate voltage offsets and offset drifts which tend to be difficult to compensate. The simple voltage follower of Figure 1 eliminates initial offset and offset drift if Q_1 and Q_2 are identically matched transistors. Since the gate to source voltage of Q_2 equals zero volts, then Q_1's gate to source voltage equals zero volts. Furthermore as V_{P1} changes with temperature (approximately 2.2 mV/°C), V_{P2} will change by a corresponding amount. However, as load current is drawn from the output, Q_1 and Q_2 will drift at different rates. A circuit which overcomes offset voltage drift is used in a new high speed buffer amplifier, the LH0033. Initial offset is typically 5 mV and offset drift is 20 μV/°C. Resistor R_2 is used to establish the drain current of current source transistor, Q_2 at 10 mA.

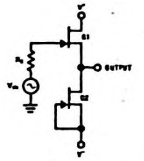


FIGURE 1. Simple Voltage Follower Schematic

The same drain current flows through Q_1 causing a voltage at the source of approximately 1.1V. The 10 mA flowing through R_1 plus Q_3's V_{BE} of 0.6V causes the output to sit at zero volts for zero volts in. Q_3 and Q_4 eliminate loading the input stage (except for base current) and CR_1 and CR_2 establish the output stage collector current.

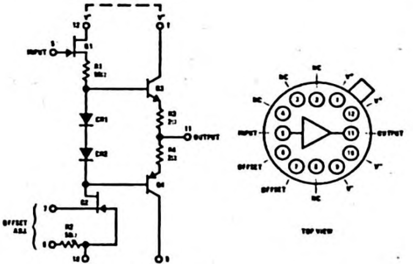


FIGURE 2. LH0033 Schematic

If Q_1 and Q_2 are matched, the resulting drift is reduced to a few μV/°C.

TABLE I COMPARISON OF VOLTAGE FOLLOWERS

PARAMETER	CONVENTIONAL MONOLITHIC OP AMP LM741	FIRST GENERATION VOLTAGE FOLLOWER LM102	SECOND GENERATION VOLTAGE FOLLOWER LM110	SPECIALLY DESIGNED VOLTAGE FOLLOWER LH0033
INPUT BIAS CURRENT	200 nA	3.0 nA	1.0 nA	0.05 nA
SLEW RATE	0.5V/μs	10V/μs	30V/μs	1500V/μs
BANDWIDTH	1.0 MHz	10 MHz	20 MHz	100 MHz
PROP. DELAY TIME	350 ns	35 ns	18 ns	1.2 ns
OUTPUT CURRENT CAPABILITY	±5 mA	±2 mA	±2 mA	±100 mA

PERFORMANCE OF THE LH0033 FAST VOLTAGE FOLLOWER/BUFFER

The major electrical characteristics of the LH0033 are summarized in Table II. All the virtues of a ultra-high speed buffer have been incorporated. Figure 3 is a plot of input bias current vs temperature and shows the typical FET input characteristics. Other typical performance curves are illustrated in Figures 4 through 10. Of particular interest is Figure 8, which demonstrates the performance of the LH0033 in video applications to over 100 MHz.

TABLE II

PARAMETER	CONDITIONS	VALUE	PARAMETER	CONDITIONS	VALUE
Output Offset Voltage	R_S = 100 kΩ	5 mV	Output Current Capability		±100 mA peak
Input Bias Current		50 pA	Slew Rate	R_S = 50Ω, R_L = 1k	1500V/μs
Input Impedance	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz	10^{11} Ω	Propagation Delay		1.2 ns
Voltage Gain	V_{IN} = 1.0 Vrms R_L = 1k, f = 1 kHz, R_S = 100k	0.98	Bandwidth	V_{IN} = 1.0 Vrms R_S = 50Ω, R_L = 1k	100 MHz
Output Voltage Swing	V_S = ±15V, R_S = 100k R_L = 1k	±13V			

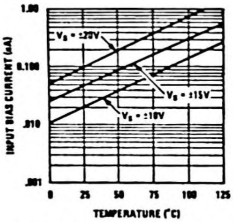


FIGURE 3. Input Bias Current vs Temperature

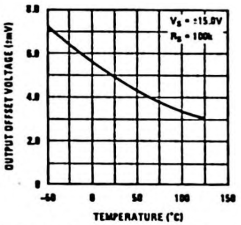


FIGURE 4. Output Offset Voltage vs Temperature

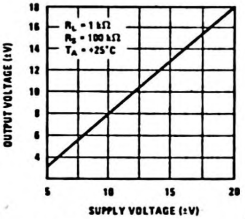


FIGURE 5. Output Voltage vs Supply Voltage

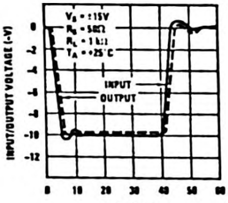


FIGURE 6. Negative Pulse Response

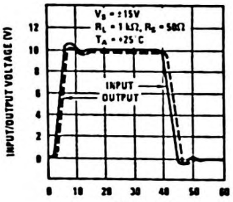


FIGURE 7. Positive Pulse Response

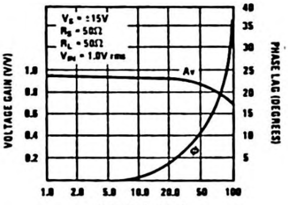


FIGURE 8. Frequency Response

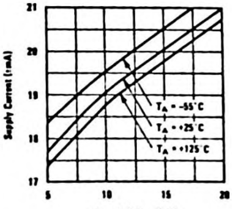


FIGURE 9. Supply Current vs Supply Voltage

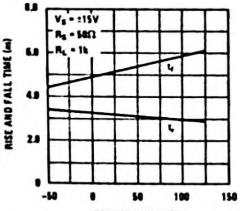


FIGURE 10. Rise and Fall Time vs Temperature

APPLICATIONS FOR ULTRA-FAST FOLLOWERS

The LH0033's high input impedance (10^{11} Ω, shunted by 2 pF) and high slew rate assure minimal loading and high fidelity in following high speed pulses and signals. As shown below, the LH0033 is used as a buffer between MOS logic and a high speed dual limit comparator. The device's high input impedance prevents loading of the MOS logic signal (even a conventional scope probe will distort high output impedance MOS). The LH0033 adds about a 1.5 ns to the total delay of the comparator. Adjustment of voltage divider R_1, R_2 allows interface to TTL, DTL and other high speed logic forms.

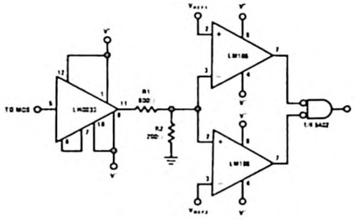


FIGURE 11. High Speed Dual Limit Comparator for MOS Logic

The LH0033 was designed to drive long cables, shielded cables, coaxial cables and other generally stringent line driving requirements. It will typically drive 200 pF with no degradation in slew rate and several thousand pF at a reduced rate. In order to prevent oscillations with large capacitive loads, provision has been made to insert damping resistors between V^+ and pin 1, and V^- and pin 9. Values between 47 and 100Ω work well for $C_L > 1000$ pF. For non-reactive loads, pin 12 should be shorted to pin 1 and pin 10 shorted to pin 9. A coaxial driver is shown in Figure 13. Pin 6 is shorted to pin 7, obtaining an initial offset of 5.0 mV, and the 43Ω coupled with the LH0033's output impedance (about 6Ω) match the coaxial cable's characteristic impedance. C_1 is adjusted as a function of cable length to optimize rise and fall time. Rise time for the circuit as shown in Figure 12, is 10 ns.

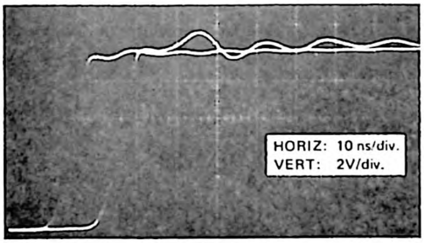


FIGURE 12. LH0033 Pulse Response into 10 Foot Open Ended Coaxial Cable

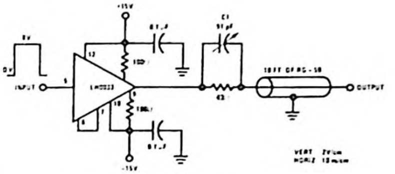


FIGURE 13.

Another application that utilizes the low input current, high speed and high capacitance drive capabilities of the LH0033 is a shield or line driver for high speed automatic test equipment. In this example, the LH0033 is mounted close to the device under test and drives the cable shield thus allowing higher speed operation since the device under test does not have to charge the cable.

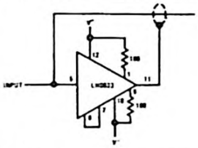


FIGURE 14. Instrumentation Shield/Line Driver

The LH0033's high input impedance and low input bias current may be utilized in medium speed circuits such as Sample and Hold, and D to A converters. Figure 15 shows an LH0033 used as a buffer in medium speed D to A converter.

Offset null is accomplished by connecting a 100Ω pot between pin 7 and V^-. It is generally a good idea to insert 20Ω in series with the pot to prevent excessive power dissipation in the LH0033 when the pot is shorted out. In non-critical or AC coupled applications, pin 6 should be shorted to pin 7. The resulting output offset is typically 5 mV at 25°C.

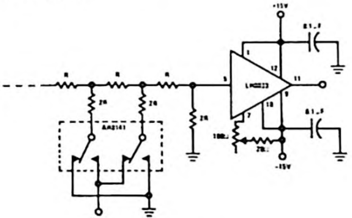


FIGURE 15.

The high output current capability and slew rate of the LH0033 are utilized in the sample and hold circuit of Figure 16. Amplifier, A1 is used to buffer high speed analog signals. With the configuration shown, acquisition time is limited by the time constant of the switch "ON" resistance and sampling capacitor, and is typically 200 or 300 ns. A_2's low input bias current, results in drifts in hold mode of $\frac{50\text{ mV}}{\text{sec}}$ at 25°C and $\frac{1\text{V}}{\text{sec}}$ at 125°C.

The LH0033 may be utilized in AC applications such as video amplifiers and active filters. The circuit of Figure 17 utilizes boot strapping to achieve input impedances in excess of 10 MΩ.

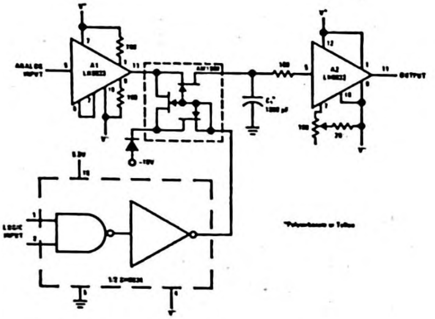


FIGURE 16. High Speed Sample & Hold

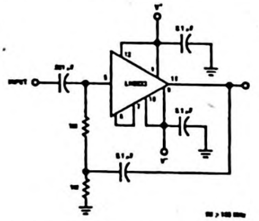


FIGURE 17. High Input Impedance AC Coupled Amplifier

A single supply, AC coupled amplifier is shown in Figure 18. Input impedance is approximately 500k and output swing is in excess of 8V peak-to-peak with a 12V supply.

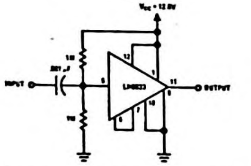


FIGURE 18. Single Supply AC Amplifier

The LH0033 may be readily used in applications where symmetrical supplies are unavailable or may not be desirable. A typical application might be an interface to an MOS shift register where $V^+ = 5.0V$ and $V^- = -25V$. In this case, an apparent output offset occurs. In reality, the output voltage is due to the LH0033's voltage gain of less than unity. The output voltage shift due to asymmetrical supplies may be predicted by:

$$\Delta V_O \cong (1 - Av)\frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where: Av = No load voltage gain, typically 0.99.

V^+ = Positive Supply Voltage.

V^- = Negative Supply Voltage.

For the foregoing application, ΔV_O would be −100 mV. This apparent "offset" may be adjusted to zero as outlined above.

Figure 19 shows a high Q, notch filter which takes advantage of the LH0033's wide bandwidth. For the values shown, the center frequency is 4.5 MHz.

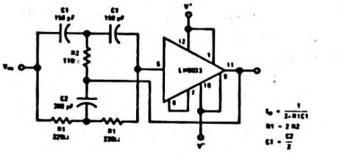


FIGURE 19. 4.5 MHz Notch Filter

The LH0033 can also be used in conjunction with an operational amplifier as current booster as shown in Figure 20. Output currents in excess of 100 mA may be obtained. Inclusion of 150Ω resistors between pins 1 and 12, and 9 and 10 provide short circuit protection, while decoupling pins 1 and 9 with 1000 pF capacitors allow near full output swing.

The value for the short circuit current is given by:

$$I_{SC} \cong \frac{V^+}{R_{LIMIT}} = \frac{V^-}{R_{LIMIT}}$$

where: $I_{SC} \leq 100$ mA.

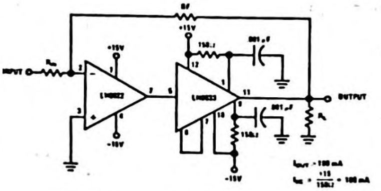


FIGURE 20. Using LH0033 as an Output Buffer

SUMMARY

The advantages of a FET input buffer have been demonstrated. The LH0033 combines very high input impedance, wide bandwidth, very high slew rate, high output capability, and design flexibility, making it an ideal buffer for applications ranging from DC to in excess of 100 MHz.

AN-51 A Unique Monolithic AGC/Squelch Amplifier

A Unique Monolithic AGC/Squelch Amplifier

National Semiconductor
Application Note 51
Todd Smathers
September 1971

INTRODUCTION

As complexity and usage of communication systems increases, there is a growing use of a special class of circuitry, designed to make the system more convenient to the user, as well as allowing it to adapt to changes in the transmission channel. The most common function is voltage-variable gain, used in volume compression and expansion, and a specialized case, squelch, in which gain remains either in its maximum or minimum state.

The main problem in such circuitry is finding a suitable nonlinear element to do the job. Conventional elements, appearing in Table 1, share common problems of distortion, cost, limited signal handling capability, sometimes limited gain reduction range, and usually insert unwanted transients onto the signal during periods of rapid gain changing. Two mechanisms may be defined for these elements; either effective resistance or effective transconductance is varied by the DC control voltage. Because the variation is accomplished by changing quiescent operating points, DC decoupling is required at the output, and only AC signals may be handled. DC decoupling, however, still allows rapid changes in DC operating point to be transmitted as switching transients. While linearity is claimed for FET and the lamp-photocell schemes, such linearity is still only part of a large-signal nonlinear characteristic. With any of the elements, quasi-linearity is obtained by traversing a small segment of the overall element range; hence, variable gain elements must precede any system voltage gain.

TABLE 1. Conventional Gain Control Elements

ELEMENT	MECHANISM	CONTROL RANGE	CONTROL/ OUTPUT ISOLATION	LARGE SIGNAL HANDLING	COMMENTS
P-N Junction	Forward Resistance	Good	Poor	Poor	Simple, predictable
Bipolar Transistor	Saturation Resistance	Fair	Poor	Fair	Beta Dependent
FET	Channel Resistance	Good	Poor	Fair	Unpredictable gate control voltage requirements; for driving fairly high impedance loads
Photocell-Lamp	Photocell Resistance	Good	Good	Good	Requires power to drive lamp; cell must be shielded from ambient light
FET	Transconductance	Fair	Poor	Poor	Unpredictable gate control voltage requirements; for driving fairly high impedance loads
Bipolar Transistor	Transconductance	Fair	Poor	Poor	Commonly used in AM-IF applications
Tetrode Vacuum Tube	Transconductance	Fair	Poor	Good	Filament Power

A MONOLITHIC APPROACH

Because of the inexpensive complexity possible with monolithic construction, techniques may be used which circumvent many of the shortcomings of discrete gain control circuits. The balanced diode attenuator of Figure 1 allows variable series-shunt attenuation, and if used in a differential circuit, with monolithic matching, can cancel all spurious control-signal effects at the output. Figure 2 gives a subsystem block diagram, for effectively controlling the balanced arrangement of Figure 1. An input differential amplifier provides differential diode drive even if only single ended inputs are available, and keeps the common-mode DC level to Q_3 and Q_6 at a constant level. Notice that emitter followers have been substituted for simple diodes, giving higher input impedance, and superior gain reduction range. The input diff.-amp. also prevents gain changes from affecting the input impedance. Since the control elements are quasi-linear only for small signal voltages, the input diff.-amp. has unity gain, with all circuit gain being performed after the variable elements.

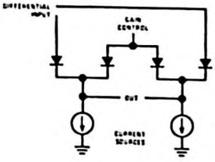

DIFFERENTIAL INPUT
GAIN CONTROL
OUT
CURRENT SOURCES

FIGURE 1. Balanced Diode Attenuator

A feedback circuit senses common-mode output from the emitter followers, and compares it with the DC control voltage, to reliably set attenuation characteristics. For maximum gain, Q_3 and Q_6 behave as ordinary emitter followers. As the control voltage rises, Q_4 and Q_5 begin to conduct, effectively "robbing" Q_3 and Q_6 of available DC emitter current. Consequently, dynamic emitter resistances of Q_3 and Q_6, in series with the signal, increase, while those of Q_4 and Q_5 decrease, shunting across the signal. In the limit, Q_3 and Q_6 are completely cut off, and the shunt pair fully conducting.

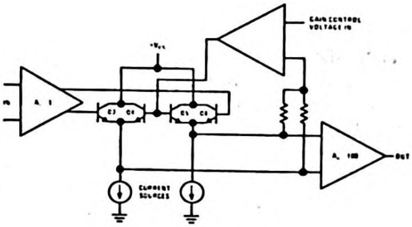

GAIN CONTROL VOLTAGE IN
+Vcc
IN
A, 1
Q3
Q4
Q5
Q6
CURRENT SOURCES
A, 100
OUT

FIGURE 2. System Block Diagram

Emitter follower output is fed into a differential input, single-ended output amplifier, where common-mode changes resulting from the gain control voltage are rejected, and the signal is amplified to usable levels. Thus, the system is a variable gain DC amplifier.

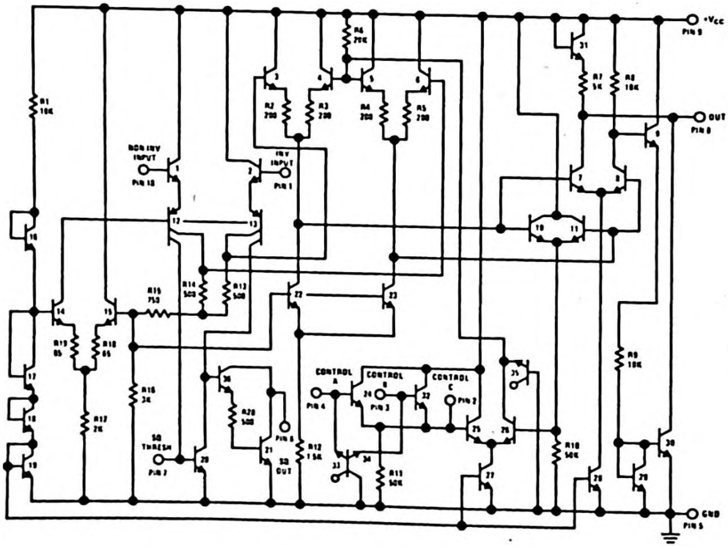

+Vcc
PIN 9
OUT
PIN 8
GND
PIN 5
NON INV INPUT
PIN 10
INV INPUT
PIN 1
CONTROL A
PIN 4
CONTROL B
PIN 3
CONTROL C
PIN 2
SQ THRESH
PIN 7
PIN 6
SQ OUT
R1 10K
R2 200
R3 200
R4 200
R5 200
R6 20K
R7 5K
R8 10K
R9 10K
R10 50K
R11 50K
R12 1.5K
R13 500
R14 500
R15 750
R16 3K
R17 2K
R20 500

FIGURE 3. LM170 Schematic

MONOLITHIC REALIZATION

A practical version of Figure 2's block diagram, National's LM170 appears as a schematic in Figure 3. Despite its apparent complexity, and its use of 34 junction devices and 20 resistors, the entire circuit has been compressed onto a 39 x 42 mil monolithic chip, Figure 4, smaller than most operational amplifiers.

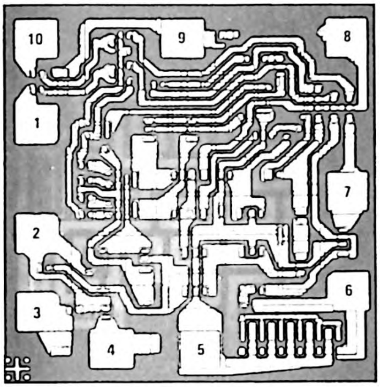


FIGURE 4. LM170 Chip

Examining first the input circuit, Figure 5, one may notice that the configuration is essentially that of the highly successful LM101 operational amplifier. Emitter followers, Q_1 and Q_2, combine with an unusual lateral PNP configuration, Q_{12} and Q_{13}, to allow large common-mode input range (up to and including the positive supply voltage), low input offset voltage, and the ability to withstand large differential input overvoltages without damage. Common-mode feedback to a differential current source, Q_{14} and Q_{15}, along with a stable, diode determined reference, automatically biases the differential input configuration to give constant and predictable DC common-mode output voltage, despite variations in the relatively unpredictable lateral PNP "beta". The input circuit draws constant power supply current regardless of power supply voltage, and consequently exhibits predictable input impedance and bias currents.

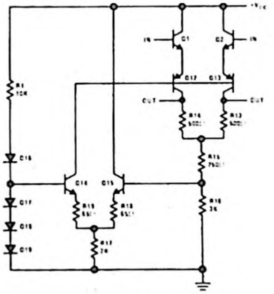


FIGURE 5. LM170 Input Differential Amplifier

The gain control circuit, Figure 6, operates as outlined in Figure 2; Q_{25}, Q_{26} and Q_{27} form the control feedback amplifier; Q_{22} and Q_{23} are matched constant current sources, whose operation is stabilized by the same circuit that regulates the input stage. Rather than obtain a common-mode feedback voltage with resistors as in Figure 2, Q_{10} and Q_{11} are used, saving chip space reducing emitter follower loading, and giving a fixed voltage drop at the summing point. Two emitter followers, Q_{24} and Q_{32} are available as gain control inputs, allowing considerable control versatility, and may be used as peak detectors, as well. Control input overvoltage protection is provided by zener diodes (reverse base-emitter junctions), Q_{33} and Q_{34}, while feedback amplifier excursion is limited by another zener, Q_{35}. Bias levels are set so that AGC action begins when the applied control voltage equals three forward diode drops, about +2.1V. As control voltage is further increased, gain is reduced by progressively shunting current from Q_3 and Q_6 into Q_4 and Q_5; the "transition width" of the system is about 400 mV, so that above approximately +2.5V, minimum gain is obtained. These control levels were chosen to be compatible with tuned gain control amplifiers, such as the LM171 RF/IF amplifier, elsewhere in the system, and to allow the circuit to be driven, in switched-gain applications, by standard monolithic 5V logic, such as TTL, DTL, or RTL.

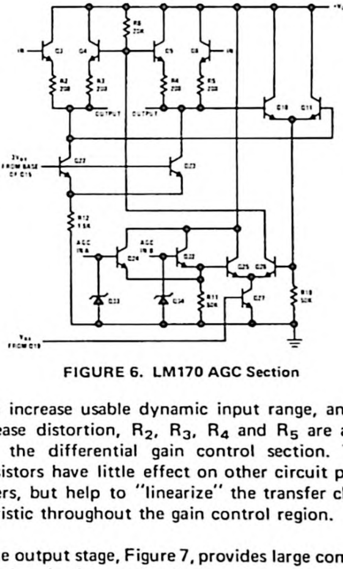


FIGURE 6. LM170 AGC Section

To increase usable dynamic input range, and decrease distortion, R_2, R_3, R_4 and R_5 are added to the differential gain control section. These resistors have little effect on other circuit parameters, but help to "linearize" the transfer characteristic throughout the gain control region.

The output stage, Figure 7, provides large common-mode rejection, and a single-ended output, which has a quiescent value halfway between ground and the positive supply. Output stage voltage gain is a function of supply voltage, being approximately 100 (40 dB) at V_{CC} = 12V. Thus, except for its lower gain, the LM170 has the same configuration and essential characteristics as an operational amplifier.

Output impedance is intentionally high (5000 ohms), and short-circuit resistant. Thus, any num-

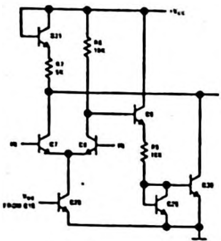


FIGURE 7. LM170 Output Stage

ber of LM170's may be directly tied together at their outputs, for multi-channel mixing or switching applications.

For AGC systems, output signal voltage is usually peak-detected, and fed back to the gain control input, maintaining essentially constant output voltage with widely varying input signals. In the case of squelch, however, the output is normally completely off, in the absence of input signals; thus, control voltage for squelch operation cannot be derived from the output, but must be sampled before the gain-reduction stage. Figure 8 shows the built-in squelch amplifier and detector. Lateral PNP transistors Q_{12} and Q_{13} are constructed with two collectors each, so that differential signals drive the gain control stage, across R_{13} and R_{14}, and separately, from the second pair of collectors, drive Q_{20}, Q_{36}, and Q_{21}. The quiescent current from the extra collectors is regulated by the same feedback circuit that controls operation of the input stage. If an external resistor (or potentiometer) is connected from Pin 7 to ground, it will serve as collector load for Q_{12}, and can be user adjusted so that Q_{20}, normally saturated, turns off for peak signal voltages exceeding any desired value. When this happens, Q_{36} and Q_{21} turn on, discharging an external capacitor, and bringing the voltage at Pin 6 below the threshold required to turn the amplifier fully on. Since the collector load for Q_{20} is a current source, in parallel with a high impedance Darlington pair, Q_{36} and Q_{21}, the voltage gain of the squelch detector is very high, and abrupt action occurs with even small incoming signals.

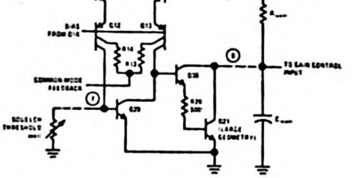


FIGURE 8. LM170 Squelch Detector

The external capacitor and large charging resistor can be chosen for time constants up to several seconds, for releasing the squelch; the geometry of Q_{21}, however, is large, allowing a very fast discharge of the time constant capacitor, so that effective fast-attack, slow-release squelch occurs. Since Q_{21} is part of a Darlington, and has a base current limiting resistor, R_{20}, it will neither saturate nor damage itself when large electrolytic capacitors are used; however, it will draw sufficiently large currents to bring the capacitor below the 2.1V gain control threshold, and then taper off in discharge rate.

GENERAL APPLICATION CONSIDERATIONS

As with any device capable of producing gain, when using the LM170, consideration must be given to proper layout of the device and its external circuitry to prevent any undesirable feedback that may cause oscillation. Since the inputs may be biased either directly from V_{CC} or indirectly through a divider network, effective power supply bypassing is essential. To guarantee effective bypassing at all frequencies, multiple bypassing should be used. A large capacitor, 10 μF or greater, should be used to absorb all low frequency power supply variations and a smaller capacitor, approximately .01 μF, to prevent any high frequency feedback through V_{CC}. These should be located as physically close to the device as possible.

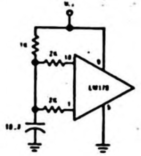


FIGURE 9. Input Biasing and Decoupling Network

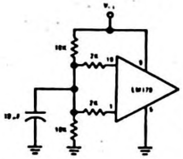


FIGURE 10. Input Biasing and Decoupling Network

Additional DC input stability may be necessary. This is most easily accomplished by a series RC roll-off from V_{CC} to the inputs to ground. If the inputs are to be biased directly from V_{CC}, the network should be connected as in Figure 9. Values of 1k ohms and 10 μF give a roll-off that is 3 dB down, at approximately 17 Hz. Since the input bias current is typically around 8.0 μA, the voltage drop across the 1k ohm resistor will be negligible. If the inputs are biased at some common mode voltage less than V_{CC}, then the addition of a single capacitor from the common mode input point to ground accomplishes the same thing (see Figure 10). Again, a value of approximately 10 μF will give effective roll-off.

The input stage exhibits the same high tolerance to abuse as does the LM101; large currents forced into either input (when input voltage exceeds the positive supply by more than 0.7V, for example) should be avoided. If such transients normally occur in the system, as frequently is the case during turn on or turn off, protect the inputs with series input resistance.

An inspection of the self-balancing action within the LM170 explains how large gain changes can be achieved, without appreciable DC output shift. Obviously, if all components in the circuit are exactly matched, this will work perfectly. There are two possible sources of DC output shift in the LM170. The first is an unavoidable small V_{BE} mismatch between critical components, causing small differential shifts to appear ahead of the output gain stage, along with the usual large common-mode shifts. Units are selected, to various specifications, at the factory, for low output shift. The second source of DC shift is externally induced input offset voltage. As with any operational-type amplifier, a certain bias current must flow into each input, in the microampere range, to operate the input transistors. While input offset current (the difference between the two input currents) is very low, use of unequal source resistances will cause different voltage drops across each input resistor or a net input offset voltage. For critical applications, then, especially if large input resistance is used, it is recommended that equal input resistors be used. Conversely, if the least expensive graded units are used, and minimum output shift is still of importance, input offset voltage may be individually trimmed for each unit, to give nearly ideal characteristics, as observed on an oscilloscope.

Another serious source of offset can occur when a large capacitor is used to couple to the input of the LM170. This may cause brief periods of positive feedback during a portion of the input waveform cycle, during which the device may oscillate. This may be easily prevented, however, by connecting a capacitor of approximately the same value as the input capacitor from the unused input terminal to ground.

Gain control inputs, Pins 3 and 4, are shunted by 6.5V zener diodes. If control voltage is anticipated to go above +6.5V, and if the driving source is capable of providing more than about 10 mA under these conditions, it is advisable to protect the zeners with a series resistance at each gain control input.

While the large geometry squelch output transistor, Q_{21}, is capable of sinking large instantaneous discharge currents from electrolytic capacitors, it is not advisable to attempt sinking large (more than 50 or 100 mA) continuous currents from "stiff" voltage sources, which may cause large dissipation on the chip.

The LM170's ability to accept common-mode input voltage equal to the positive supply can be a great convenience to the circuit designer, and saves several components, in such applications as direct dynamic microphone drive. It should be realized, however, that this system works only with the small (under 100 mV) input signals for which the circuit was intended. While input transistors Q_1 and Q_2 still are effective as emitter followers with zero, and even less than zero volts collector-to-base, large positive base voltages (more than about 400 mV above the positive supply, will allow Q_1 and Q_2 to saturate, degrading amplifier gain, input impedance, bandwidth, and input bias current. Normal operation should never see more than about 50 mV of input signal, so that this is not a problem.

AGC APPLICATIONS

AGC Using Built in Detectors

In most systems, the LM170 will be followed by further voltage amplification. This may be advantageous, as it can provide increased forward gain in the AGC loop, resulting in tighter output regulation. In systems having widely varying load impedances, AGC derived from the system output can automatically compensate for additional output loading. Connected as in Figure 11, the emitter follower at Pin 4 is used as a high impedance detector, with detector smoothing performed by a capacitor at Pin 2. DC threshold for the detector is set at any desired level by a potentiometer, determining the positive peak output voltage which initiates gain regulation.

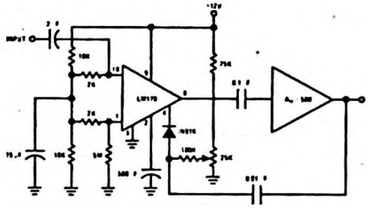


FIGURE 11. LM170 AGC Using Internal Peak Detector and Additional System Gain

A word of caution is necessary here. When operating the LM170 with an external gain stage to provide very high AGC loop gains (on the order of several hundred), proper layout is essential. As with any high gain circuitry, good power supply regulation is a necessity. Multiple bypass capacitors are used (Figure 11) to give effective wide band filtering. This should prevent any undesirable ripples or transient spikes from being transferred from one device to another through V_{CC}.

Depending on the amount of external loop gain desired, several other steps may be necessary. As with many other AGC circuits, there is a DC shift in output voltage associated with the change in applied AGC control voltage. If this shift is fast enough and of sufficient magnitude, it may be coupled from the output of the LM170 to the following gain stage. This may cause severe spiking in the output of the LM170 which may swing the gain stage into limiting causing extreme distortion. This can be prevented by providing a given amount of offset in a given direction to the input of the LM170. If an increase in AGC voltage at the AGC threshold causes a positive shift in output voltage, it may be fed back through the system to cause a further increase in AGC control voltage. If, however, an increase in AGC voltage causes a negative shift in output voltage, when this shift is fed back it will tend to decrease AGC voltage which should help to prevent the spike from occurring. In normal application, the LM170 inputs are biased with approximately 2 kΩ resistors. If a resistor on the order of 5 MΩ is tied from the inverting input (Pin 1) to ground, it will provide enough offset to control both the direction and magnitude of the output shift. A potentiometer may be substituted to trim the offset to any desired value.

The other problem that may occur can result from too large an AC swing at the AGC control point. Pins 3 and 4 are protected from positive over voltages by a 6.3V zener. If the AC swing is so large that it swings negative below .7V, the zener will be forward biased. If this occurs, a parasitic NPN transistor can be formed causing an undesired transistor action. To prevent this, two solutions are available. In the first a germanium diode can be used to shunt all negative swings from the AGC pin to ground. It is tied directly from the AGC pin (Pin 3 or Pin 4) to ground, being forward biased if the AC signal tries to swing negative. The alternate method, as shown in Figure 11 is a silicon diode in series with the AGC pin. It is forward biased for all positive voltages so DC bias is provided and all positive going AC swings provide proper AGC action. All negative swing are promptly cut off at +0.7V.

Care should be taken to avoid exposing the circuit to any RF radiation or 60 Hz power line fields as they may get into the high gain loop and cause erratic AGC action. Coupling capacitors should be selected to give proper operation over the desired range of frequencies. In Figure 11, the low frequency limiting factor is the .01 AGC feedback capacitor which gives a roll off near 160 Hz. Increasing its size would proportionally lower the low frequency cutoff.

Figure 12 shows the output regulation resulting from this system with an added 46 dB of voltage gain following the LM170.

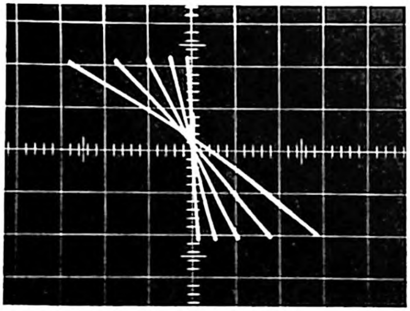


FIGURE 12. AGC Transfer Characteristics, Internal Detector, For Varying Inputs

Vert. = output, 10 mV/cm
Horiz. = input, 10 mV/cm

Both available AGC inputs may be used, as in Figure 13, to provide full-wave output detection, which responds to both positive and negative output peak voltages.

If a transformer is used to provide full wave AGC detection as shown in Figure 13, it must be chosen to meet two criteria. First, it must have a high enough input impedance to avoid loading down the output of the LM170 or of following gain stages if they are used. If driven directly from the output of the LM170, a primary impedance greater than 50 kΩ is acceptable. Figure 14 shows that AGC voltage inputs greater than approximately 2.5V will provide maximum available gain reduction. Therefore if the transformer output provides a voltage swing of approximately 3V peak, it will be more than adequate to operate the LM170 over its entire AGC range.

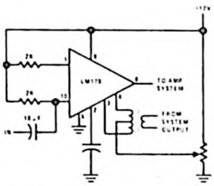


FIGURE 13. Internal Full Wave AGC Detection

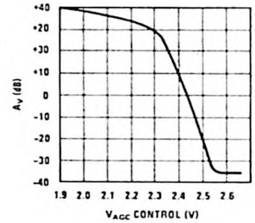


FIGURE 14. Typical Voltage Gain vs AGC Control Voltage (Pin 3 or Pin 4)

AGC CIRCUIT WITH TRANSISTOR DETECTOR

In Figure 15, an external PNP transistor acts as a negative peak detector, with threshold set by a potentiometer. In its quiescent state, the PNP transistor is off; negative going signal peaks, AC coupled to the detector, cause momentary conduction, which turns on the high impedance gain control input, Pin 4. Pin 2 is bypassed by a relatively large capacitor which will charge, and maintain a sufficient DC voltage to operate the amplifier's gain at the correct level. This level, set by the threshold potentiometer, is the point at which negative peaks marginally turn on the PNP transistor. Thus, as input signal level increases, the circuit automatically lowers gain, to maintain a constant peak-to-peak output level. Since the capacitor at Pin 2 cannot follow instantaneous audio

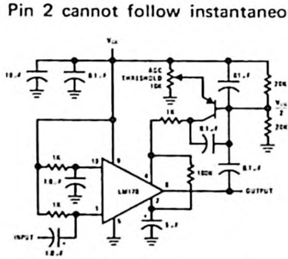


FIGURE 15. AGC Circuit with External Peak Detector

variations, audio frequency linearity is not disturbed, although charging from the low impedance of Pin 2 and discharging through a much higher resistance, causes fast attack, slow release AGC action.

In this example, common-mode input bias is obtained directly from V_{CC}, through equal resistors, to minimize offsets resulting from input bias current.

The family of transfer characteristics, Figure 16, shows that some output increase occurs as the input increases, but by only a small percentage.

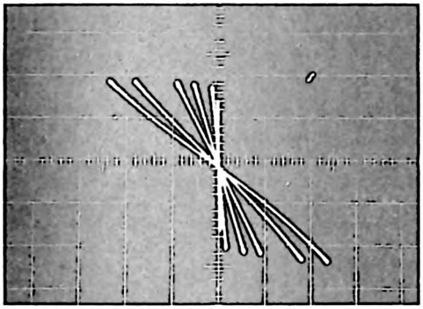


FIGURE 16. AGC Transfer Characteristics Transistor Detector, For Varying Inputs

Vert. = output, 10mV/cm
Horiz. = input, 10mV/cm

When using an external peak detector, proper layout and biasing are essential to prevent the transistor from oscillating. As always multiple bypassing of the power supply should be used. In addition, a capacitor of approximately .01 µF should be connected from the base of the PNP to the collector and from the base to V_{CC}. These prevent any positive feedback from causing the external peak detector to oscillate.

SQUELCH APPLICATIONS

Squelch Preamplifier with Hysteresis

Audio squelch is useful in noisy acoustic environments, to suppress background microphone noises, and in receiving systems, where the constant clatter of an unused transmission channel must be removed, until useful information is received. The squelch circuit of Figure 17 includes a number of refinements, which make it smooth-acting, and easy on the ear of the listener.

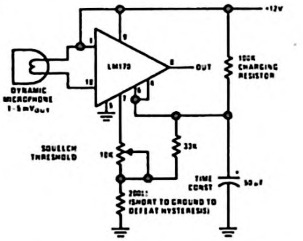


FIGURE 17. Squelched Preamplifier with Hysteresis

The threshold potentiometer at Pin 7 is manually set to cut in at any desired input level. The large capacitor at Pin 6, and its associated charging resistor, may be chosen to give squelch release times of as much as several seconds, while the large current sinking capability into Pin 6 assures fast attack, so that first speech syllables are not lost.

A portion of the voltage at Pin 6 is fed back to the threshold potentiometer; since there are two stable voltage states at Pin 6, this creates a controlled amount of hysteresis in the squelch circuit. Thus, there exists a "dead band" of squelch sensitivity, which greatly enhances the circuit's immunity to rapid transmission channel fading, or erratic speech patterns. Combined with the slow-release characteristic, hysteresis gives a very well-behaved squelch system. A typical threshold control setting might be one at which amplification begins above a 20 mV p-p input. With the feedback values shown, the input level must consistently stay below 12 mV p-p before gain is cut off. The small feedback resistor may be eliminated if hysteresis is not required.

While squelch attack is abrupt, release follows the slow charging contour of the time constant capacitor, through the logarithmic gain control region. Thus, gain "fades out" following cessation of speech, rather than the less ear-pleasing effect of conventional squelch circuits, in which a rush of background noise may be heard, followed by an abrupt and often percussive cutoff.

The time constant capacitor is charged by a voltage divider, rather than a single resistor, so that its quiescent charged voltage is about +3V, with the values shown, from a +12V supply. There is no need to charge the capacitor much above this point, because gain has already been completely cut off, and further charging only makes more work for the large geometry transistor at Pin 6, in performing its rapid discharge function. In any event, if a single charging resistor is used, the timing capacitor cannot charge above about +6.5V, because both Pins 3 and 4 are shunted internally by protective zener diodes.

In Figure 17, the LM170 appears in another of its many possible input configurations. It is directly driven by a low resistance dynamic or controlled-magnetic microphone, with no other input biasing components required. The amplifier is compact enough to fit inside even the smallest commercial microphone cases; its low current drain from supplies between +4.5 and +6.0V would permit inclusion of batteries within the same case.

Figure 18 illustrates how a large number of such microphones could be directly connected to a

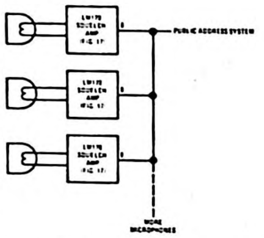


FIGURE 18. Random Access Microphone System

common bus, at their outputs, to give a random access, automatic break-in public address or paging system, which might be useful, for example, at a large conference table, or in a courtroom. While background noises at each microphone location would be suppressed, close talking would immediately allow one or more speakers to be heard. Because squelch switching levels are compatible with TTL logic, a priority logic system could be devised, which would not only give certain speakers "break-in" priority, but allow them to automatically cut off certain other speakers at the same time.

TRANSMITTER OR TAPE RECORDER VOX

In addition to squelching its own gain, the LM170 can become a voice-operated-relay control, or VOX, to switch high powered electronic or electromechanical devices. Automatic transmit-receive operation is possible in two way communication systems, or tape recorder motors may be switched on at the first syllable of infrequent speech, such as in dictation, conserving tape.

To handle large amounts of power, all that is needed is a small PNP power transistor, driving a relay, which can have multiple poles. Action is essentially the same as in squelch operation, except that the capacitor discharged by Pin 6 is charged by the relay driving circuitry. The amplifier may simultaneously be used as a continuous-running preamplifier, may be squelched along with the relay, or may even operate with an independent AGC signal, into Pin 3 or 4.

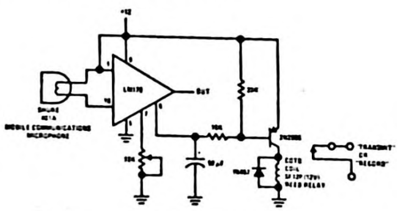


FIGURE 19. VOX Preamp

A reed relay is shown in the schematic of Figure 19, but any fast acting relay may be used. The relay coil is shunted by a diode, to protect the PNP transistor. If power supply impedance is high the circuit may tend to oscillate; bypassing the supply with a fairly large capacitor will eliminate the problem.

OSCILLATORS

Wein-Bridge Oscillator Using the LM170

The classic Wein-Bridge Oscillator is still a popular choice for many designs.

A brief review of the principle of this form of oscillator will show how ideally suited is the LM170 to this configuration.

Figure 20 shows the general configuration of the Wein-Bridge oscillator.

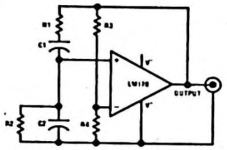


FIGURE 20. General Wein-Bridge Oscillator Configuration

The components R_1C_1 and R_2C_2 form a positive feedback network whose transfer, it can be shown, is a maximum when the lead produced by R_1C_1 and the lag afforded by R_2C_2 have the same value. At this condition the "gain" of the network's is

$$A_V = \frac{1}{(1 + R_1/R_2 + C_2/C_1)}$$

and the frequency is given by the expression:

$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

R_3 and R_4 form a negative feedback loop and control the gain of the amplifier. For sustained oscillation, the loop gain of the system must equal unity (in practice slightly greater), therefore the condition for oscillation is

$$\frac{R_3 + R_4}{R_4} = 1 + \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

or

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

Amplitude control of an oscillator assists in stabilizing its frequency as well as amplitude since it prevents the poles from wandering about on their root locus plot with gain changes and ensures starting.

Practically, one of the negative feedback resistors is often made voltage sensitive to ensure reliable starting and to control the output amplitude. If R_3 is chosen to be voltage sensitive, its characteristic has to be negative (such as a thermistor) or more usually R_4 is the control element, using, very often, a light bulb which has a positive voltage-resistance characteristic.

The simple elements such as the thermistor and light bulb rely for their action on their thermal characteristics. The response time for these devices limits their usefulness.

Alternatively the gain of the amplifier itself may be varied to afford amplitude stability.

It can now be seen how the LM170 dovetails nicely with the Wein-Bridge Oscillator configuration. It has gain, plus and minus inputs and an auxiliary control of gain via its "AGC Control inputs".

Figure 21 shows a suitable low-frequency oscillator design embodying the principles just discussed.

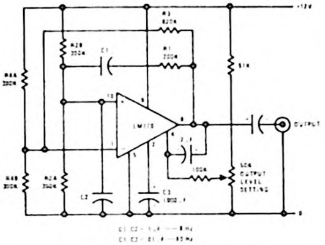


FIGURE 21. Wein-Bridge Oscillator

The positive feedback loop from Pin 8, the output, to Pin 10 uses R = 200k and C = .1 for 8 Hz. The R of the lag arm is formed from two resistors which provide bias for Pin 10, they are of course in parallel with regard to signal. The bias for Pin 1 is provided in the same manner. The 820k resistor together with the bias resistors provides a maximum loop gain of about 4, the system needs a gain of three for oscillation since the attenuation of the positive feedback loop at resonance is 3.

The resulting output is peak detected at constant Pin 4 of the device which is the base of an emitter follower biased by the external adjustable potentiometer chain, the amplitude adjustment. Detector smoothing is provided by the 1000 µF capacitor connected to Pin 2, the emitter of the detector emitter follower. The large value is dictated in this particular design by the desire to achieve regulation at about 10 Hz.

The frequency may be changed by changing only the capacitors up to a few kHz, beyond that it is desirable to reduce the bridge resistor values so that the input current offset characteristics of the LM170 do not limit the performance. Oscillators up to a few MHz may then be fabricated.

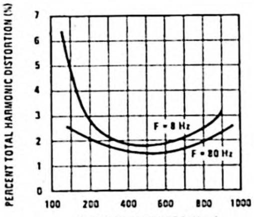


FIGURE 22. Oscillator Distortion vs Output Level

Figure 22 shows the distortion versus output amplitude of the circuit shown in Figure 3 for 8 Hz and 80 Hz versions of the oscillator.

Decade Tunable Oscillator

By using a modified twin-tee feedback network, the LM170 will produce a sine wave oscillation, tunable over one decade in frequency. The technique used is shown in Figure 23 where wideband positive feedback is applied to the non-inverting input by the capacitive divider C_1 & C_2. Capacitor C_1 also decouples the input from supply noise.

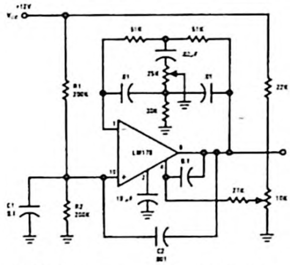


FIGURE 23. Decade Tunable Oscillator

Negative feedback occurs through the twin T at all frequencies except the null frequency of the T network, allowing the circuit to oscillate there. The nominal low frequency of oscillation for the circuit is approximately 320 Hz with the assymmetric parallel T shown. At this frequency and 1V rms out, the total harmonic distortion is under 0.25%. At the upper frequency limit, 3300 Hz the output has dropped less than 1.5 dB and the distortion is 0.45%.

A Modulated 455 kHz Signal Generator

An inexpensive, high "Q", 455 kHz ceramic filter may be substituted for the twin-tee feedback net-

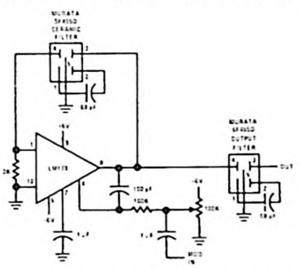


FIGURE 24. 455 kHz Modulated Constant Output Oscillator

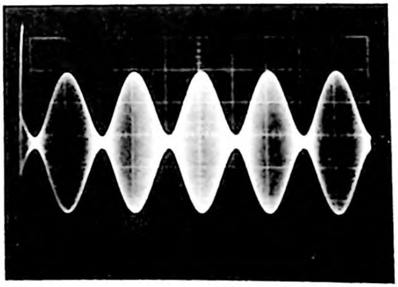


FIGURE 25. 455 kHz Modulated by 100 Hz

work of the previous example, to create a regulated-output AM IF alignment generator, Figure 24. If the AGC threshold voltage, which determines stabilized output, is varied at a low (audio) rate, the output amplitude will be forced to track the audio modulation, as in Figure 25.

The input configuration shown in Figure 19 may be used when two power supplies are available elsewhere in the system, as it allows the inputs and output of the LM170 to be referred to ground. Of course, any other suitable input biasing scheme may be used instead, for the 455 kHz signal generator.

Simultaneous Squelch & AGC Using the LM170

An interesting application of the LM170 involves simultaneously obtaining AGC and a fast attack, slow release squelch. It has been contributed by B. Chandler Shaw of Bendix Electrodynamics, North Hollywood, California.

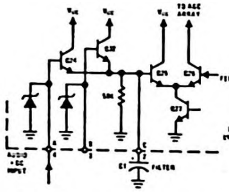


FIGURE 26. Internal AGC Control Circuitry

In normal AGC operation, a filter capacitor is required on Pin 2 to store the peak AGC control signal. The circuitry involved, shown in Figure 26, uses the emitter follower Q_{24} as a buffer and peak detector. Obviously, the voltage on the filter capacitor can be rapidly increased (lowering the gain) by the current available through the emitter follower but decreases slowly by discharging through the 50k resistor (increasing the gain). This is exactly opposite of what we require. The normal squelch circuitry, shown in Figure 27 connects one of the AGC control pins, Pin 4, to the collector of a saturating switch, Q_{21}, at Pin 6. With no signal, Q_{20} is saturated and Q_{21} is off, and Pin 6 sits at the voltage determined by the supply and resistive dividing network, or by the internal zener.

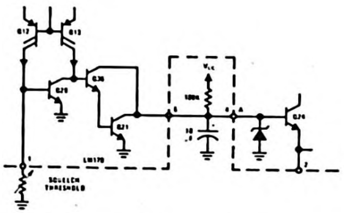


FIGURE 27. Normal Squelch Circuit

Note that no capacitor is connected to Pin 2. When the combination of peak decreasing signal currents and low enough shunt-values of Squelch Threshold control are such that the base drive for Q_{20} no longer causes saturation, Q_{36} and Q_{21} immediately turn on, rapidly discharging the capacitor at Pin 6, lowering the voltage at Pins 4 and 2, and bringing the amplifier quickly up to full gain. Upon cessation of the signal, Q_{20} saturates again turning Q_{36} and Q_{21} off, and the voltage at Pin 4 rises according to the RC time constant of the network, giving some delay, and finally a smooth turn-off of the amplifier.

If a filter capacitor were connected from Pin 2 to ground, it would not be possible to lower quickly the voltage at Pin 2 to obtain a fast attack squelch. However, if the capacitor C_1 is connected to Pin 6, as shown in Figure 28, Pin 2 is drawn down rapidly when unsquelching and the low impedance path through Q_{21} provides the ground for the filtering action required for AGC with signal and threshold level applied at Pin 3. With no signal, Q_{21} turns off and the voltage at Pin 4 rises nor-

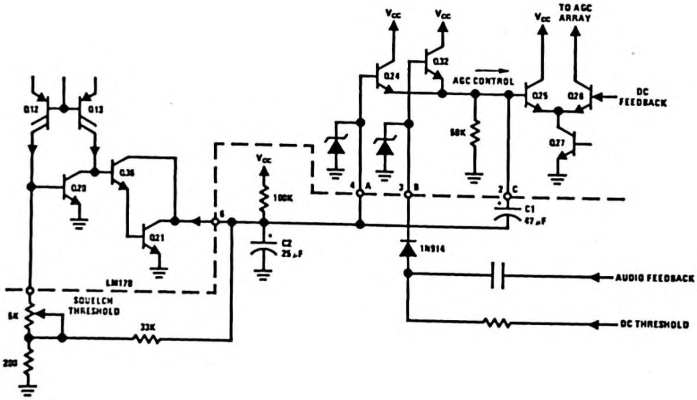


FIGURE 28. Simultaneous Squelch and AGC

mally, slowly squelching the amplifier. Note that C_1 becomes reverse biased with no signal. Since the voltage between Pin 4 and 2 is only one diode drop, this is insufficient to forward bias the capacitor and no deforming occurs. Hysteresis is provided by the positive feedback to the bottom end of the threshold control through the 33k resistor.

Temperature Compensating Techniques

The LM170 AGC control circuit is designed for a "transition width" of approximately 400 mV, to go from full gain to practically zero output swing. Due to this narrow control voltage width and to the AGC control stage being biased essentially from a three diode chain, the gain of the LM170 is subject to large variation with temperature. (See data sheet for curves of A_v vs Control Voltage at different temperatures.) With approximately a 2 mV per degree C shift per diode the three diode chain bias voltage can vary by 600 mV over a ΔT of 100°C. As a worst case, at a given control voltage of 2.4V at room temperature, the gain may vary from +40 dB at −55°C to −30 dB at +125°C. This necessitates the use of an external voltage compensation circuit that can stabilize gain variations over any temperature range from −55°C to +125°C.

Two circuits were found to be quite effective in reducing voltage gain drift. The first has less components but is less flexible, while the second is slightly more difficult to adjust but gives a wide degree of compensation over the guaranteed temperature operating range.

The first circuit is shown in Figures 29A and 29B. Figure 29A has only two diodes and is used only where a maximum shift of 4 mV/°C in AGC control voltage is required. This will be effective at gain levels only slightly below maximum. From the curves it can be seen that at lower gain levels, more than 4 mV/°C of compensation is required so the three diode chain shown in Figure 29B is used. Adjustment is simple. Once the amount of compensation needed is found from the curves and the correct circuit is chosen, potentiometer R_1 is adjusted to give the desired gain.

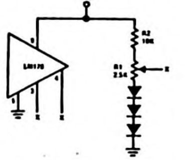


FIGURE 29A. Temperature Compensating Circuitry

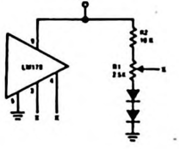


FIGURE 29B. Temperature Compensating Circuitry

If a more flexible circuit is desired, the one shown in Figure 30 can be used. Transistor T_1 biased by R_4 and $2R_4$ provides a maximum of 6 mV/°C thermal coefficient. Potentiometer R_1 shunting T_1, is adjusted to provide the amount of compensation needed. Potentiometer R_2 then sets the AGC control voltage going to Pin 3 or Pin 4 of the LM170 to give the desired gain. To adjust this circuit, the amount of thermal compensation needed is determined from the curves as before. The temperature shift over the desired operating range and the amount of gain needed are also known. Therefore, the amount of DC shift in AGC control voltage is also known by taking it straight from the A_v vs Control Voltage curves. This gives the number of mV per degree C required. Potentiometers R_1 and R_2 are then set to give proper operation. An example is shown below:

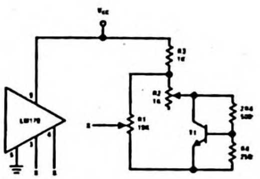


FIGURE 30. Temperature Compensating Circuitry

Gain Required	30 dB
Operating Temperature Range:	−55°C to +125°C
Change in AGC Control Voltage (from A_V vs Control Voltage Curves in data sheet)	1.9V to 2.7V = 800 mV
This means	$\frac{800\ \text{mV}}{180^\circ\text{C}}$ or 4.4 mV/°C

Potentiometer R_1 shunts T_1 thereby reducing the compensation from a maximum of 6 mV/°C. The value of R_1 was chosen to be approximately 10k ohms to prevent an unnecessary waste of current from V_{CC}.

$$\text{Let } R_1 = 10\ \text{k}\Omega$$

To set for a T.C. of 4.4 mV, set R_1 to 4.4/6.0 or 74% of its total value or 7400 ohms.

Now potentiometer R_2 is used to set the AGC control voltage to give a gain of 30 dB.

The relative displacement of the three temperature curves on the A_v vs Control voltage plot clearly shows that the relation between control voltage and temperature is not linear. Therefore, since both of the compensating techniques described above are approximately linear, some gain change with temperature is to be expected. This shift is minimized however, by either of these simple, easily adjusted, circuits so that total variations in gain less than ±3 dB over the entire operating range is possible.

Conclusion

The LM170 is an extremely versatile system component, allowing squelch and AGC in inexpensive communication systems. As a general purpose variable gain element, the device opens up many new areas of circuit design, in which closed loop gain feedback may be used to control other parameters, heretofore never considered as convenient variables. Its compatibility with ordinary monolithic logic creates possibilities in digital-communication system interfacing. The applications discussed in this report should stimulate fresh thinking, in finding new and useful services for a unique variable circuit element made possible only by monolithic technology.

APPENDIX

Squelch Release Timing

The timing capacitor from Pin 6 to ground in Figure 17 is charged by an external resistor (nominally 100 kΩ), to determine the delay between cessation of speech and turnoff of the LM170. Figures 31, 32 and 33 show timings available from 5, 10 and 25 μF capacitors. The upper trace is the input, 15 20 mV/cm. Notice that the input does not have to be completely shut off, but must only remain below the externally set squelch threshold long enough for the timing capacitor to charge to the gain control region. Both traces are shown at 200 ms per division.

The lower trace is the amplifier's output. At first, since input level is below the squelch threshold, output is zero. An abrupt increase in input level above the threshold causes almost immediate turn-on of the amplifier. When input level is decreased to its original value, amplifier output follows linearly, because gain is still at its maximum value. A delay period follows, during which the timing capacitor charges from the low voltage (less than 1V) previously forced by the squelch output, Pin 6, up to the gain control region, which begins at about +2.1V. The capacitor is still charging along an exponential RC curve while it passes through the gain control region, so that a gradual turnoff is observed, rather than the less pleasant abrupt turnoff of conventional squelch systems.

As an alternative to choosing different timing capacitor values for different release times, a single value may be used along with a potentiometer which would replace the 100k charging resistor. This would allow a front panel variable delay control, accessible by the system user.

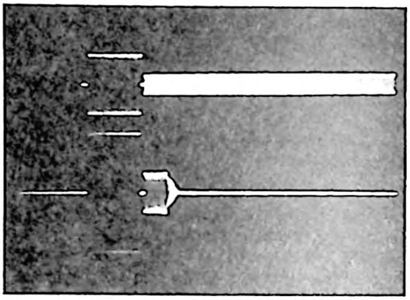


FIGURE 31. 5 μF Capacitor Timings

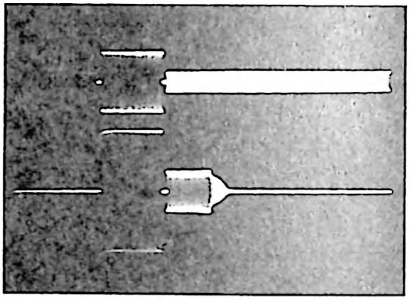


FIGURE 32. 10 μF Capacitor Timings

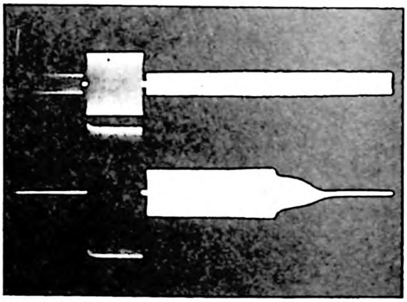


FIGURE 33. 25 μF Capacitor Timings

1.2 Volt Reference

National Semiconductor
Application Note 56
Robert C. Dobkin
December 1971

INTRODUCTION

Temperature compensated zener diodes are the most easily used voltage reference. However, the lowest voltage temperature-compensated zener is 6.2 volts. This makes it inconvenient to obtain a zero temperature-coefficient reference when the operating supply voltage is 6 volts or lower. With the availability of the LM113, this problem no longer exists.

The LM113 is a 1.2V temperature compensated shunt regulator diode. The reference is synthesized using transistors and resistors rather than a breakdown mechanism. It provides extremely tight regulation over a wide range of operating currents in addition to unusually low breakdown voltage and low temperature coefficient.

DESIGN CONCEPTS

The reference in the LM113 is developed from the highly-predictable emitter-base voltage of integrated transistors. In its simplest form, the voltage is equal to the energy-band-gap voltage of the semiconductor material. For silicon, this is 1.205V. Further, the output voltage is well determined in a production environment.

A simplified version of this reference[1] is shown in Figure 1. In this circuit, Q_1 is operated at a relatively high current density. The current density of Q_2 is about ten times lower, and the emitter-base voltage differential (ΔV_{BE}) between the two devices appears across R_3. If the transistors have high current gains, the voltage across R_2 will also be proportional to ΔV_{BE}. Q_3 is a gain stage that will regulate the output at a voltage equal to its emitter base voltage plus the drop across R_2. The emitter base voltage of Q_3 has a negative temperature coefficient while the ΔV_{BE} component across R_2 has a positive temperature coefficient. It will be shown that the ouput voltage will be temperature compensated when the sum of the two voltages is equal to the energy-band-gap voltage.

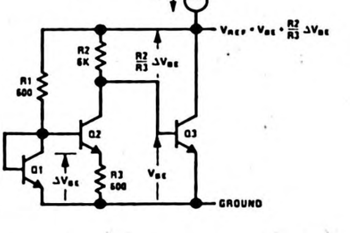

V+
I
R1
600
R2
6K
$\frac{R2}{R3}\Delta V_{BE}$
R3
600
Q1
Q2
Q3
ΔV_{BE}
V_{BE}
$V_{REF} = V_{BE} + \frac{R2}{R3}\Delta V_{BE}$
GROUND

FIGURE 1. The Low Voltage Reference in One of Its Simpler Forms.

Conditions for temperature compensation can be derived starting with the equation for the emitter-base voltage of a transistor which is[2]

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{nkT}{q}\log_e\frac{T_0}{T} + \frac{kT}{q}\log_e\frac{I_C}{I_{C0}}, \qquad (1)$$

where V_{g0} is the extrapolated energy-band-gap voltage for the semiconductor material at absolute zero, q is the charge of an electron, n is a constant which depends on how the transistor is made (approximately 1.5 for double-diffused, NPN transistors), k is Boltzmann's constant, T is absolute temperature, I_C is collector current and V_{BE0} is the emitter-base voltage at T_0 and I_{C0}.

The emitter-base voltage differential between two transistors operated at different current densities is given by

$$\Delta V_{BE} = \frac{kT}{q}\log_e\frac{J_1}{J_2} \qquad (2)$$

where J is current density.

Referring to Equation (1), the last two terms are quite small and are made even smaller by making I_C vary as absolute temperature. At any rate, they can be ignored for now because they are of the same order as errors caused by nontheoretical behavior of the transistors that must be determined empirically.

If the reference is composed of V_{BE} plus a voltage proportional to ΔV_{BE}, the output voltage is obtained by adding (1) in its simplified form to (2):

$$V_{ref} = V_{g0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{kT}{q}\log_e\frac{J_1}{J_2}. \qquad (3)$$

Differentiating with respect to temperature yields

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{g0}}{T_0} + \frac{V_{BEO}}{T_0} + \frac{k}{q}\log_e\frac{J_1}{J_2}. \qquad (4)$$

For zero temperature drift, this quantity should equal zero, giving

$$V_{g0} = V_{BEO} + \frac{kT_0}{q}\log_e\frac{J_1}{J_2}. \qquad (5)$$

The first term on the right is the initial emitter-base voltage while the second is the component proportional to emitter-base voltage differential. Hence, if the sum of the two are equal to the energy-band-gap voltage of the semiconductor, the reference will be temperature-compensated.

Figure 2 shows the actual circuit of the LM113. Q_1 and Q_2 provide the ΔV_{BE} term and Q_4 provides the V_{BE} term as in the simplified circuit. The additional transistors are used to decrease the dynamic resistance, improving the regulation of the reference against current changes. Q_3 in conjunction with current inverter, Q_5 and Q_6, provide a current source load for Q_4 to achieve high gain.

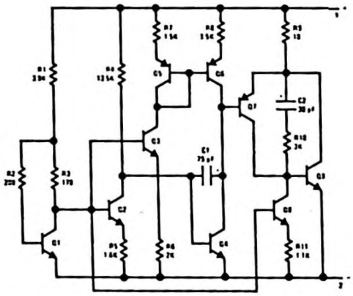


FIGURE 2. Schematic of the LM113

Q_7 and Q_9 buffer Q_4 against changes in operating current and give the reference a very low output resistance. Q_8 sets the minimum operating current of Q_7 and absorbs any leakage from Q_9. Capacitors C_1, C_2 and resistors R_9 and R_{10} frequency compensate the regulator diode.

PERFORMANCE

The most important features of the regulator diode are its good temperature stability and low dynamic resistance. Figure 3 shows the typical change in output voltage over a −55°C to +125°C temperature range. The reference voltage changes less than 0.5% with temperature, and the temperature coefficient is relatively independent of operating current.

Figure 4 shows the output voltage change with operating current. From 0.5 mA to 20 mA there is only about 6 mV of change. A good portion of the output change is due to the resistance of the aluminum bonding wires and the Kovar leads on the package. At currents below about 0.3 mA the diode no longer regulates. This is because there is insufficient current to bias the internal transistors into their active region. Figure 5 illustrates the breakdown characteristic of the diode.

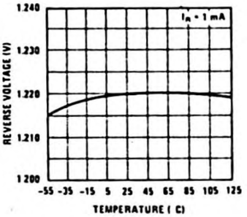


FIGURE 3. Output Voltage Change with Temperature

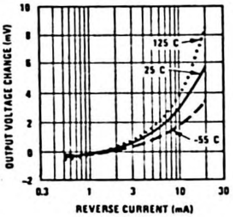


FIGURE 4. Output Voltage Change with Current

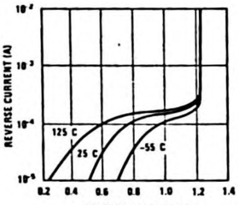


FIGURE 5. Reverse Breakdown Characteristics

APPLICATIONS

The applications for zener diodes are so numerous that no attempt to delineate them will be made. However, the low breakdown voltage and the fact that the breakdown voltage is equal to a physical property of silicon — the energy band gap voltage — makes it useful in several interesting applications.

Also the low temperature coefficient makes it useful in regulator applications — especially in battery powered systems where the input voltage is less than 6V.

Figure 6 shows a 2V voltage regulator which will operate on input voltages of only 3V. An LM113 is the voltage reference and is driven by a FET current source, Q_1. An operational amplifier compares a fraction of the output voltage with the reference. Drive is supplied to output transistor Q_2 through the V^+ power lead of the operational amplifier. Pin 6 of the op amp is connected to the LM113 rather than the output since this allows a lower minimum input voltage. The dynamic resistance of the LM113 is so low that current changes from the output of the operational amplifier do not appreciably affect regulation. Frequency compensation is accomplished with both the 50 pF and the 1 μF output capacitor.

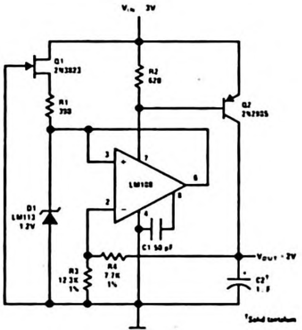


FIGURE 6. Low Voltage Regulator Circuit

It is important to use an operational amplifier with low quiescent current such as an LM108. The quiescent current flows through R_2 and tends to turn on Q_2. However, the value shown is low enough to insure that Q_2 can be turned off at worst case condition of no load and 125°C operation.

Figure 7 shows a differential amplifier with the current source biased by an LM113. Since the LM113 supplies a reference voltage equal to the energy band gap of silicon, the output current of the 2N2222 will vary as absolute temperature. This compensates the temperature sensitivity of the transconductance of the differential amplifier making the gain temperature stable. Further, the operating current is regulated against supply variations keeping the gain stable over a wide supply range.

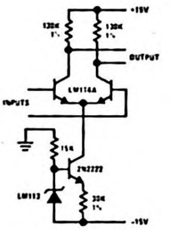
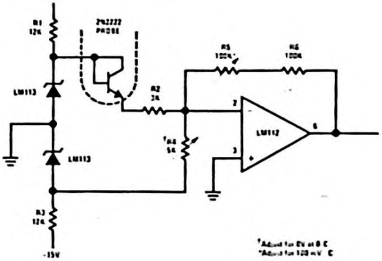


FIGURE 7. Amplifier Biasing for Constant Gain with Temperature

As shown, the gain will change less than two per cent over a −55°C to +125°C temperature range. Using the LM114A monolithic transistor and low drift metal film resistors, the amplifier will have less than 2 μV/°C voltage drift. Even lower drift may be obtained by unbalancing the collector. load resistors to null out the initial offset. Drift under nulled condition will be typically less than 0.5 μV/°C.

The differential amplifier may be used as a preamplifier for a low-cost operational amplifier such as an LM101A to improve its voltage drift characteristics. Since the gain of the operational amplifier is increased by a factor of 100, the frequency compensation capacitor must also be increased from 30 pF to 3000 pF for unity gain operation. To realize low voltage drift, case must be taken to minimize thermoelectric potentials due to temperature gradients. For example, the thermoelectric potential of some resistors may be more than 30 μV/°C, so a 1°C temperature gradient across the resistor on a circuit board will cause much larger errors than the amplifier drift alone. Wirewound resistors such as Evenohm are a good choice for low thermoelectric potential.

Figure 8 illustrates an electronic thermometer using an inexpensive silicon transistor as the temperature sensor. It can provide better than 1°C



†Adjust for 0V at 0°C
*Adjust for 100 mV/°C

FIGURE 8. Electronic Thermometer

accuracy over a 100°C range. The emitter-base turn-on voltage of silicon transistors is linear with temperature. If the operating current of the sensing transistor is made proportional to absolute temperature the nonlinearily of emitter-base voltage can be minimized. Over a −55°C to 125°C temperature range the nonlinearily is less than 2 mV or the equivalent of 1°C temperature change.

An LM113 diode regulates the input voltage to 1.2V. The 1.2V is applied through R_2 to set the operating current of the temperature-sensing transistor.

Resistor R_4 biases the output of the amplifier for zero output at 0°C. Feedback resistor R_5 is then used to calibrate the output scale factor to 100 mV/°C. Once the output is zeroed, adjusting the scale factor does not change the zero.

CONCLUSION

A new two terminal low voltage shunt regulator has been described. It is electrically equivalent to a temperature-stable 1.2V breakdown diode. Over a −55°C to 125°C temperature range and operating currents of 0.5 mA to 20 mA the LM113 has one hundred times better reverse characteristics than breakdown diodes. Additionally, wideband noise and long term stability are good since no breakdown mechanism is involved.

The low temperature coefficient and low regulation voltage make it especially suitable for a low voltage regulator or battery operated equipment. Circuit design is eased by the fact that the output voltage and temperature coefficient are largely independent of operating current. Since the reference voltage is equal to the extrapolated energy-band-gap of silicon, the device is useful in many temperature compensation and temperature measurement applications.

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1. R.J. Widlar, *"On Card Regulator for Logic Circuits,"* National Semiconductor AN-42, February, 1971.

2. J.S. Brugler, *"Silicon Transistor Biasing for Linear Collector Current Temperature Dependence,"* IEEE Journal of Solid State Circuits, pp. 57-58, June, 1967.

LM381 Low Noise Dual Preamplifier

National Semiconductor
Application Note 64
Joe E. Byerly
Ernest L. Long
May 1972

INTRODUCTION

The LM381 is a dual preamplifier expressly designed to meet the requirements of amplifying low level signals in low noise applications. Total equivalent input noise is typically 0.5 μV rms (R_S = 600Ω, 10–10, 000 Hz).

Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (112 dB), large output voltage swing (V_{CC} −2V) p–p, and wide power bandwidth (75 kHz, 20 $V_{p\text{-}p}$). The LM381 operates from a single supply across the wide range of 9 to 40V. The amplifier is internally compensated and short-circuit protected.

Attempts have been made to fill this function with selected operational amplifiers. However, due to the many special requirements of this application, these recharacterizations have not adequately met the need.

With the low output level of magnetic tape heads and phonograph cartridges, amplifier noise becomes critical in achieving an acceptable signal-to-noise ratio. This is a major deficiency of the op amp in this application. Other inadequacies of the op amp are insufficient power supply rejection, limited small-signal and power bandwidths, and excessive external components.

TABLE 1. T_A = 25°C, V_{CC} = 14V, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	Open Loop (Differential Input)		160,000		V/V
	Open Loop (Single Ended Input)		320,000		V/V
Supply Current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input Resistance					
(Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current					
(Positive Input)			0.2		μA
(Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-peak		V_{CC} −2		V
Small Signal Bandwidth			15		MHz
Power Bandwidth	20$V_{p\text{-}p}$ (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1 kHz		120		dB
Channel Separation	f = 1 kHz		60		dB
Total Harmonic Distortion	75 dB Gain, f = 1 kHz		0.1%		%
Total Equivalent Input Noise	R_S = 600Ω, 10-10, 000 Hz (Single Ended Input)		0.55		μVrms
Noise Figure	50 kΩ, 10-10, 000 Hz (Single Ended Input)		1.0		dB
	10 kΩ, 10-10, 000 Hz (Single Ended Input)		1.3		dB
	5 kΩ, 10-10, 000 Hz (Single Ended Input)		1.6		dB

CIRCUIT DESCRIPTION

To achieve low noise performance, special consideration must be taken in the design of the input stage. First, the input should be capable of being operated single ended; since both transistors contribute noise in a differential stage degrading input noise by the factor $\sqrt{2}$. Secondly, both the load and biasing elements must be resistive; since active components would each contribute as much noise as the input device.

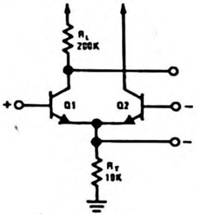


FIGURE 1. Input Stage

The basic input stage, Figure 1, can operate as a differential or single ended amplifier. For optimum noise performance Q_2 is turned OFF and feedback is brought to the emitter of Q_1.

In applications where noise is less critical, Q_1 and Q_2 can be used in the differential configuration. This has the advantage of higher impedance at the feedback summing point, allowing the use of larger resistors and smaller capacitors in the tone control and equilization networks.

The voltage gain of the single ended input stage is given by:

$$A_{V(AC)} = \frac{R_L}{re} = \frac{200k}{1.25k} = 160 \qquad (1)$$

Where:

$$re = \frac{KT}{qI_E} \approx 1.25 \times 10^3 \text{ at } 25^\circ\text{C} \quad I_E \approx 20\,\mu\text{A}$$

The voltage gain of the differential input stage is:

$$A_V = \frac{1}{2}\,\frac{R_L}{re} = \frac{1}{2}\,\frac{R_L\,qI_E}{KT} \approx 80 \qquad (2)$$

The schematic diagram of the LM381, Figure 2, is divided into separate groups by function; first and second voltage gain stages, third current gain stage, and the bias regulator.

The second stage is a common-emitter amplifier (Q_5) with a current source load (Q_6). The Darlington emitter-follower Q_3, Q_4 provides level shifting and current gain to the common-emitter stage (Q_5) and the output current sink (Q_7). The voltage gain of the second stage is approximately 2000 making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C_1. This compensates to unity gain at 15 MHz. The compensation is adequate to preserve stability to a closed loop gain of 10. Compensation for unity gain closure may be provided with the addition of an external capacitor in parallel with C_1 between Pins 5 and 6, 10 and 11.

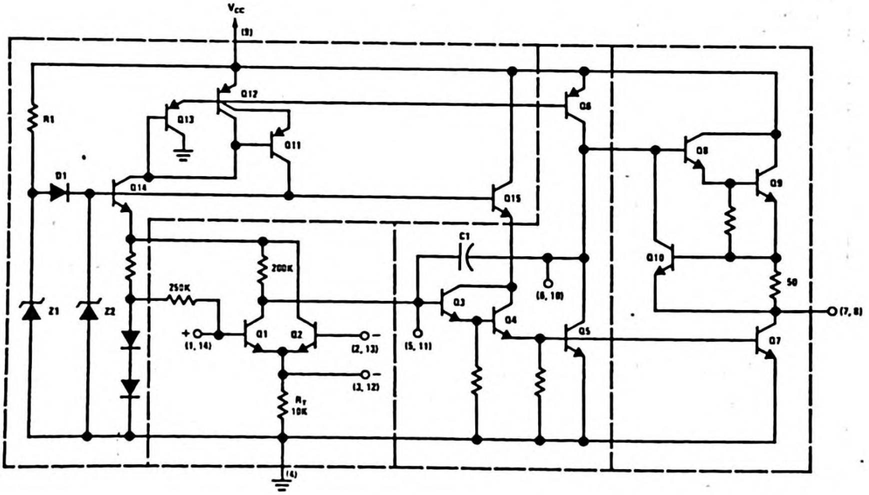


FIGURE 2. Schematic Diagram

Three basic compensation schemes are possible for this amplifier: first stage pole, second stage pole and pole-splitting. First stage compensation will cause an increase in high frequency noise because the first stage gain is reduced, allowing the second stage to contribute noise. Second stage compensation causes poor slew rate (power bandwidth) because the capacitor must swing the full output voltage. Pole-splitting overcomes both these deficiencies and has the advantage that a small monolithic compensation capacitor can be used.

The output stage is a Darlington emitter-follower (Q_8, Q_9) with an active current sink (Q_7). Transistor Q_{10} provides short-circuit protection by limiting the output to 12 mA.

The biasing reference is a zener diode (Z_2) driven from a constant current source (Q_{11}). Supply decoupling is the ratio of the current source impedance to the zener impedance. To achieve the high current source impedance necessary for 120 dB supply rejection, a cascode configuration is used (Q_{11} and Q_{12}). The reference voltage is used to power the first stages of the amplifier through emitter-followers Q_{14} and Q_{15}. Resistor R_1 and zener Z_1 provide the starting mechanism for the regulator. After starting, zero volts appears across D_1 taking it out of conduction.

Biasing

Figure 3 shows an AC equivalent circuit of the LM381. The non-inverting input, Q_1, is referenced to a voltage source two V_{BE} above ground. The output quiescent point is established by negative DC feedback through the external divider R_4/R_5 (Figure 4).

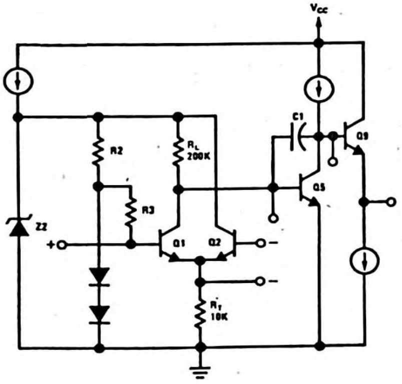


FIGURE 3. AC Equivalent Circuit

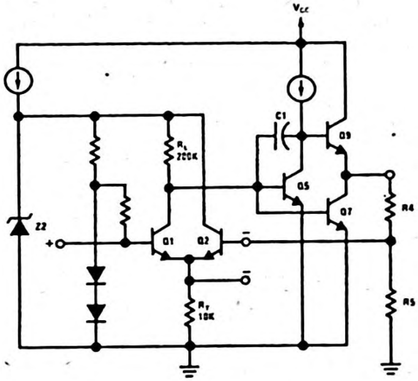


FIGURE 4. Differential Input Biasing

For bias stability, the current through R_5 is made ten times the input current of Q_2 ($\approx 0.5\ \mu A$). Then, for the differential input, resistors R_5 and R_4 are:

$$R_5 = \frac{2V_{BE}}{10\ I_{Q2}} = \frac{1.2}{5 \times 10^{-6}} = 240\ k\Omega \text{ MAXIMUM} \quad (3)$$

$$R_4 = \left(\frac{V_{CC}}{2.4} - 1\right) R_5. \quad (4)$$

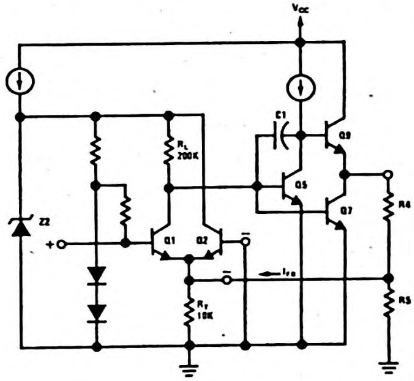


FIGURE 5. Single Ended Input Biasing

When using the single ended input, Q_2 is turned OFF and DC feedback is brought to the emitter of Q_1 (Figure 5). The impedance of the feedback summing point is now two orders of magnitude lower than the base of Q_2 ($\approx 10\ k\Omega$). Therefore, to preserve bias stability, the impedance of the feedback network must be decreased. In keeping with reasonable resistance values, the impedance of the feedback voltage source can be 1/5 the summing point impedance.

The feedback current is <100 μA worst case. Therefore, for single ended input, resistors R_5 and R_4 are:

$$R_5 = \frac{V_{BE}}{5\,I_{FB}} = \frac{0.6}{5 \times 10^{-4}} = 1200\Omega \text{ MAXIMUM} \tag{5}$$

$$R_4 = \left(\frac{V_{CC}}{1.2} - 1\right) R_5. \tag{6}$$

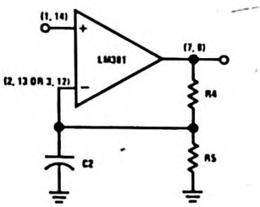


FIGURE 6. AC Open Loop

The circuits of Figures 4 and 5 have an AC and DC gain equal to the ratio R_4/R_5. To open the AC gain, capacitor C_2 is used to shunt R_5 (Figure 6). The AC gain now approaches open loop. The low frequency 3 dB corner, f_o, is given by:

$$f_o = \frac{A_o}{2\pi\, C_2 R_4} \quad \text{where: } A_o = \text{open loop gain} \tag{7}$$

Tape Playback Preamplifier

Figure 7 shows the LM381 in a flat response tape playback configuration. The mid-band gain is set by resistor ratio

$$(R_4 + R_6)/R_6 \tag{8}$$

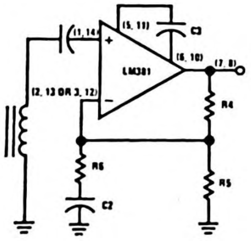


FIGURE 7. Flat Response Tape Amplifier

Capacitor C_2 sets the low frequency 3 dB corner where $X_{C2} = R_6$

$$C_2 = \frac{1}{2\pi f_o R_6} \tag{9}$$

The small-signal bandwidth of the LM381 is 15 MHz making the preamp suitable for wide-band instrumentation applications. However, in narrow-band applications it is desirable to limit the amplifier bandwidth and thus eliminate high frequency noise. Capacitor C_3 accomplishes this by shunting the internal pole-splitting capacitor (C_1), limiting the bandwidth of the amplifier. Thus, the high frequency 3 dB corner is set by C_3 according to equation 10.

$$C_3 = \frac{1}{2\pi f_3\, re\, 10^{\frac{A}{20}}} - 4 \times 10^{-12} \tag{10}$$

f_3 = high frequency 3 dB corner

re = first stage small-signal emitter resistance $\approx 2.6\ k\Omega$

A = mid-band gain in dB

For music applications, response shaping is required to provide the NAB standard tape playback equalization. Figure 8 shows the NAB equalization characteristic.

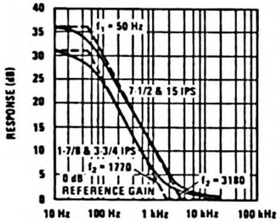


FIGURE 8. NAB Equilization Characteristic

The NAB response is achieved with the circuit of Figure 9. Resistors R_4 and R_5 set the DC bias and are chosen according to equations 3 and 4 for differential input operation and equations 5 and 6 for the single ended input. The reference gain of

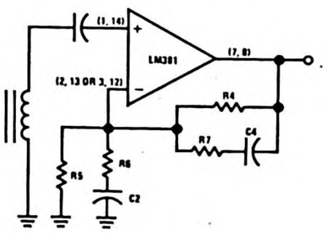


FIGURE 9. NAB Tape Preamp.

the preamp, above corner frequency f_2 (Figure 8), is set by the ratio:

$$0 \text{ dB reference gain } = \frac{R_7 + R_6}{R_6}. \quad (11)$$

The corner frequency f_2 (Figure 8) is determined where $X_{C4} = R_7$ and is given by:

$$f_2 = \frac{1}{2\pi C_4 R_7}. \quad (12)$$

Corner frequency f_1 is determined where $X_{C4} = R_4$:

$$f_1 = \frac{1}{2\pi C_4 R_4}. \quad (13)$$

The low frequency 3 dB roll-off point, f_o, is set where $X_{C2} = R_6$:

$$f_o = \frac{1}{2\pi C_2 R_6}. \quad (14)$$

Example: Design a NAB equalized preamp for a tape player requiring 0.5V rms output from a head sensitivity of 800 μV at 1 kHz, 3-3/4 IPS. The power supply voltage is 24V and the differential input configuration is used.

1. From equation (3) let $R_5 = 240 \text{ k}\Omega$.
2. Equation (4) $R_4 = \left(\frac{V_{CC}}{2.4} - 1\right) R_5$

$$R_4 = \left(\frac{24}{2.4} - 1\right) 2.4 \times 10^5$$

$$R_4 = 2.16 \times 10^5 \approx 2.2 \text{ M}\Omega$$

3. For a corner frequency, f_1 equal to 50 Hz, equation (13) is used.

$$(13) \quad C_4 = \frac{1}{2\pi f_1 R_4} = \frac{1}{6.28 \text{x} 50 \text{x} 2.2 \text{x} 10^6}$$

$$= 1.44 \text{x} 10^{-9}$$

$$C_4 \approx 1500 \text{ pF}.$$

4. From Figure 8, the corner frequency f_2 = 1770 Hz at 3-3/4 IPS. Resistor R_7 is found from equation (12).

$$(12) \quad C_4 = \frac{1}{2\pi f_2 R_7}$$

$$R_7 = \frac{1}{6.28 \text{x} 1770 \text{x} 1.5 \text{x} 10^{-9}} = 6 \text{x} 10^4$$

$$R_7 \approx 62 \text{ k}\Omega.$$

5. The required voltage gain at 1 kHz is:

$$A_V = \frac{0.5 \text{V rms}}{800\,\mu\text{V rms}} = 6.25 \text{x} 10^2 \text{ V/V} = 56 \text{ dB}.$$

6. From Figure 8 we see the reference frequency gain, above f_2, is 5 dB down from the 1 kHz value or 51 dB (355 V/V).

Equation (11)

$$0 \text{ dB Reference Gain } = \frac{R_7 + R_6}{R_6} = 355$$

$$R_6 = \frac{R_7}{355-1} = \frac{62\text{k}}{354} = 175$$

$$R_6 \approx 180\Omega.$$

7. For low frequency corner f_o = 40 Hz, equation (14)

$$C_2 = \frac{1}{2\pi\ f_o R_6} = \frac{1}{6.28 \text{x} 40 \text{x} 180} = 2.21 \text{x} 10^{-5}$$

$$C_2 \approx 20\,\mu\text{F}.$$

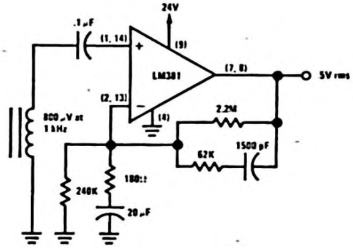


FIGURE 10. Typical Tape Playback Amplifier

This circuit is shown in Figure 10 and requires approximately 5 seconds to turn-ON for the gain and supply voltage chosen in the example. Turn-ON time can closely be approximated by:

$$t_{ON} \approx -R_4 C_2 \ln \left(1 - \frac{2.4}{V_{CC}}\right). \quad (15)$$

As seen by equation (15), increasing the supply voltage decreases turn-ON time. Decreasing the amplifier gain also decreases turn-ON time by reducing the R_4C_2 product.

Where the turn-ON time of the circuit of Figure 9 is too long, the time may be shortened by using the circuit of Figure 11. The addition of resistor R_D forms a voltage divider with R_6'. This divider is chosen so that zero DC voltage appears across

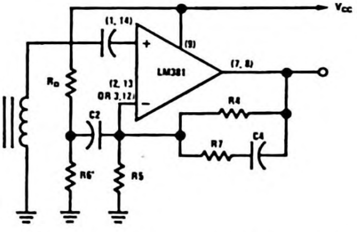


FIGURE 11. Fast Turn-On NAB Tape Preamp.

C_2. The parallel resistance of R_6' and R_D is made equal to the value of R_6 found by equation (11). In most cases the shunting effect of R_D is negligible and $R_6' \approx R_6$.

For differential input, R_D is given by:

$$R_D = \frac{(V_{CC} - 1.2)\ R_6'}{1.2}. \qquad (16)$$

For single ended input:

$$R_D = \frac{(V_{CC} - 0.6)\ R_6'}{0.6} \qquad (17)$$

In cases where power supply ripple is excessive, the circuit of Figure 11 cannot be used since the ripple is coupled into the input of the preamplifier through the divider.

The circuit of Figure 12 provides fast turn-ON while preserving the 120 dB power supply rejection.

The DC operating point is still established by R_4/R_5. However, equations (3) and (5) are modified by a factor of 10 to preserve DC bias stability.

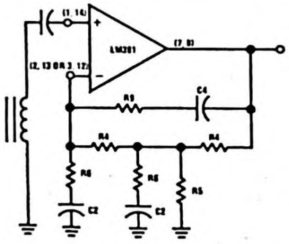


FIGURE 12. Two-Pole Fast Turn-On NAB Tape Preamp.

For differential input, equation (3) is modified as:

$$\text{(3A)}\quad R_5 = \frac{2\ V_{BE}}{100\ I_{Q2}} = \frac{1.2}{50 \times 10^{-8}}$$

$$= 24\ k\Omega \text{ MAXIMUM.}$$

For single ended input:

$$\text{Equation (5A)}\quad R_5 = \frac{V_{BE}}{50\ I_{FB}} = \frac{0.6}{50 \times 10^{-4}}$$

$$= 120\Omega \text{ MAXIMUM.}$$

Equations (11), (12) and (14) describe the high frequency gain and corner frequencies f_2 and f_o as before. Frequency f_1 now occurs where X_{C4} equals the composite impedance of the R_4, R_6, C_2 network as given by equation (18).

$$C_4 = \frac{1}{2\pi f_1 R_6 \left[\left(\frac{R_4 + R_6}{R_6}\right)^2 - 1\right]} \qquad (18)$$

The turn-ON time becomes:

$$t_{ON} \approx -2\sqrt{R_4 C_2}\ \ln\left(1 - \frac{2.4}{V_{CC}}\right). \qquad (19)$$

Example: Design an NAB equalized preamp with the fast turn-ON circuit of Figure 12 for the same requirements as the previous example.

1. From equation (3A) let $R_5 = 24\ k\Omega$.
2. Equation (4) $R_4 = \left(\frac{V_{CC}}{2.4} - 1\right) R_5$

$$= \left(\frac{24}{2.4} - 1\right) 24 \times 10^3$$

$$R_4 = 2.16 \times 10^5 \approx 220\ k\Omega.$$

3. From the previous example the reference frequency gain, above f_2, was found to be 51 dB or 355 V/V.

   Equation (11) $\frac{R_7 + R_6}{R_6} = 355.$
4. The corner frequency f_2 is 1770 Hz for 3-3/4 IPS.

   Equation (12) $C_4 = \frac{1}{2\pi f_2 R_7}$
5. The corner frequency f_1 is 50 Hz and is given by equation (18).

$$\text{(18)}\qquad C_4 = \frac{1}{2\pi f_1 R_6 \left[\left(\frac{R_4 + R_6}{R_6}\right)^2 - 1\right]}$$

6. Solving equations (11), (12), and (18) simultaneously gives:

$$R_6 = \frac{R_4\ (f_1 + \sqrt{f_1^2 + f_1 f_2\ (\text{Ref. Gain})}}{f_2\ (\text{Ref. Gain})} \qquad (20)$$

$$R_6 = \frac{2.2 \times 10^5\ (50 + \sqrt{2500 + 50 \times 1770 \times 355})}{1770 \times 355}$$

$$= 1.98 \times 10^3$$

$$R_6 \approx 2\ k\Omega.$$

7. From equation (11) $R_7 = 354\ R_6 = 708 \times 10^3$
   $R_7 \approx 680\ k\Omega.$
8. Equation (12) $C_4 = \frac{1}{2\pi f_2 R_7}$

$$= \frac{1}{6.28 \times 1770 \times 680 \times 10^3}$$

$$C_4 = 1.32 \times 10^{-10} \approx 120\ pF.$$

9. Equation (14) $C_2 = \frac{1}{2\pi f_o R_6}$

$$= \frac{1}{6.28 \times 40 \times 2 \times 10^3}$$

$$C_2 = 1.99 \times 10^{-6} \approx 2\ \mu F.$$

This circuit is shown in Figure 13 and requires only 0.1 seconds to turn-ON.

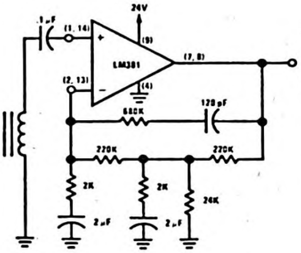


FIGURE 13

TAPE RECORD PREAMPLIFIER

When recording, the frequency response is the complement of the NAB playback equalization, making the composite record and playback response flat. Figure 14 shows the record characteristic superimposed on the NAB playback response.

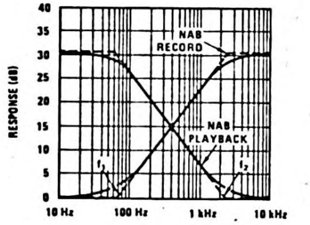


FIGURE 14. NAB Record & Playback Equilization

Curve A of Figure 15 shows the response characteristics of a typical laminated core, quarter-track head.

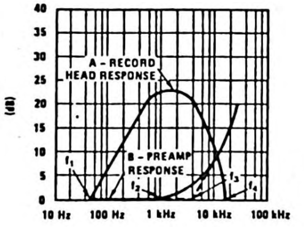


FIGURE 15. Recording Head & Preamp. Response for NAB Equilization

Curve B shows the required preamplifier response to make the composite, A + B, provide the NAB recording characteristic. This response is obtained with the circuit of Figure 16. Resistors R_4 and R_5 set the DC bias as before using equations (3) and (4) for the differential input and equations (5) and (6) for the single ended input. Resistor R_6 and capacitor C_2 set the mid-band gain as before (equations (8) and (9)). Capacitor C_5 sets the high frequency 3 dB point, f_3, (Figure 15) as:

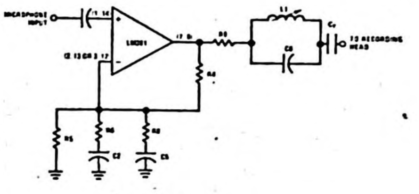


FIGURE 16. Tape Recording Preamp.

$$f_3 = \frac{1}{2\pi C_5 R_6} \tag{21}$$

The preamp gain increases at 6 dB/octave above f_3 until $R_8 = X_{C5}$.

$$R_8 = \frac{1}{2\pi f_4 C_5} \tag{22}$$

f_4 = desired high frequency cutoff

Resistor R_9 is chosen to provide the proper recording head current.

$$R_9 = \frac{V_o}{i_{\text{RECORD HEAD}}} \tag{23}$$

L_1 and C_6 form a parallel resonant bias trap to present a high impedance to the recording bias frequency and prevent intermodulation distortion.

Example: A recorder having a 24V power supply uses recording heads requiring 30 μA AC drive current. A microphone of 10 mV peak output is used. Single ended input is desired for optimum noise performance.

1. From equation (5) let $R_5 = 1200\Omega$.
2. Equation (6) $R_4 = \left(\frac{V_{CC}}{1.2} - 1\right) R_5$

   $R_4 = \left(\frac{24}{1.2} - 1\right) 1200.$

   $R_4 = 2.28 \times 10^4 \approx 22\ k\Omega.$
3. The maximum output of the LM381 is $(V_{CC} - 2V)_{p\text{-}p}$. For a 24V power supply, the maximum output is $22V_{p\text{-}p}$ or 7.8V rms. Therefore, an output swing of 6V rms is reasonable.

From equation (23) $R_9 = \dfrac{V_o}{i_{RECORD\,HEAD}}$

$$R_9 = \frac{6V}{30\,\mu A} = 200\ k\Omega.$$

4. Let the high frequency cutoff f_4 = 16 kHz (Figure 15). The recording head frequency response begins falling off at approximately 4 kHz. Therefore, the preamp gain must increase at this frequency to obtain the proper composite characteristic. The slope is 6 dB/octave for the two octaves between f_3 (4 kHz) and the cutoff frequency f_4 (16 kHz). Therefore, the mid-band gain lies 12 dB below the peak gain.

   We are allowing 6V rms output voltage swing.

   Therefore, the peak gain $= \dfrac{6V}{10\ mV} = 600$ or 55.6 dB.

   The mid-band gain = 43.6 dB or 150.

5. From equation (8) the mid-band gain =

$$\frac{R_4 + R_6}{R_6} = 150.$$

$$R_6 = \frac{R_4}{149} = \frac{22 \times 10^3}{149} = 147.7$$

$$R_6 \approx 150\Omega$$

6. Equation (9) $C_2 = \dfrac{1}{2\pi f_o R_6}$

$$= \frac{1}{6.28 \times 50 \times 150}$$

$$= 2.12 \times 10^{-5}$$

$$C_2 \approx 20\,\mu F.$$

7. Equation (21) $C_5 = \dfrac{1}{2\pi f_3 R_6}$

$$= \frac{1}{6.28 \times 4 \times 10^3 \times 150}$$

$$= 2.66 \times 10^{-7}$$

$$C_5 \approx 0.27\,\mu F.$$

8. Equation (22) $R_8 = \dfrac{1}{2\pi f_4 C_5}$

$$= \frac{1}{6.28 \times 16 \times 10^3 \times 2.7 \times 10^{-7}}$$

$$= 36.8$$

$$R_8 \approx 33\Omega.$$

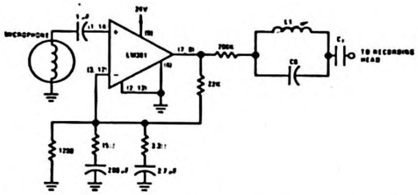


FIGURE 17. Typical Tape Recording Amplifier

PHONO PREAMPLIFIER

Crystal and ceramic phono cartridges provide output levels of 100 mV to 2V and therefore do not require preamplification. Magnetic cartridges, however, provide much lower outputs as shown in Table 2.

TABLE 2.

MANUFACTURER	MODEL	OUTPUT AT 5 cm/sec
Empire Scientific	999 888	5 mV 8 mV
Shure	V-15 M91	3.5 mV 5 mV
Pickering	V-15 AT3	5 mV

Output voltage is specified for a given modulation velocity. The magnetic pickup is a velocity device, therefore, output is proportional to velocity. For example, a cartridge producing 5 mV at 5 cm/sec will produce 1 mV at 1 cm/sec and is specified as having a sensitivity of 1 mV/cm/sec.

In order to transform cartridge sensitivity into useful preamp design information, we need to know typical and maximum modulation velocity limits of stereo records.

The RIAA recording characteristic establishes a maximum recording velocity of 25 centimeters per second in the range of 800 to 2500 Hz. Typically, good quality records are recorded at a velocity of 3 to 5 cm/sec.

Figure 18 shows the RIAA playback equalization. This response is obtained with the circuit of Figure 19.

Resistors R_4 and R_5 set the DC bias (equations (3) and (4), or (5) and (6)). The 0 dB reference gain is set by the ratio:

$$0\ \text{dB Ref Gain} = \frac{R_{10} + R_6}{R_6}. \qquad (24)$$

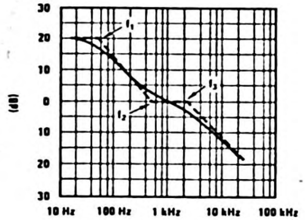


FIGURE 18. RIAA Playback Equilization

The corner frequency, f_1, (Figure 18) is established where $X_{C7} = R_4$ or:

$$C_7 = \frac{1}{2\pi f_1 R_4}. \tag{25}$$

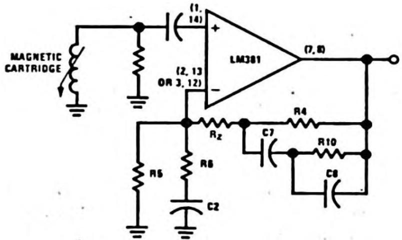


FIGURE 19. RIAA Phono Preamp.

Likewise, frequency, f_2 occurs where $X_{C7} = R_{10}$ or:

$$C_7 = \frac{1}{2\pi f_2 R_{10}}. \tag{26}$$

The third corner frequency, f_3, is determined where $X_{C8} = R_{10}$:

$$C_8 = \frac{1}{2\pi f_3 R_{10}}. \tag{27}$$

Resistor R_Z is used to insert a zero in the feedback loop since the LM381 is not compensated for unity gain. Either R_Z is required to provide a zero at or above a gain of 20 dB ($R_Z = 10\ R_6$), or external compensation is provided for unity gain stability according to equation (10).

Example: Design a phonograph preamp operating from a 30 volt supply, with a cartridge of 0.5 mV/cm/sec sensitivity, to drive a power amplifier of 5V rms input overload limit.

1. From equation (3) let $R_5 = 100\ k\Omega$.

2. Equation (4) $R_4 = \left(\frac{V_{CC}}{2.4} - 1\right) R_5$

$$= \left(\frac{30}{2.4} - 1\right) 10^5$$

$$R_4 = 11.5 \times 10^5 \approx 1.2\ M\Omega.$$

3. Equation (25) $C_7 = \frac{1}{2\pi f_1 R_4}$

$$= \frac{1}{6.28 \times 50 \times 1.2 \times 10^6}$$

$$= 2.65 \times 10^{-9}$$

$$C_7 \approx .003\ \mu F.$$

4. Equation (26) $C_7 = \frac{1}{2\pi f_2 R_{10}}$;

$$R_{10} = \frac{1}{6.28 \times 500 \times 3 \times 10^{-9}}$$

$$= 1.03 \times 10^5$$

$$R_{10} \approx 100\ k\Omega.$$

5. The maximum cartridge output at 25cm/sec is: (.5 mV/cm/sec) x (25 cm/sec) = 12.5 mV. The required mid-band gain is therefore:

$$\frac{5V\ rms}{12.5\ mV\ rms} = 400.$$

6. Equation (24)

$$0\ dB\ Ref.\ Gain = \frac{R_{10} + R_6}{R_6} = 400;$$

$$R_6 = \frac{100k}{399} = 251 \approx 240\Omega$$

$$R_Z = 10\ R_6 = 2400\Omega.$$

7. Equation (9)

$$C_2 = \frac{1}{2\pi f_o R_6} = \frac{1}{6.28 \times 40 \times 240} = 1.7 \times 10^{-5}$$

$$C_2 \approx 20\ \mu F.$$

8. Equation (27)

$$C_8 = \frac{1}{2\pi f_3 R_{10}} = \frac{1}{6.28 \times 2200 \times 6.8 \times 10^4}$$

$$= 7.23 \times 10^{-10}$$

$$C_8 \approx 0.001\ \mu F.$$

The completed design is shown in Figure 20 where a 47 kΩ input resistor has been included to provide the RIAA standard cartridge load.

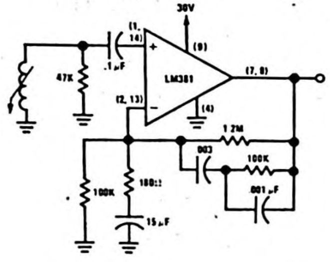


FIGURE 20. Typical Magnetic Phono Preamp.

TONE CONTROLS

Most tape and phonograph applications require bass and treble tone controls. Due to the insertion loss of the tone control, (equal to the available boost), it has been normal to use two preamplifiers with the control placed between them. However, due to the excellent gain and large output capability of the LM381, only a single preamp is required.

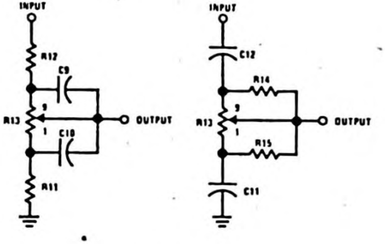


FIGURE 21. Bass & Treble Controls

Figure 21 shows the bass and treble tone controls. The potentiometers, R_{13}, are audio taper; i.e., at the center of shaft rotation the wiper is at the 90%—10% point of the total resistance. Both controls are simple AC dividers, with the flat response position where the signal is attenuated from the "full boost".

In the bass control the ratio of resistors R_{11}/R_{12} and R_{12}/R_{13} determine the degree of "boost" and "cut". For example, if 20 dB of "boost" and "cut" is desired, the ratio R_{11}/R_{12} and R_{12}/R_{13} is 20 dB or 10:1. The low frequency control point, f_1, (Figure 22) is set where $X_{C9} = R_{12}$ and $X_{C10} = R_{11}$.

$$C_9 = \frac{1}{2\pi f_1 R_{12}}, \tag{28}$$

$$C_{10} = \frac{1}{2\pi f_1 R_{11}}. \tag{29}$$

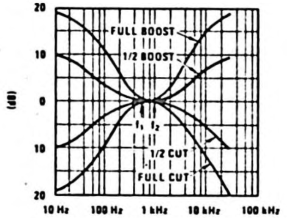


FIGURE 22. Bass & Treble Tone Control Response for 20 dB Boost & Attenuation

The treble control is the analogue of the bass control with the resistor and capacitor dividers reversed. The ratio of reactance of C_{11}/C_{12} is set equal to the amount of "boost" and "cut". The high frequency control point, f_2, is established where $X_{C12} = R_{13}$.

$$C_{12} = \frac{1}{2\pi f_2 R_{13}}. \tag{30}$$

$$R_{14} = \frac{1}{2\pi f_2 C_{12}}. \tag{31}$$

$$R_{15} = \frac{1}{2\pi f_2 C_{11}}. \tag{32}$$

Figure 23 shows one channel of a practical preamplifier for a stereo phonograph. The preamp is complete with RIAA equalization, bass and treble tone control, balance control and volume control.

AUDIO MIXER

In many audio applications it is desirable to provide a mixer to combined or select several inputs. Such applications include public address systems where more than one microphone is used; tape recorders, high fidelity phonographs, guitar amplifiers, etc.

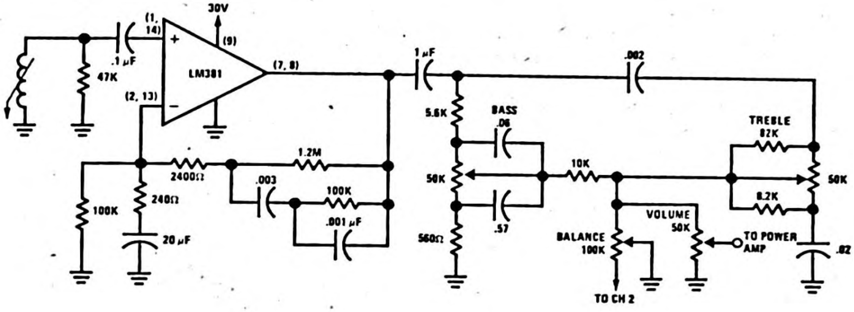

30V
(1, 14)
(9)
+
−
LM381
(7, 8)
(2, 13)
.1 μF
47K
100K
240Ω
2400Ω
20 μF
1.2M
.003
100K
.001 μF
1 μF
.002
5.6K
BASS
.06
50K
.57
560Ω
10K
BALANCE
100K
TO CH 2
VOLUME
50K
TO POWER
AMP
TREBLE
82K
8.2K
50K
.02

FIGURE 23. Single Channel of Complete Phono Preamp.

Figure 24 shows the LM381 in a mixer configuration. Inputs at A, B, C, −N can be selected and combined (summed) with potentiometers R_A, R_B, R_C, $-R_N$. Resistors R_4 and R_5 establish the DC quiescent point in accordance with equations (3A) and (4). (Only the differential input configuration is used in the mixer application since the high source impedance of the input potentiometers would negate any advantage of the single ended input.) Input bias current is supplied through resistor R_F. Therefore, an upper limit of R_F should be established to avoid output offset voltage problems. A safe upper limit is to let:

$$R_F = R_4 \text{ MAXIMUM} \qquad (33)$$

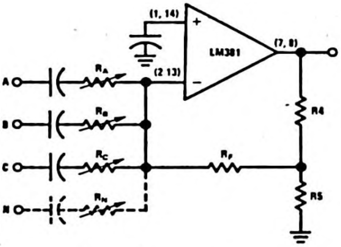

(1, 14)
+
−
LM381
(7, 8)
(2 13)
A
B
C
N
R_A
R_B
R_C
R_N
R_F
R4
R5

FIGURE 24. Audio Mixer

The voltage gain of the mixer is:

$$|A_{V_{A,B,C}}| = \frac{R_4R_F + R_4R_5 + R_5R_F}{R_5\,(R_{A,B,C} + R_{S_{A,B,C}})} \qquad (34)$$

Where the values of R_F and the source impedance, R_S, are such that the gain of the circuit of Figure 24 is inadequate, the configuration of Figure 25 may be used.

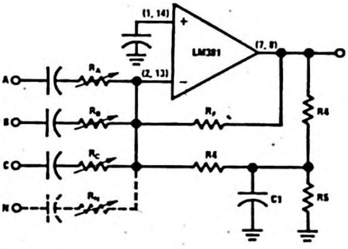

(1, 14)
+
−
LM381
(7, 8)
(2, 13)
A
B
C
N
R_A
R_B
R_C
R_N
R_F
R4
C1
R4
R5

FIGURE 25.

The voltage gain of the mixer is now:

$$|A_V| = \frac{R_F}{R_{A,B,C} + R_{S_{A,B,C}}} \qquad (35)$$

Since resistor R_F is no longer required to supply the input bias current, it does not have the upper limit as in the previous circuit. Therefore, the open loop gain of the LM381 can be realized. Capacitor C_1, shunts the AC feedback of the $R_4 - R_5$ network and is found by:

$$C_1 = \frac{10^{\frac{A_o}{20}}}{2\pi f_o R_4}$$

A_o = amplifier open loop gain in dB

f_o = low frequency 3 dB corner

Example: Design a microphone mixer for use with 600Ω dynamic microphones with an output level of 10 mV. The mixer should operate from a 24V supply and deliver 5 volts output. A dynamic range of 80 dB is desired.

1. From equation (3A) $R_5 = 24\ k\Omega$

2. Equation (4)

$$R_4 = \left(\frac{V_{CC}}{2.4} - 1\right) R_5$$

$$R_4 = \left(\frac{24}{2.4} - 1\right) 24 \times 10^3$$

$$R_4 = 2.16 \times 10^5 \approx 220\ k\Omega$$

3. For 5V output:

$$\text{Gain} = \frac{5V}{10\ mV} = 500$$

4. For 80 dB dynamic range:

$$\text{Attenuation} = \frac{500}{80\ dB} = 5 \times 10^{-2}$$

5. Equation (34)

$$|A_V| = \frac{R_4R_F + R_4R_5 + R_5R_F}{R_5(R_{A,B,C} + R_S)}$$

$$R_F = \frac{|A_V|\, R_5(R_{A,B,C} + R_S) - R_4R_5}{R_4 + R_5}$$

At maximum volume: $R_{A,B,C,} = 0$, Gain = 500

$$R_F = \frac{500 \times 2.4 \times 10^4\ (0 + 600) - (2.2 \times 10^5)(2.4 \times 10^4)}{2.2 \times 10^5 + 2.4 \times 10^4}$$

$$R_F = 7.87k \approx 8.2k$$

At maximum attenuation:

$$R_{A,B,C} = \frac{R_4R_F + R_4R_5 + R_5R_F - |A_V|R_5R_S}{A_V R_5}$$

$$R_{A,B,C} = 5.99 \times 10^6 \approx 5M\Omega$$

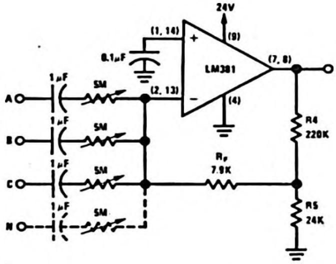


FIGURE 26.

CONCLUSION:

The applications presented in this note are by no means exhaustive. The LM381 is a widely versatile low noise, high gain, wide band gain block and, as such has many applications outside the audio spectrum.

AN-69 LM380 Power Audio Amplifier

LM380 Power Audio Amplifier

National Semiconductor
Application Note 69
Joe E. Byerly
Marvin K. Vander Kooi
December 1972

INTRODUCTION

The LM380 is a power audio amplifier intended for consumer applications. It features an internally fixed gain of 50 (34 dB) and an output which automatically centers itself at one-half of the supply voltage. A unique input stage allows inputs to be ground referenced or AC coupled as required. The output stage of the LM380 is protected with both short circuit current limiting and thermal shutdown circuitry. All of these internally provided features result in a minimum external parts count integrated circuit for audio applications.

This paper describes the circuit operation of the LM380, its power handling capability, methods of volume and tone control, distortion, and various application circuits such as a bridge amplifier, a power supply splitter, and a high input impedance audio amplifier.

CIRCUIT DESCRIPTION

Figure 1 shows a simplified circuit schematic of the LM380. The input stage is a PNP emitter-follower driving a PNP differential pair with a slave current-source load. The PNP input is chosen to reference the input to ground, thus enabling the input transducer to be directly coupled.

The output is biased to half the supply voltage by resistor ratio R_1/R_2. Negative DC feedback, through resistor R_2, balances the differential stage with the output at half supply, since $R_1 = 2\,R_2$ (Figure 1).

The second stage is a common emitter voltage gain amplifier with a current-source load. Internal compensation is provided by the pole-splitting capacitor C'. Pole-splitting compensation is used to preserve wide power bandwidth (100 kHz at 2W, 8Ω). The output is a quasi-complementary pair emitter-follower.

The amplifier gain is internally fixed to 34 dB or 50. This is accomplished by the internal feedback network R_2–R_3. The gain is twice that of the ratio R_2/R_3 due to the slave current-source which provides the full differential gain of the input stage.

TABLE 1. Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Output (rms)	8Ω load, 3% T.H.D. (Notes 3, 4)	2.5			Wrms
Gain		40	50	60	V/V
Output Voltage Swing	8Ω load		14		$V_{p\text{-}p}$
Input Resistance			150k		Ω
Total Harmonic Distortion	P_o = 1W, (Notes 4 & 5)		0.2		%
Power Supply Rejection	C_{bypass} = 5 μF, f = 120 Hz (Note 2)		38		dB
Supply Voltage Range		8		22	V
Bandwidth	P_O = 2W, R_L = 8Ω		100k		Hz
Quiescent Output Voltage		8	9	10	V
Quiescent Supply Current			7	25	mA
Short Circuit Current			1.3		A

Note 1: V_S = 18V; T_A = 25°C unless otherwise specified.

Note 2: Rejection ratio referred to output.

Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of six square inches.

Note 4: If oscillation exists under some load conditions, add a 2.7Ω resistor and 0.1 μF series network from Pin 8 to ground.

Note 5: C_{bypass} = 0.47 μF on Pin 1.

Note 6: Pins 3, 4, 5, 10, 11, 12 at 50°C derates 25°C/W above 50°C case.

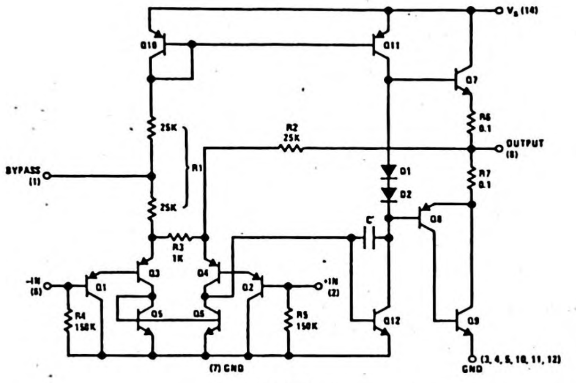


FIGURE 1.

GENERAL OPERATING CHARACTERISTICS

The output current of the LM380 is rated at 1.3A peak. The 14 pin dual-in-line package is rated at 35°C/W when soldered into a printed circuit board with 6 square inches of 2 ounce copper foil (Figure 2). Since the device junction temperature is limited to 150°C via the thermal shutdown circuitry, the package will support 3 watts dissipation at 50°C ambient or 3.7 watts at 25°C ambient.

Figure 2 shows the maximum package dissipation versus ambient temperature for various amounts of heat sinking.

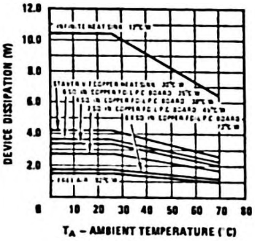


FIGURE 2. Device Dissipation vs Ambient Temperature

Figures 3A, B, and C show device dissipation versus output power for various supply voltages and loads.

The maximum device dissipation is obtained from Figure 2 for the heat sink and ambient temperature conditions under which the device will be operating. With this maximum allowed dissipation, Figures 3A, B and C show the maximum power supply allowed (to stay within dissipation limits) and the output power delivered into 4, 8 or 16 ohm loads. The three percent total-harmonic-distortion line is approximately the on-set of clipping.

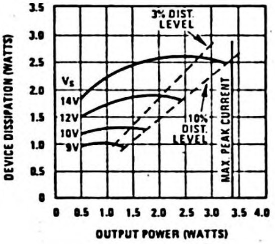


FIGURE 3A. Device Dissipation vs Output Power — 4Ω Load

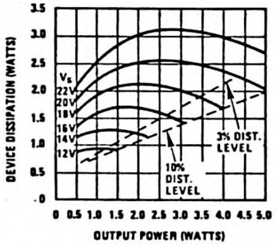


FIGURE 3B. Device Dissipation vs Output Power — 8Ω Load

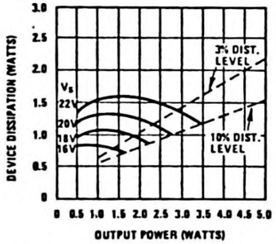


FIGURE 3C. Device Dissipation vs Output Power — 16Ω Load

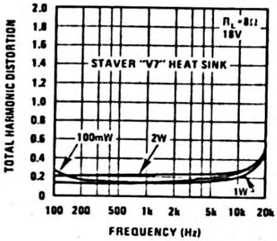


FIGURE 4. Total Harmonic Distortion vs Frequency

Figure 4 shows total harmonic distortion versus frequency for various output levels, while Figure 5 shows the power bandwidth of the LM380.

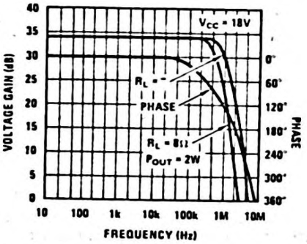


FIGURE 5. Output Voltage Gain vs Frequency

Power supply decoupling is achieved through the AC divider formed by R_1 (Figure 1) and an external bypass capacitor. Resistor R_1 is split into two 25 kΩ halves providing a high source impedance for the integrator. Figure 6 shows supply decoupling versus frequency for various bypass capacitors.

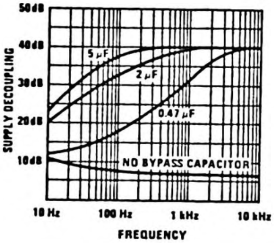


FIGURE 6. Supply Decoupling vs Frequency

BIASING

The simplified schematic of Figure 1 shows that the LM380 is internally biased with the 150 kΩ resistance to ground. This enables input transducers which are referenced to ground to be direct-coupled to either the inverting or non-inverting inputs of the amplifier. The unused input may be either: 1) left floating, 2) returned to ground through a resistor or capacitor or 3) shorted to ground. In most applications where the non-inverting input is used, the inverting input is left floating. When the inverting input is used and the non-inverting input is left floating, the amplifier may be found to be sensitive to board layout since stray coupling to the floating input is positive feedback. This can be avoided by employing one of three alternatives: 1) AC grounding the unused input with a small capacitor. This is preferred when using high source impedance transducers. 2) Returning the unused input to ground through a resistor. This is preferred when using moderate to low DC source impedance transducers and when output offset from half supply voltage is critical. The resistor is made equal to the resistance of the input transducer, thus maintaining balance in the input differential amplifier and minimizing output offset. 3) Shorting the unused input to ground. This is used with low DC source impedance transducers or when output offset voltage is non-critical.

OSCILLATION

The normal power supply decoupling precautions should be taken when installing the LM380. If V_S is more than 2" to 3" from the power supply filter capacitor it should be decoupled with a 0.1μF disc ceramic capacitor at the V_S terminal of the IC.

The R_C and C_C shown as dotted line components on Figure 7 and throughout this paper suppresses a 5 to 10 MHz small amplitude oscillation which can occur during the negative swing into a load which draws high current. The oscillation is of course at too high of a frequency to pass through a speaker, but it should be guarded against when operating in an RF sensitive environment.

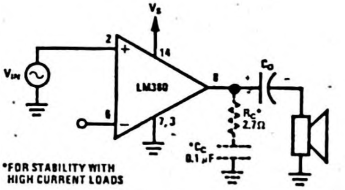
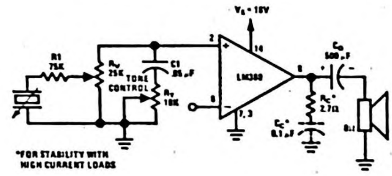


FIGURE 7. Minimum Component Configuration

APPLICATIONS

With the internal baising and compensation of the LM380, the simplest and most basic circuit configuration requires only an output coupling capacitor as seen in Figure 7.

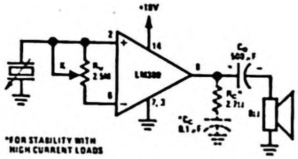
An application of this basic configuration is the phonograph amplifier where the addition of volume and tone controls is required. Figure 8 shows the LM380 with a voltage divider volume control and high frequency roll-off tone control.



V_S = 18V
R1
75K
R_V
25K
TONE
CONTROL
C1
.05 μF
R_T
10K
2
14
LM380
6
7, 3
8
C_O
500 μF
R_C*
2.7Ω
C_C*
0.1 μF
8Ω
*FOR STABILITY WITH
HIGH CURRENT LOADS

FIGURE 8. Phono Amp

When maximum input impedance is required or the signal attenuation of the voltage divider volume control is undesirable, a "common mode" volume control may be used as seen in Figure 9.

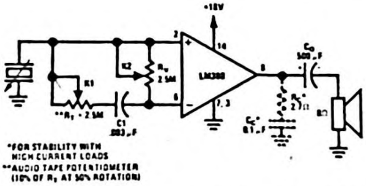


+18V
2
14
K
R_V
2.5M
LM380
6
7, 3
8
C_O
500 μF
R_C*
2.7Ω
*C_C
0.1 μF
8Ω
*FOR STABILITY WITH
HIGH CURRENT LOADS

FIGURE 9. "Common Mode" Volume Control

With this volume control the source loading impedance is only the input impedance of the amplifier when in the full-volume position. This reduces to one-half the amplifier input impedance at the zero volume position. Equation 1 describes the output voltage as a function of the potentiometer setting.

$$V_{OUT} = 50\,V_{IN}\left(1 - \frac{150 \times 10^3}{k_1 R_V + 150 \times 10^3}\right)_{0 \leq k_1 \leq 1} \quad (1)$$



+18V
2
14
K2
R_V
2.5M
K1
**R_T = 2.5M
C1
.003 μF
LM380
6
7, 3
8
C_O
500 μF
R_C*
2.7Ω
C_C*
0.1 μF
8Ω
*FOR STABILITY WITH
HIGH CURRENT LOADS
**AUDIO TAPE POTENTIOMETER
(10% OF R_T AT 50% ROTATION)

FIGURE 10. "Common Mode" Volume and Tone Control

This "common mode" volume control can be combined with a "common mode" tone control as seen in Figure 10.

This circuit has a distinct advantage over the circuit of Figure 7 when transducers of high source impedance are used, in that, the full input impedance of the amplifier is realized. It also has an advantage with transducers of low source impedance since the signal attenuation of the input voltage divider is eliminated. The transfer function of the circuit of Figure 10 is given by:

$$\frac{V_{OUT}}{V_{IN}} = 50\left(1 - \frac{150k}{150k + \dfrac{k_1 R_T k_2 R_V + \dfrac{k_2 R_V}{j2\pi f c_1}}{k_1 R_T + k_2 R_V + \dfrac{1}{j2\pi f c_1}}}\right)_{\substack{0 \leq k_1 \leq 1 \\ 0 \leq k_2 \leq 1}} \quad (2)$$

Figure 11 shows the response of the circuit of Figure 10.

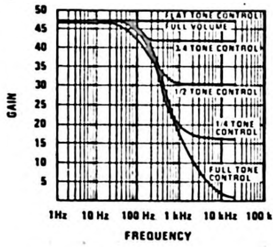


FIGURE 11. Tone Control Response

Most phonograph applications require frequency response shaping to provide the RIAA equalization characteristic. When recording, the low frequencies are attenuated to prevent large undulations from destroying the record groove walls. (Bass tones have higher energy content than high frequency tones.) Conversely, the high frequencies are emphasized to achieve greater signal-to-noise ratio. Therefore, when played back the phono amplifier should have the inverse frequency response as shown in Figure 12.

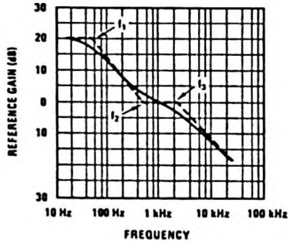
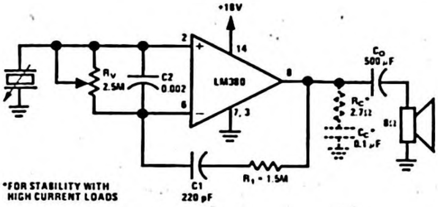


FIGURE 12. RIA Playback Equalization

This response is achieved with the circuit of Figure 13.

The mid-band gain, between frequencies f_2 and f_3, Figure 12, is established by the ratio of R_1 to the input resistance of the amplifier (150 kΩ).

$$\text{Mid-band Gain} = \frac{R_1 + 150\ \text{k}\Omega}{150\ \text{k}\Omega} \qquad (3)$$



*FOR STABILITY WITH HIGH CURRENT LOADS

FIGURE 13. RIAA Phono Amplifier

Capacitor C_1 sets the corner frequency f_2 where $R_1 = X_{C1}$.

$$C_1 = \frac{1}{2\pi f_2 R_1} \qquad (4)$$

Capacitor C_2 establishes the corner frequency f_3 where X_{C2} equals the impedance of the inverting input. This is normally 150 kΩ. However, in the circuit of Figure 13 negative feedback reduces the impedance at the inverting input as:

$$Z = \frac{Z_o}{1 + A_o\beta} \qquad (5)$$

Where:

Z_o = impedance at node 6 without external feedback (150 kΩ)

A_o = gain without external feedback (50)

β = feedback transfer function $\beta = \dfrac{A_o - A}{A_o A}$

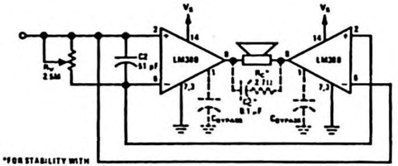
A = closed loop gain with external feedback.

Therefore:

$$C_2 = \frac{1}{2\pi f_3 \left(\dfrac{Z_o}{1 + A_o\beta}\right)} = \frac{1}{2\pi f_3 \left(\dfrac{150\text{k}}{1 + 50\beta}\right)} \qquad (6)$$

BRIDGE AMPLIFIER

Where more power is desired than can be provided with one amplifier, two amps may be used in the bridge configuration shown in Figure 14.



*FOR STABILITY WITH HIGH CURRENT LOADS

FIGURE 14. Bridge Configuration

This provides twice the voltage swing across the load for a given supply, thereby, increasing the power capability by a factor of four over the single amplifier. However, in most cases the package dissipation will be the first parameter limiting power delivered to the load. When this is the case, the power capability of the bridge will be only twice that of the single amplifier. Figures 15A and B show output power versus device package dissipation for both 8 and 16Ω loads in the bridge configuration. The 3% and 10% harmonic distortion contours double back due to the thermal limiting of the LM380. Different amounts of heat sinking will change the point at which the distortion contours bend.

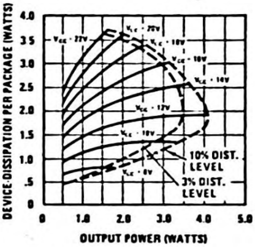


FIGURE 15A. 8Ω Load

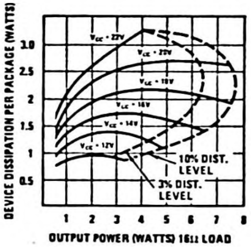
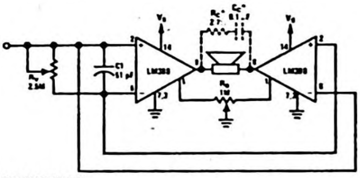


FIGURE 15B. 16Ω Load

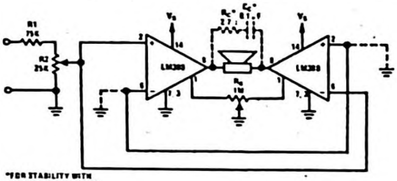
The quiescent output voltage of the LM380 is specified at 9 ± 1 volts with an 18 volt supply. Therefore, under the worst case condition, it is possible to have two volts DC across the load. With an 8Ω speaker this is 0.25A which may be excessive. Three alternatives are available; 1) care can be taken to match the quiescent voltages, 2) a non-polar capacitor may be placed in series with the load, 3) the offset balance control of Figure 16 may be used.



*FOR STABILITY WITH HIGH CURRENT LOADS

FIGURE 16. Quiescent Balance Control

The circuits of Figures 14 and 16 employ the "common mode" volume control as shown before. However, any of the various input connection schemes discussed previously may be used. Figure 17 shows the bridge configuration with the voltage divider input. As discussed in the "Biasing" section the undriven input may be AC or DC grounded. If V_S is an appreciable distance from the power supply (>3") filter capacitor it should be decoupled with a 1µF tantaulum capacitor.

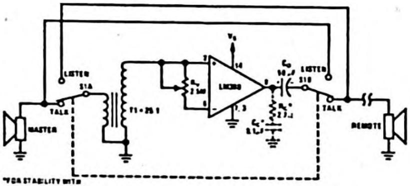


*FOR STABILITY WITH HIGH CURRENT LOADS

FIGURE 17. Voltage Divider Input

INTERCOM

The circuit of Figure 18 provides a minimum component intercom. With switch S_1 in the talk position, the speaker of the master station acts as the microphone with the aid of step-up transformer T_1.



*FOR STABILITY WITH HIGH CURRENT LOADS

FIGURE 18. Intercom

A turns ratio of 25 and a device gain of 50 allows a maximum loop gain of 1250. R_V provides a "common mode" volume control. Switching S_1 to the listen position reverses the role of the master and remote speakers.

LOW COST DUAL SUPPLY

The circuit shown in Figure 19 demonstrates a minimum parts count method of symmetrically splitting a supply voltage. Unlike the normal R, C, and power zener diode technique the LM380 circuit does not require a high standby current and power dissipation to maintain regulation.

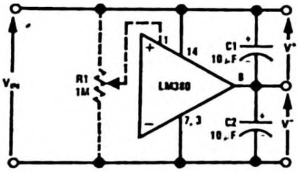


FIGURE 19. Dual Supply

With a 20 volt input voltage (±10 volt output) the circuit exhibits a change in output voltage of approximately 2% per 100 mA of unbalanced load change. Any balanced load change will reflect only the regulation of the source voltage V_{IN}.

The theoretical plus and minus output tracking ability is 100% since the device will provide an output voltage at one-half of the instantaneous supply voltage in the absence of a capacitor on the bypass terminal. The actual error in tracking will be directly proportional to the unbalance in the quiescent output voltage. An optional potentiometer may be placed at pin 1 as shown in Figure 19 to null output offset. The unbalanced current output for the circuit of Figure 18 is limited by the power dissipation of the package.

In the case of sustained unbalanced excess loads, the device will go into thermal limiting as the temperature sensing circuit begins to function. For instantaneous high current loads or short circuits the device limits the output current to approximately 1.3 amperes until thermal shut-down takes over or until the fault is removed.

HIGH INPUT IMPEDANCE CIRCUIT

The junction FET isolation circuit shown in Figure 20 raises the input impedance to 22 MΩ for low frequency input signals. The gate to drain capacitance (2 pF maximum for the KE4221 shown) of the FET limits the input impedance as frequency increases.

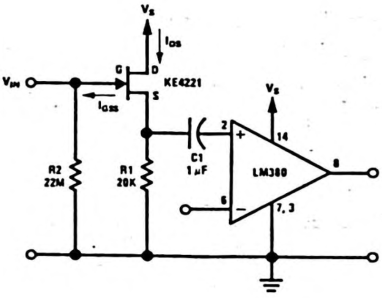


FIGURE 20.

At 20 kHz the reactance of this capacitor is approximately –j4 MΩ giving a net input impedance magnitude of 3.9 MΩ. The values chosen for R_1, R_2 and C_1 provide an overall circuit gain of at least 45 for the complete range of parameters specified for the KE4221.

When using another FET device the relevant design equations are as follows:

$$A_V = \left(\frac{R_1}{R_1 + \frac{1}{g_m}} \right) (50) \tag{7}$$

$$g_m = g_{mo} \left(1 - \frac{V_{GS}}{V_P} \right) \tag{8}$$

$$V_{GS} = I_{DS} R_1 \tag{9}$$

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \tag{10}$$

The maximum value of R_2 is determined by the product of the gate reverse leakage I_{GSS} and R_2. This voltage should be 10 to 100 times smaller than V_P. The output impedance of the FET source follower is:

$$R_o = \frac{1}{g_m} \tag{11}$$

so that the determining resistance for the inter-stage RC time constant is the input resistance of the LM380.

BOOSTED GAIN USING POSITIVE FEEDBACK

For applications requiring gains higher than the internally set gain of 50, it is possible to apply positive feedback around the LM380 for closed loop gains of up to 300. Figure 21 shows a practical example of an LM380 in a gain of 200 circuit.

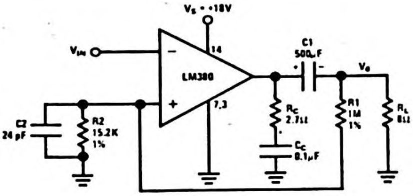


FIGURE 21. Boosted Gain of 200 Using Positive Feedback

The equation describing the closed loop gain is:

$$A_{VCL} = \frac{-A_{V(\omega)}}{1 - \frac{A_{V(\omega)}}{1 + \frac{R_1}{R_2}}} \tag{12}$$

where $A_{V(\omega)}$ is complex at high frequencies but is nominally the 40 to 60 specified on the data sheet for the pass band of the amplifier. If $1 + R_1/R_2$ approaches the value of $A_{V(\omega)}$, the denominator of equation 12 approaches zero, the closed loop gain increases toward infinity, and the circuit oscillates. This is the reason for limiting the closed loop gain values to 300 or less. Figure 22 shows the loaded and unloaded bode plot for the circuit shown in Figure 21.

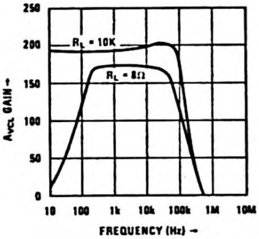


FIGURE 22. Boosted Gain Bode Plot

The 24 pF capacitor C_2 shown on Figure 21 was added to give an overdamped square wave response under full load conditions. It causes a high frequency roll-off of:

$$f_2 = \frac{1}{2\pi R_2 C_2} \tag{13}$$

The circuit of Figure 21 will have a very long (1000 sec) turn on time if R_L is not present, but only a 0.01 second turn on time with an 8Ω load.

LM381A Dual Preamplifier for Ultra-Low Noise Applications

National Semiconductor
Application Note 70
Joe E. Byerly
Dennis Bohn
August 1972

INTRODUCTION

The LM381A is a dual preamplifier expressly designed to meet the requirements of amplifying low level signals in noise critical applications. Such applications include hydrophones, scientific and instrumentation recorders, low level wideband gain blocks, tape recorders, studio sound equipment, etc.

The LM381A can be externally biased for optimum noise performance in ultra-low noise applications. When this is done the LM381A provides a wideband, high gain amplifier with noise performance that exceeds that of todays best transistors.

The amplifier can be operated in either the differential or single ended input configuration. However, for optimum noise performance, the input must be operated single ended, since both transistors contribute noise in a differential stage, degrading input noise by the factor $\sqrt{2}$. A second consideration is the design of the input bias circuitry. Both the load and biasing elements must be resistive, since active components would each contribute additional noise equal to that of the input device. Thirdly, the current density of the input device should be optimized for the source resistance of the input transducer.

Figure 1 shows the schematic diagram of one channel of LM381A (a detailed explanation of the circuit operation is given in application note AN-64). To operate the input single ended, transistor Q_2 is turned OFF by returning the base of Q_2 (Pins 2, 13) to ground.

Figures 2A and 2B show the wide-band (10 Hz – 10 kHz) input noise voltage and input noise current versus collector current for the single ended

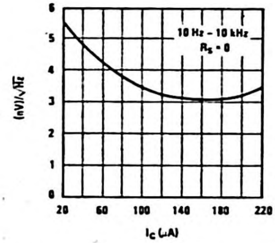


FIGURE 2A. Wideband Equivalent Input Noise Voltage vs Collector Current

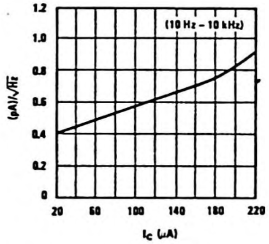


FIGURE 2B. Wideband Equivalent Input Noise Current vs Collector Current

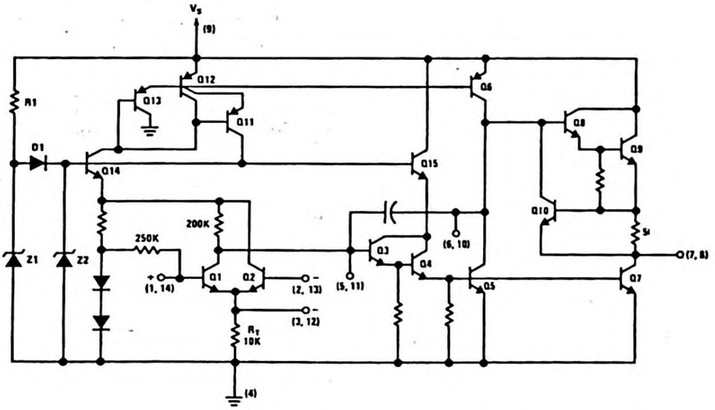


FIGURE 1. LM381A Schematic Diagram

input configuration of the LM381A. Total input noise of the amplifier is found by:

$$E_T = \sqrt{[e_n{}^2 + (i_nR_S)^2 + 4kTR_S]\ \text{B.W.}} \qquad (1)$$

Where:

e_n = amplifier noise voltage/$\sqrt{\text{Hz}}$

i_n = amplifier noise current/$\sqrt{\text{Hz}}$

R_S = source resistance Ω

k = Boltzmann's constant = 1.38×10^{-23} J/°K

T = source resistance temperature °K

B.W. = noise bandwidth

Figure 3 shows a plot of input transistor (Q_1) collector current versus source resistance for optimum noise performance of the LM381A. For source impedances less than 3 kΩ the noise voltage term (e_n) dominates and the input is biased at 170 μA which is optimum for noise voltage. In the region between 3 kΩ and 15 kΩ, both the e_n and i_nR_S terms contribute and the input should be biased as indicated by Figure 3. Above 15 kΩ, the i_nR_S term is dominant and the amplifier is operated without additional external biasing.

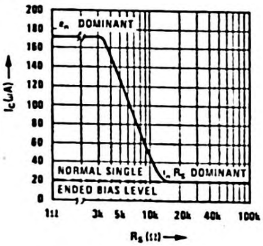


FIGURE 3. Collector Current vs Source Resistance for Optimum Noise Performance

Figure 4 shows the input stage of the LM381A with the external components added to increase the current density of transistor Q_1. Resistors R_1 and R_2 supply the additional current (I_2) to the existing collector current (I_1) which is approximately 18 μA.

The sum of resistors R_1 & R_2 is given by:

$$(R_1 + R_2) = \frac{V_S - 2.1}{I_C - 18 \times 10^{-6}} \qquad (2)$$

For DC considerations, only the sum ($R_1 + R_2$) is important. When considering the AC effects, however, the values of R_1 and R_2 become significant.

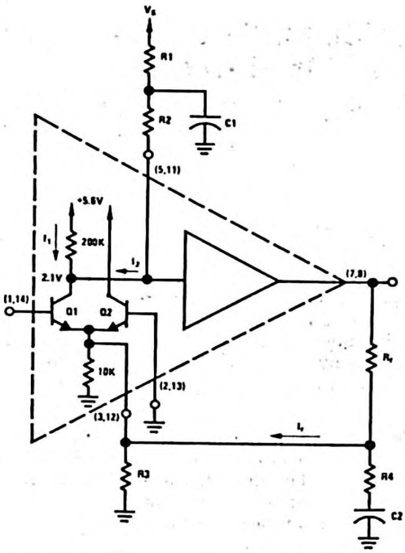


FIGURE 4. LM381A with Biasing Components for Increasing Q_1 Current Density

Since resistors R_1 and R_2 are biased from the power supply, the decoupling capacitor, C_1, is required to preserve supply rejection. The value of C_1 is given by:

$$C_1 = \frac{10^{\frac{\text{P.S.R.}}{20}}}{2\pi f_S R_1 A_1} \qquad (3)$$

Where:

P.S.R. = Supply rejection in dB referred to input

f_S = Frequency of supply ripple

A_1 = Voltage gain of first stage

As R_1 becomes smaller capacitor C_1 increases for a given power supply rejection ratio. Conversely, as R_2 becomes smaller the gain of the input stage decreases, adversely affecting noise performance. For the range of collector currents over which the LM381A is operating, a reasonable compromise is obtained with:

$$R_2 = 3\,R_1 \qquad (4)$$

The gain of the input stage is:

$$A_1 = \frac{\dfrac{(2 \times 10^5)\,R_2}{R_2 + 2 \times 10^5}}{\dfrac{.026}{I_C} + \dfrac{1}{\dfrac{1}{10^4} + \dfrac{1}{R_3} + \dfrac{1}{R_4}}} \qquad (5)$$

Resistor divider R_f/R_3 provides negative DC feedback around the amplifier establishing the quiescent operating point. R_f is found by:

$$R_f = \frac{1}{2}\left[\frac{V_S R_3 \times 10^4}{.55(R_3 + 1 \times 10^4) + I_C\,(R_3 \times 10^4)}\right] - \frac{R_3 \times 10^4}{R_3 + 1 \times 10^4} \qquad (6)$$

For DC stability let:

$$R_3 = 1\ \text{k}\Omega \text{ Maximum} \qquad (7)$$

R_f can then be found from:

$$R_f = \frac{1}{2}\left[\frac{V_S \times 10^7}{6.05 \times 10^3 + I_C \times 10^7}\right] -910 \qquad (8)$$

Where:

V_S = Supply Voltage

I_C = Q_1 Collector Current

The AC closed loop gain is set by the ratio:

$$(R_f + R_4)/R_4 \qquad (9)$$

Capacitor C_2 sets the low frequency 3 dB corner where:

$$f_o = \frac{1}{2\pi C_2 R_4} \qquad (10)$$

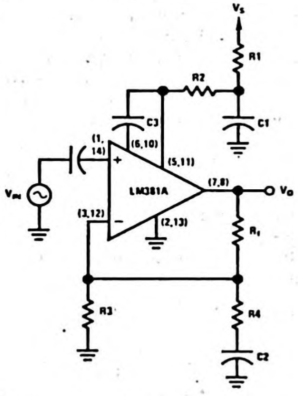


FIGURE 5. Single Ended Input Configuration with External Biasing Components

Figure 5 shows the LM381A in the single ended input configuration with the additional biasing components. Capacitor C_3 may be added to limit the amplifier bandwidth to the frequency range of interest, thus eliminating excess noise outside the pertinent bandwidth.

$$C_3 = \frac{1}{2\pi f_1 \left(\frac{.026}{I_C}\right) 10^{\frac{A}{20}}} -4 \times 10^{-12} \qquad (11)$$

Where:

f_1 = high frequency 3 dB corner

I_C = Q_1 collector current

A = mid band gain dB

Example: Design an ultra-low noise preamplifier with a gain of 1,000 operating from a 24 volt supply and a 600Ω source impedance. Bandwidth of interest is 20 Hz to 10 kHz.

1. From Figure 3 the optimum collector current for 600Ω source resistance is 170 μA.
2. From equation (2),

$$R_1 + R_2 = \frac{V_S - 2.1}{I_C - 18 \times 10^{-6}}$$

$$= \frac{24 - 2.1}{(170 - 18) \times 10^{-6}}$$

$$R_1 + R_2 = 1.44 \times 10^5.$$

3. From equation (4),

$$R_2 = 3\,R_1 = \frac{1.44 \times 10^5}{1.333} = 1.08 \times 10^5$$

$$R_2 \approx 100\ \text{k}\Omega.$$

$$R_1 = 36 \times 10^3 \approx 39\ \text{k}\Omega.$$

4. From equation (7) let $R_8 = 1$ kΩ.
5. From equation (8),

$$R_f = \frac{1}{2}\left[\frac{V_S \times 10^7}{6.05 \times 10^3 + I_C \times 10^7}\right] -910$$

$$R_f = \frac{1}{2}\left[\frac{24 \times 10^7}{6.05 \times 10^3 + 1.7 \times 10^3}\right] -910$$

$$R_f = 2.67 \times 10^4 \approx 27\ \text{k}\Omega.$$

6. For a gain of 1,000; equation (9),

$$\text{Amplifier Gain} = \frac{(R_f + R_4)}{R_4} = 1{,}000$$

$$R_4 = \frac{27 \times 10^3}{10^3} = 27\Omega.$$

7. For a low corner frequency, f_o, of 20 Hz; equation (10),

$$C_2 = \frac{1}{2\pi f_o R_4} = \frac{1}{6.28 \times 20 \times 27.}$$

$$= 2.95 \times 10^{-4}$$

$$C_2 \approx 300\ \mu\text{F}.$$

8. From equation (5) the gain of the input stage is:

$$A_1 = \frac{\dfrac{(2 \times 10^5)\,R_2}{R_2 + 2 \times 10^5}}{\dfrac{.026}{I_C} + \dfrac{1}{\dfrac{1}{10^4} + \dfrac{1}{R_3} + \dfrac{1}{R_4}}}$$

$$A_1 = \frac{\dfrac{2 \times 10^5 \times 10^5}{10^5 + 2 \times 10^5}}{\dfrac{.026}{1.7 \times 10^{-4}} + \dfrac{1}{\dfrac{1}{10^4} + \dfrac{1}{10^3} + \dfrac{1}{27}}}$$

$$A_1 = 372.$$

9. For 100 dB supply rejection at 120 Hz. Equation (3),

$$C_1 = \frac{10^{\frac{P.S.R.}{20}}}{2\pi f\, R_1 A_1} = \frac{10^{\frac{100}{20}}}{2\pi \times 120 \times 39 \times 10^3 \times 372}$$

$$C_1 = \frac{10^5}{1.09 \times 10^{10}} = 9.1 \times 10^{-6}$$

$$C_1 \approx 10\,\mu F.$$

10. For a high frequency corner, f_1, of 10 kHz; equation (11),

$$C_3 = \frac{1}{2\pi f_1 \left(\dfrac{.026}{I_C}\right) 10^{\frac{A}{20}}} - 4 \times 10^{-12}$$

$$C_3 = \frac{1}{6.28 \times 10^4 \times 1.53 \times 10^2 \times 10^4} - 4 \times 10^{-12}$$

$$C_3 = 6.4 \times 10^{-12} \approx 6.8\ pF.$$

The noise performance of the circuit of Figure 6 can be found with the aid of Figures 2A and 2B and equation (1). From Figures 2A and 2B the noise voltage (e_n) and noise current (i_n) at 170 μA I_C are: $e_n = 3.0\ nV/\sqrt{Hz}$, $i_n = .72\ pA/\sqrt{Hz}$. From equation (1)

$$E_T = \sqrt{[e_n^2 + (i_n R_S)^2 + 4KTR_S]\ B.W.}$$

$$= \sqrt{[(3.0 \times 10^{9})^2 + (7.2 \times 10^{13} \times 600)^2 + 9.94 \times 10^{18}]\ 10^4}$$

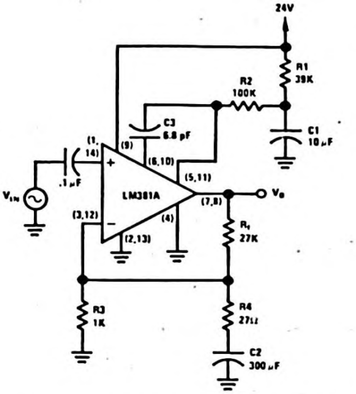


FIGURE 6. Typical Application with Increased Current Density of Input Stage

Total Wideband Noise Voltage $= 4.37 \times 10^{-7}$V.

$$\text{Wideband Noise Figure} = 10 \log \frac{4KTR_S + e_n^2 + (i_n R_S)^2}{4KTR_S}$$

$$= 10 \log \frac{9.94 \times 10^{-18} + 9.0 \times 10^{-18} + 1.86 \times 10^{-19}}{9.94 \times 10^{-18}}$$

$= 10 \log 1.92 = 2.83$ dB.

CONCLUSION

In applications requiring a wide band, high gain preamplifier where noise performance is critical, the LM381A is unsurpassed. In addition to ultra low noise performance, the LM381A offers two completely independent amplifiers, each with an internal power supply decoupler-regulator providing 120 dB supply rejection and 60 dB channel separation.

Other outstanding features include, high gain (112 dB) large output voltage swing (V_S – 2V) peak to peak, wide supply operating range (9 – 40V), wide power bandwidth (75 kHz, 20 $V_{p\text{-}p}$), internal frequency compensation, and short-circuit protection

REFERENCE

J.E. Byerly and E.L. Long – *"LM381 Low Noise Dual Preamplifier"* National Semiconductor Corporation AN-64, May 1972.

Micropower Circuits Using the LM4250 Programmable Op Amp

National Semiconductor
Application Note 71
Marvin K. Vander Kooi
George Cleveland
July 1972

INTRODUCTION

The LM4250 is a highly versatile monolithic operational amplifier. A single external programming resistor determines the quiescent power dissipation, input offset and bias currents, slew rate, gain-bandwidth product, and input noise characteristics of the amplifier. Since the device is in effect a different op amp for each externally programmed set current, it is possible to use a single stock item for a variety of circuit functions in a system.

This paper describes the circuit operation of the LM4250, various methods of biasing the device, frequency response considerations, and some circuit applications exercising the unique characteristics of the LM4250.

CIRCUIT DESCRIPTION LM4250

The LM4250 has two special features when compared with other monolithic operational amplifiers. One is the ability to externally set the bias current levels of the amplifiers, and the other is the use of PNP transistors as the differential input pair.

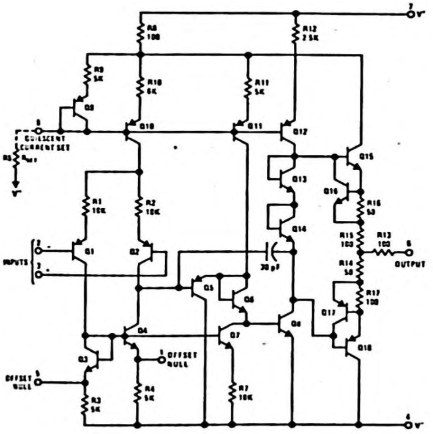


FIGURE 1. LM4250 Schematic Diagram

Referring to Figure 1, Q_1 and Q_2 are high current gain lateral PNPs connected as a differential pair. R_1 and R_2 provide emitter degeneration for greater stability at high bias currents. Q_3 and Q_4 are used as active loads for Q_1 and Q_2 to provide high gain and also form a current inverter to provide the maximum drive for the single ended output into Q_5. Q_5 is an emitter follower which prevents loading of the input stage by the succeeding amplifier stage.

One advantage of this lateral PNP input stage is a common mode swing to within 200 mV of the negative supply. This feature is especially useful in single supply operation with signals referred to ground. Another advantage is the almost constant input bias current over a wide temperature range. The input resistance R_{IN} is approximately equal to $2\beta\ (R_E + r_e)$ where β is the current gain, r_e is the emitter resistance of one of the input lateral PNPs, and R_E is the resistance of one of the 10 kΩ emitter resistor. Using a DC beta of 100 and the normal temperature dependent expression for r_e gives:

$$R_{IN} \approx 2\,\text{M}\Omega + 2\,\frac{kT}{qI_B}. \tag{1}$$

where I_B is input bias current. At room temperature this formula becomes:

$$R_{IN} \approx 2\,\text{M}\Omega + \frac{52\,\text{mV}}{I_B}. \tag{2}$$

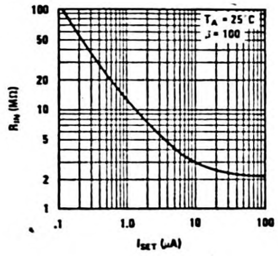


FIGURE 2. Input Resistance vs I_{SET}

Figure 2 gives a typical plot of R_{IN} vs I_{set} derived from the above equation.

Continuing with the circuit description, Q_6 level shifts downward to the base of Q_8 which is the second stage amplifier. Q_8 is run as a common emitter amplifier with a current source load (Q_{12}) to provide maximum gain. The output of Q_8 drives the class B complementary output stage composed of Q_{15} and Q_{18}.

The bias current levels in the LM4250 are set by the amount of current (I_{set}) drawn out of Pin 8. The constant current sources Q_{10}, Q_{11}, and Q_{12} are controlled by the amount of I_{set} current through the diode connected transistor Q_9 and resistor R_9. The constant collector current from Q_{10} biases the differential input stage. Therefore, the level Q_{10} is set at will control such amplifier characteristics as input bias current, input resistance, and amplifier slew rate. Current source Q_{11} biases Q_5 and Q_6. The current ratio between Q_5 and Q_6 is controlled by constant current sink Q_7. Current source Q_{12} sets the currents in diodes Q_{13} and Q_{14} which bias the output stage to the verge of conduction thereby eliminating the dead zone in the class B output. Q_{12} also acts as the load for Q_8 and limits the drive current to Q_{15}.

The output current limiting is provided by Q_{16} and Q_{17} and their associated resistors R_{16} and R_{17}. When enough current is drawn from the output, Q_{16} turns on and limits the base drive of Q_{15}. Similarly Q_{17} turns on when the LM4250 attempts to sink too much current, limiting the base drive of Q_{18} and therefore output current. Frequency compensation is provided by the 30 pF capacitor across the second stage amplifier, Q_8, of the LM4250. This provides a 6 dB per octave rolloff of the open loop gain.

BIAS CURRENT SETTING PROCEDURE

The single set resistor shown in Figure 3a offers the most straightforward method of biasing the LM4250. When the set resistor is connected from Pin 8 to ground the resistance value for a given set current is:

$$R_{SET} = \frac{V^+ - 0.5}{I_{SET}} \qquad (3)$$

The 0.5 volts shown in Equation 3 is the voltage drop of the master bias current diode connected transistor on the integrated circuit chip. In applications where the regulation of the V^+ supply with respect to the V^- supply (as in the case of tracking regulators) is better than the V^+ supply with respect to ground the set resistor should be connected from Pin 8 to V^-. R_{SET} is then:

$$R_{SET} = \frac{V^+ + |V^-| - 0.5}{I_{SET}} \qquad (4)$$

The transistor and resistor scheme shown in Figure 3b allows one to switch the amplifier off without disturbing the main V^+ and V^- power supply connections. Attaching C_1 across the circuit prevents any switching transient from appearing at the amplifier output. The dual scheme shown in Figure 3c has a constant set current flowing through R_{S1} and a variable current through R_{S2}. Transistor Q_2 acts as an emitter follower current sink whose value depends on the control voltage V_c on the base. This circuit provides a method of varying the amplifier's characteristics over a limited range while the amplifier is in operation. The FET circuit shown in Figure 3d covers the full range of set currents in response to as little as a 0.5V gate potential change on a low pinch-off voltage FET such as the 2N3687. The limit resistor prevents excessive current flow out of the LM4250 when the FET is fully turned on.

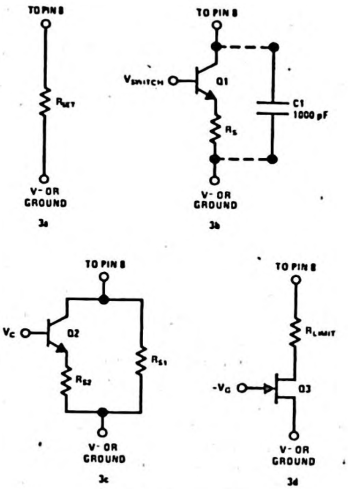


FIGURE 3. Biasing Schemes

FREQUENCY RESPONSE OF A PROGRAMMABLE OP AMP

This section provides a method of determining the sine and step voltage response of a programmable op amp. Both the sine and step voltage responses of an amplifier are modified when the rate of change of the output voltage reaches the slew rate limit of the amplifier. The following analysis develops the Bode plot as well as the small signal and slew rate limited responses of an amplifier to these two basic categories of waveforms.

Small Signal Sine Wave Response

The key to constructing the Bode plot for a programmable op amp is to find the gain bandwidth product, GBWP, for a given set current. Quiescent power drain, input bias current, or slew rate considerations usually dictate the desired set current. The data sheet curve relating GBWP to set current provides the value of GBWP which when divided by one yields the unity gain crossover of f_u. Assuming a set current of 6 μA gives a GBWP of 200,000 Hz and therefore an f_u of 200 kHz for the example shown in Figure 4. Since the device has a single dominant pole, the rolloff slope is −20 dB of gain per decade of frequency (−6 dB/octave). The dotted line shown

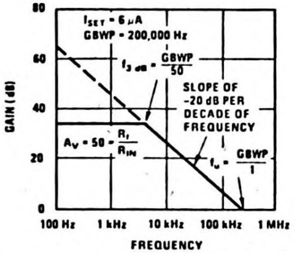


FIGURE 4. Bode Plot

on Figure 4 has this slope and passes through the 200 kHz f_u point. Arbitrarily choosing an inverting amplifier with a closed loop gain magnitude of 50 determines the height of the 34 dB horizontal line shown in Figure 4. Graphically finding the intersection of the sloped line and the horizontal line or mathematically dividing GBWP by 50 determines the 3 dB down frequency of 4 kHz for the closed loop response of this amplifier configuration. Therefore, the amplifier will now apply a gain of −50 to all small signal sine waves at frequencies up to 4 kHz. For frequencies above 4 kHz, the gain will be as shown on the sloped portion of the Bode plot.

Small Signal Step Input Response

The amplifier's response to a positive step voltage change at the input will be an exponentially rising waveform whose rise time is a function of the closed loop 3 dB down bandwidth of the amplifier. The amplifier may be modeled as a single pole low pass filter followed by a gain of 50 wideband amplifier. From basic filter theory*, the 10% to 90% rise time of a single pole low pass filter is:

$$t_r = \frac{0.35}{f_{3\,dB}} \qquad (5)$$

For the example shown in Figure 4 the 4 kHz 3 dB down frequency would give a rise time of 87.5 μs.

Slew Rate Limited Large Signal Response

The final consideration, which determines the upper speed limitation on the previous two types of signal responses, is the amplifier slew rate. The slew rate of an amplifier is the maximum rate of change of the output signal which the amplifier is capable of delivering. In the case of sinosoidal signals, the maximum rate of change occurs at the zero crossing and may be derived as follows:

$$v_o = V_p \sin 2\pi f\, t \qquad (6)$$

$$\frac{d\,v_o}{d\,t} = 2\pi\, f\, V_p \cos 2\pi\, f\, t \qquad (7)$$

$$\left.\frac{d\,v_o}{d\,t}\right|_{t=0} = 2\pi\, f\, V_p \qquad (8)$$

$$S_r = 2\pi\, f_{MAX}\, V_p \qquad (9)$$

where:

v_o = output voltage

V_p = peak output voltage

S_r = maximum $\frac{d\,v_o}{d\,t}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{MAX} = \frac{S_r}{2\pi\, V_p} \qquad (10)$$

Figure 5 shows a quick reference graphical presentation of this formula with the area below any V_{peak} line representing an undistorted small signal sine wave response for a given frequency and amplifier slew rate and the area above the V_{peak} line representing a distorted sinewave response due to slew rate limiting for a sine wave with the given V_{peak}.

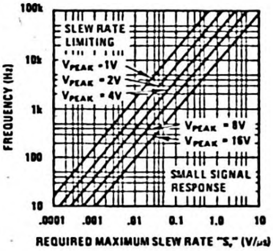


FIGURE 5. Frequency vs Slew Rate Limit vs Peak Output Voltage

Large signal step voltage changes at the output will have a rise time as shown in equation 5 until a signal with a rate of output voltage change equal to the slew rate of the amplifier occurs. At this point the output will become a ramp function with a slope equal to S_r. This action occurs when:

$$S_r \leq \frac{V_{step}}{t_r} \qquad (11)$$

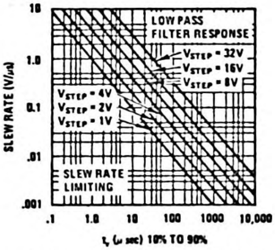


FIGURE 6. Slew Rate vs Rise Time vs Step Voltage

Figure 6 graphically expresses this formula and shows the maximum amplitude of undistorted step voltage for a given slew rate and rise time.

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*See reference.

The area above each step voltage line represents the undistorted low pass filter type response mode of the amplifier. If the intersection of the rise time and slew rate values of a particular amplifier configuration falls below the expected step voltage amplitude line, the rise time will be determined by the slew rate of the amplifier. The rise time will then be equal to the amplitude of the step divided by the slew rate S_r.

Full Power Bandwidth

The full power bandwidth often found on amplifier specification sheets is the range of frequencies from zero to the frequency found at the intersection on Figure 5 of the maximum rated output voltage and the slew rate S_r of the amplifier. Mathematically this is:

$$f_{\text{full power}} = \frac{S_r}{2\pi V_{\text{rated}}} \tag{12}$$

The full power bandwidth of a programmable amplifier such as the LM4250 varies with the master bias set current.

The above analysis of sine wave and step voltage amplifier responses applies for all single dominant pole op amps such as the LM101A, LM107, LM108A, LM112, LM118, and LM741 as well as the LM4250 programmable op amp.

500 NANO-WATT X10 AMPLIFIER

The X10 inverting amplifier shown in Figure 7 demonstrates the low power capability of the LM4250 at extremely low values of supply voltage and set current. The circuit draws 260 nA from the +1.0V supply of which 50 nA flows through the 12 MΩ set resistor. The current into the −1.0V supply is only 210 nA since the set resistor is tied to ground rather than V^-. Total quiescent power dissipation is:

$$P_D = (260\text{ nA})\,(1\text{V}) + (210\text{ nA})\,(1\text{V}) \tag{13}$$

$$P_D = 470\text{ nW} \tag{14}$$

The slew rate determined from the data sheet typical performance curve is 1 V/ms for a .05 μA set current. Samples of actual values observed were 1.2 V/ms for the negative slew rate and 0.85 V/ms for the positive slew rate. This difference occurs due to the non-symmetry in the current sources used for charging and discharging the internal 30 pF compensation capacitor.

The 3 dB down (gain of −7.07) frequency observed for this configuration was approximately 300 Hz which agrees fairly closely with the 3.5 kHz GBWP divided by 10 taken from an extrapolation of the data sheet typical GBWP versus set current curve.

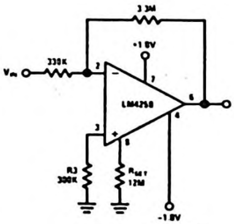

FIGURE 7. 500 nW x 10 Amplifier

Peak-to-peak output voltage swing into a 100 kΩ load is 0.7V or ±0.35V peak. An increase in supply voltage to ±1.35V such as delivered by a pair of mercury cells directly increases the output swing by ±0.35V to 1.4V peak-to-peak. Although this increases the power dissipation to approximately 1 μW per battery, a power drain of 15 μW or less will not affect the shelf life of a mercury cell.

MICRO-POWER MONITOR WITH HIGH CURRENT SWITCH

Figure 8 shows the combination of a micro-power comparator and a high current switch run from a separate supply. This circuit provides a method of continuously monitoring an input voltage while dissipating only 100 μW of power and still being capable of switching a 500 mA load if the input exceeds a given value. The reference voltage can be any value between +8.5V and −8.5V. With a minimum gain of approximately 100,000 the comparator can resolve input voltage differences down into the 0.2 mV region.

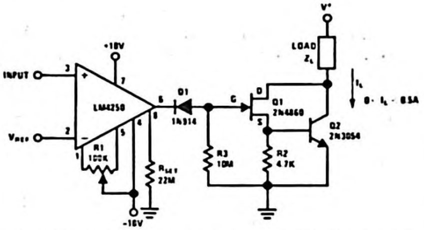

FIGURE 8. μ–Power Comparator with High Current Switch

The bias current for the LM4250 shown in Figure 8 is set at 0.44 μA by the 22 MΩ R_{set} resistor. This results in a total comparator power drain of 100 μW and a slew rate of approximately 11 V/ms in the positive direction and 12.8 V/ms in the negative direction. Potentiometer R_1 provides input offset nulling capability for high accuracy applications. When the input voltage is less than the reference voltage, the output of the LM4250 is at approximately −9.5V causing diode D_1 to conduct. The gate of Q_1 is held at −8.8V by the voltage developed across R_3. With a large negative voltage on the gate of Q_1 it turns off and removes the base drive from Q_2. This results in a high voltage or open switch condition at the collector of Q_2. When the input voltage exceeds the reference voltage, the LM4250 output goes to +9.5V causing D_1 to be reverse biased. Q_1 turns on as does Q_2, and the collector of Q_2 drops to approximately 1V while sinking the 500 mA of load current.

The load denoted as Z_L can be resistor, relay coil, or indicator lamp as required; but the load current should not exceed 500 mA. For V^+ values of less than 15V and I_L values of less than 25 mA both Q_2 and R_2 may be omitted. With only the 2N4860 JFET as an output device the circuit is still capable of driving most common types of indicator lamps.

IC METER AMPLIFIER RUNS ON TWO FLASHLIGHT BATTERIES

Meter amplifiers normally require one or two 9V transistor batteries. Due to the heavy current drain on these supplies, the meters must be switched to the OFF position when not in use. The meter circuit described here operates on two 1.5V flashlight batteries and has a quiescent power drain so low that no ON-OFF switch is needed. A pair of Eveready No. 950 "D" cells will serve for a minimum of one year without replacement. As a DC ammeter, the circuit will provide current ranges as low as 100 nA full-scale.

The basic meter amplifier circuit shown in Figure 9 is a current-to-voltage converter. Negative feedback around the amplifier insures that currents I_{IN} and I_f are always equal, and the high gain of the op amp insures that the input voltage between Pins 2 and 3 is in the microvolt region. Output voltage V_o is therefore equal to $-I_fR_f$. Considering the ±1.5V sources (±1.2V end-of-life) a practical value of V_o for full scale meter deflection is 300 mV. With the master bias-current setting resistor (R_s) set at 10 MΩ, the total quiescent current drain of the circuit is 0.6 μA for a total power supply drain of 1.8 μW. The input bias current, required by the amplifier at this low level of quiescent current, is in the range of 600 pA.

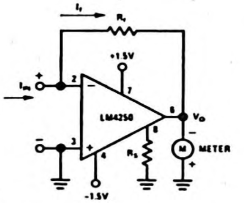

FIGURE 9. Basic Meter Amplifier

The Complete Nanoammeter

The complete meter amplifier shown in Figure 10 is a differential current-to-voltage converter with input protection, zeroing and full scale adjust provisions, and input resistor balancing for minimum offset voltage. Resistor R'_f (equal in value to R_f for measurements of less than 1 μA) insures that the input bias currents for the two input terminals of the amplifier do not contribute significantly to an output error voltage. The output voltage V_o for the differential current-to-voltage converter is equal to $-2I_fR_f$ since the floating input current I_{IN} must flow through R_f and R'_f. R'_f may be omitted for R_f values of 500 kΩ or less, since a resistance of this value contributes an error of less than 0.1% in output voltage. Potentiometer R_2 provides an electrical meter zero by forcing the input offset voltage V_{os} to zero. Full scale meter deflection is set by R_1. Both R_1 and R_2 only need to be set once for each op amp and meter combination. For a 50 microamp 2 kΩ meter movement, R_1 should be about 4 kΩ to give full scale meter deflection in response to a 300 mV output voltage. Diodes D_1 and D_2 provide full input protection for overcurrents up to 75 mA.

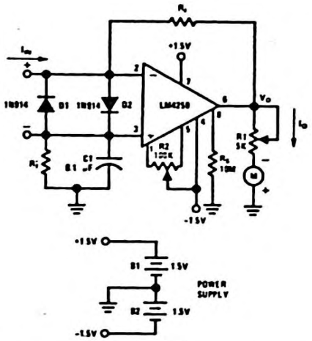

FIGURE 10. Complete Meter Amplifier

Resistance Values for
DC Nano and Micro Ammeter

I FULL SCALE	R_f (Ω)	R'_f (Ω)
100 nA	1.5M	1.5M
500 nA	300k	300k
1 μA	300k	0
5 μA	60k	0
10 μA	30k	0
50 μA	6k	0
100 μA	3k	0

With an R_f resistor value of 1.5M the circuit in Figure 10 becomes a nanommeter with a full scale reading capability of 100 nA. Reducing R_f to 3 kΩ in steps, as shown in Figure 10 increases the full scale deflection to 100 μA, the maximum for this circuit configuration. The voltage drop across the two input terminals is equal to the output voltage V_o divided by the open loop gain. Assuming an open loop gain of 10,000 gives an input voltage drop of 30 μV or less.

Circuit for Higher Current Readings

For DC current readings higher than 100 μA, the inverting amplifier configuration shown in Figure 11 provides the required gain. Resistor R_A develops a voltage drop in response to input current I_A. This voltage is amplified by a factor equal to the ratio of R_f/R_B. R_B must be sufficiently larger than R_A, so as not to load the input signal. Figure 11 also shows the proper values of R_A, R_B and R_f for full scale meter deflections of from 1 mA to 10A.

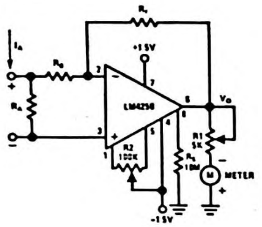

FIGURE 11. Ammeter

Resistance Values for
DC Ammeter

I FULL SCALE	R_A (Ω)	R_B (Ω)	R_f (Ω)
1 mA	3.0	3k	300k
10 mA	.3	3k	300k
100 mA	.3	30k	300k
1A	.03	30k	300k
10A	.03	30k	30k

A 10 mV to 100V Full-Scale Voltmeter

A resistor inserted in series with one of the input leads of the basic meter amplifier converts it to a wide range voltmeter circuit, as shown in Figure 12. This inverting amplifier has a gain varying from −30 for the 10 mV full scale range to −0.003 for the 100V full scale range. Figure 12 also lists the proper values of R_v, R_f, and R'_f for each range. Diodes D_1 and D_2 provide complete amplifier protection for input overvoltages as high as 500V on the 10 mV range, but if overvoltages of this magnitude are expected under continuous operation, the power ratingof R_v should be adjusted accordingly.

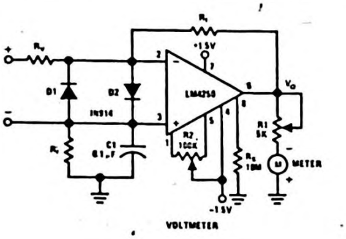

FIGURE 12. Voltmeter

Resistance Values for a
DC Voltmeter

V FULL SCALE	R_V (Ω)	R_f (Ω)	R'_f (Ω)
10 mV	100k	1.5M	1.5M
100 mV	1M	1.5M	1.5M
1V	10M	1.5M	1.5M
10V	10M	300k	0
100V	10M	30k	0

LOW FREQUENCY PULSE GENERATOR USING A SINGLE +5V SUPPLY

The variable frequency pulse generator shown in Figure 13 provides an example of the LM4250 operated from a single supply. The circuit is a buffered output free running multivibrator with a constant width output pulse occurring with a frequency determined by potentiometer R_2.

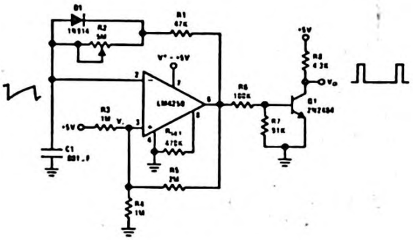

FIGURE 13. Pulse Generator

The LM4250 acts as a comparator for the voltages found at the upper plate of capacitor C_1 and at the reference point denoted as V_r on Figure 13. Capacitor C_1 charges and discharges with a peak-to-peak amplitude of approximately 1V determined by the shift in reference voltage V_r at Pin 3 of the op amp. The charge path of C_1 is from the amplifier output, which is at its maximum positive voltage V_{HIGH} (approximately V^+ −0.5V), through R_1 and through the potentiometer R_2. Diode D_1 is reverse biased during the charge period. When C_1 charges to the V_r value determined by the net result of V_{HIGH} through resistor R_5 and V^+ through the voltage divider made up of resistors R_3 and R_4 the amplifier swings to its lower limit of approximately 0.5V causing C_1 to begin discharging. The discharge path is through the forward biased diode D_1, through resistor R_1, and into Pin 6 of the op amp. Since the impedance in the discharge path does not vary for R_2 settings of from 3 kΩ to 5 MΩ, the output pulse maintains a constant pulse width of 41 μs ±1.5 μs over this range of potentiometer settings. Figure 14 shows the output pulse frequency variation from 6 kHz down to 360 Hz as R_2 places from 100 kΩ up to 5 MΩ of additional resistance in the charge path of C_1. Setting R_2 to zero ohms will short out diode D_1 and cause a symmetrical square wave output at a frequency of 10 kHz. Increasing the value of C_1 will lower the range of frequencies available in response to the R_2 variation shown on Figure 14. Electrolytic capacitors may be used for the larger values of C_1 since it has only positive voltages applied to it.

The output buffer Q_1 presents a constant load to the op amp output thereby preventing frequency variations caused by V_{HIGH} and V_{LOW} voltages changing as a function of load current. The output of Q_1 will interface directly with a standard TTL or DTL logic device. Reversing diode D_1 will invert

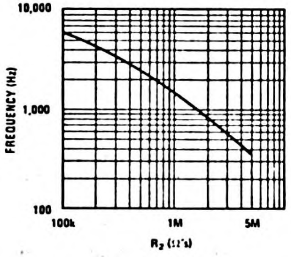

FIGURE 14. Pulse Frequency vs R_2

the polarity of the generator output providing a series of negative going pulses dropping from +5V to the saturation voltage of Q_1.

The change in output frequency as a function of supply voltage is less than ±4% for a V^+ change of from 4V to 10V. This stability of frequency versus supply voltage is due to the fact that the reference voltage V_r and the drive voltage for the capacitor are both direct functions of V^+.

The power dissipation of the free running multivibrator is 300 μW and the power dissipation of the buffer circuit is approximately 5.8 mW.

X100 INSTRUMENTATION AMPLIFIER

The instrumentation amplifier circuit shown in Figure 15 has a full differential input center tapped to ground. With the bias current set at approximately 0.1 μA, the impedance looking into either V_{IN_1} or V_{IN_2} is 100 MΩ with respect to ground, and the input bias current at either terminal is 0.2 nA. The two non-inverting input stages A_1 and A_2 apply a gain of 10 to the input signal, and the differential output stage applies an additional gain of −10 for a net amplifier gain of −100:

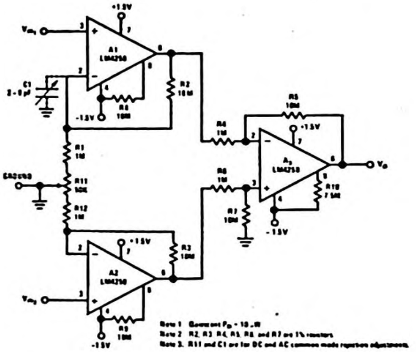
V_{IN_1}
+1.5V
A1
LM4250
C1
2-8 pF
R8
10M
R2
10M
-1.5V
R1
1M
GROUND
R11
50K
R12
1M
R4
1M
R5
10M
A_3
LM4250
V_o
R6
1M
R7
10M
R10
7.5M
-1.5V
A2
LM4250
R3
10M
V_{IN_2}
R9
10M
-1.5V
Note 1 Quiescent P_D = 10 μW
Note 2 R2, R3, R4, R5, R6 and R7 are 1% resistors
Note 3. R11 and C1 are for DC and AC common mode rejection adjustments

FIGURE 15. x 100 Instrumentation Amplifier

$$V_o = -100\,(V_{IN_1} - V_{IN_2})\,. \tag{15}$$

The entire circuit can run from two 1.5V batteries connected directly (no power switch) to the V^+ and V^- terminals. With a total current drain of 2.8 μA the quiescent power dissipation of the circuit is 8.4 μW. This is low enough to have no significant effect on the shelf life of most batteries.

Potentiometer R_{11} provides a means for matching the gains of A_1 and A_2 to achieve maximum DC common mode rejection ratio CMRR. With R_{11} adjusted to its null point for DC common mode rejection the small AC CMRR trimmer capacitor C_1 will normally give an additional 10 to 20 dB of CMRR over the operating frequency range. Since C_1 actually balances wiring capacitance rather than amplifier frequency characteristics, it may be necessary to attach it to Pin 2 of either A_1 or A_2 as required. Figure 16 shows the variation of CMRR (referred to the input) with frequency for this configuration. Since the circuit applies a gain of 100 or 40 dB to an input signal, the actual observed rejection ratio is the difference between the CMRR curve and A_V curve. For example, a 60 Hz common mode signal will be attenuated by 67 dB minus 40 dB or 27 dB for an actual rejection ratio of V_{IN}/V_O equal to 22.4.

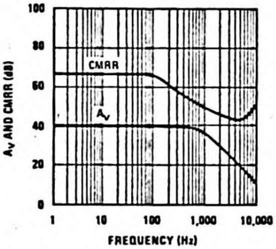

FIGURE 16. A_V and CMRR vs Frequency

The maximum peak-to-peak output signal into a 100 kΩ load resistor is approximately 1.8V. With no input signal, the noise seen at the output is approximately 0.8 mV_{RMS} or 8 μV_{RMS} referred to the input. When doing power dissipation measurements on this circuit, it should be kept in mind that even a 1 MΩ oscilloscope probe placed between +1.5V and −1.5V will more than double the power drawn from the batteries.

5V REGULATOR FOR CMOS LOGIC CIRCUITS

The ideal regulator for low power CMOS logic elements should dissipate essentially no power when the CMOS devices are running at low frequencies, but be capable of delivering full output power on demand when the CMOS devices are running in the 0.1 MHz to 10 MHz region. With a 10V input voltage, the regulator shown in Figure 17 will dissipate 350 μW in the stand-by mode but will deliver up to 50 mA of continuous load current when required.

The circuit is basically a boosted output voltage-follower referenced to a low current zener diode.

The voltage divider consisting of R_2 and R_3 provides a 5V tap voltage from the 6.5V reference diode to determine the regulator output. Since a standard 6.5V zener diode does not exhibit good regulation in the 2 μA to 60 μA reverse current region, Q_2 must be a special device. An NPN transistor with its collector and base terminals grounded and its emitter tied to the junction of R_1 and R_2 exhibits a well-controlled base emitter reverse breakdown voltage. A National Semiconductor process 25 small signal NPN transistor sorted to a 2N registration such as 2N3252 has a BV_{EBO} at 10 μA specified as 5.5V minimum, 6.5V typical, and 7.0V maximum. Using a diode connected 2N3252 as a reference, the regulator output voltage changed 78 mV in response to an 8V to 36V change in the input voltage. This test was done under both no load and full load conditions and represents a line regulation of better than 1.6%.

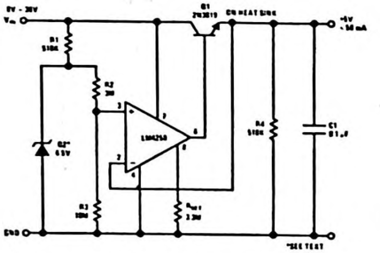

FIGURE 17. 350 μW Quiescent Drain 5 Volt Regulator

A load change from 10 μA to 50 mA caused a 1 mV change in output voltage giving a load regulation value of .05%. When operating the regulator at load currents of less than 25 mA, no heat sink is required for Q_1. For load currents in excess of 50 mA, Q_1 should be replaced by a Darlington pair with the 2N3019 acting as a driver for a higher power device such as a 2N3054.

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The LM3900 — A New Current-Differencing Quad of ± Input Amplifiers

National Semiconductor
Application Note 72
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PREFACE

With all the existing literature on "how to apply op amps" why should another application note be produced on this subject? There are two answers to this question; 1) the LM3900 operates in quite an unusual manner (compared to a conventional op amp) and therefore needs some explanation to familiarize a new user with this product, and 2) the standard op amp applications assume a split power supply (±15 V_{DC}) is available and our emphasis here is directed toward circuits for lower cost single power supply control systems. Some of these circuits are simply "re-biased" versions of conventional handbook circuits but many are new approaches which are made possible by some of the unique features of the LM3900.

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THE LM3900—A NEW CURRENT-DIFFERENCING QUAD OF ±INPUT AMPLIFIERS

1.0 AN INTRODUCTION TO THE NEW "NORTON" AMPLIFIER

The LM3900 represents a departure from conventional amplifier designs. Instead of using a standard transistor differential amplifier at the input, the non-inverting input function has been achieved by making use of a "current-mirror" to "mirror" the non-inverting input current about ground and then to extract this current from that which is entering the inverting input terminal. Whereas the conventional op amp differences input voltages, this amplifier differences input currents and therefore the name "Norton Amp" has been used to indicate this new type of operation. Many biasing advantages are realized when operating with only a single power supply voltage. The fact that currents can be passed between the input terminals allows some unusual applications. If external, large valued input resistors are used (to convert from input voltages to input currents) most of the standard op amp applications can be realized.

Many industrial electronic control systems are designed that operate off of only a single power supply voltage. The conventional integrated-circuit operational amplifier (IC op amp) is typically designed for split power supplies (± 15 V_{DC}) and suffers from a poor output voltage swing and a rather large minimum common-mode input voltage range (approximately + 2 V_{DC}) when used in a single power supply application. In addition, some of the performance characteristics of these op amps could be sacrificed—especially in favor of reduced costs.

To meet the needs of the designers of low-cost, single-power-supply control systems, a new internally compensated amplifier has been designed that operates over a power supply voltage range of +4 V_{DC} to 36 V_{DC} with small changes in performance characteristics and provides an output peak-to-peak voltage swing that is only 1V less than the magnitude of the power supply voltage. Four of these amplifiers have been fabricated on a single chip and are provided in the standard 14-pin dual-in-line package.

The cost, application and performance advantages of this new quad amplifier will guarantee it a place in many single power supply electronic systems. Many of the "housekeeping" applications which are now handled by standard IC op amps can also be handled by this "Norton" amplifier operating off the existing ± 15 V_{DC} power supplies.

1.1 Basic Gain Stage

The gain stage is basically a single common-emitter amplifier. By making use of current source loads, a large voltage gain has been achieved which is very constant over temperature changes. The output voltage has a large dynamic range, from essentially ground to one V_{BE} less than the power supply voltage. The output stage is biased class A for small signals but converts to class B to increase the load current which can be "absorbed" by the amplifier under large signal conditions. Power supply current drain is essentially independent of the power supply voltage and ripple on the supply line is also rejected. A very small input biasing current allows high impedance feedback elements to be used and even lower "effective" input biasing currents can be realized by using one of the amplifiers to supply essentially all of the bias currents for the other amplifiers by making use of the "matching" which exists between the 4 amplifiers which are on the same IC chip (see Figure 84).

The simplest inverting amplifier is the common-emitter stage. If a current source is used in place of a load resistor, a large open-loop gain can be obtained, even at low power-supply voltages. This basic stage (Figure 1) is used for the amplifier.

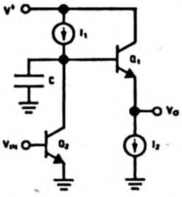


FIGURE 1. Basic Gain Stage

All of the voltage gain is provided by the gain transistor, Q_2, and an output emitter-follower transistor, Q_1, serves to isolate the load impedance from the high impedance that exists at the collector of the gain transistor, Q_2. Closed-loop stability is guaranteed by an on-chip capacitor C=3 pF, which provides the single dominant open-loop pole. The output emitter-follower is biased for class-A operation by the current source I_2.

This basic stage can provide an adequate open-loop voltage gain (70 dB) and has the desired large output voltage swing capability. A disadvantage of this circuit is that the DC input current, I_{IN}, is large; as it is essentially equal to the maximum output current, I_{OUT}, divided by β^2. For example, for an output current capability of 10 mA the input current would be at least 1 μA (assuming $\beta^2 = 10^4$). It would be desirable to further reduce this by adding an additional transistor to achieve an overall β^3 reduction. Unfortunately, if a transistor is added at the output (by making Q_1 a Darlington pair) the peak-to-peak output voltage swing would be somewhat reduced and if Q_2 were made a Darlington pair the DC input voltage level would be undesirably doubled.

To overcome these problems, a lateral PNP transistor has been added as shown in Figure 2. This connection neither reduces the output voltage swing nor raises the DC input voltage, but does provide the additional gain that was needed to reduce the input current.

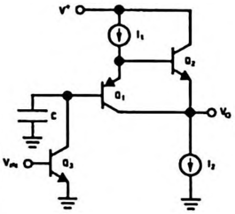


FIGURE 2. **Adding a PNP Transistor to the Basic Gain Stage**

Notice that the collector of this PNP transistor, Q_1, is connected directly to the output terminal. This "bootstraps" the output impedance of Q_1 and therefore reduces the loading at the high-impedance collector of the gain transistor, Q_3.

In addition, the collector-base junction of the PNP transistor becomes forward biased under a large-signal negative output voltage swing condition. The design of this device has allowed Q_1 to convert to a vertical PNP transistor during this operating mode which causes the output to change from the class A bias to a class B output stage. This allows the amplifier to sink more current than that provided by the current source, I_2, (1.3 mA) under large signal conditions.

1.2 Obtaining a Non-inverting Input Function

The circuit of Figure 2 has only the inverting input. A general purpose amplifier requires two input terminals to obtain both an inverting and a non-inverting input. In conventional op amp designs, an input differential amplifier provides these required inputs. The output voltage then depends upon the difference (or error) between the two input voltages. An input common-mode voltage range specification exists and, basically, input voltages are compared.

For circuit simplicity, and ease of application in single power supply systems, a non-inverting input can be provided by adding a standard IC "current-mirror" circuit directly across the inverting input terminal, as shown in Figure 3.

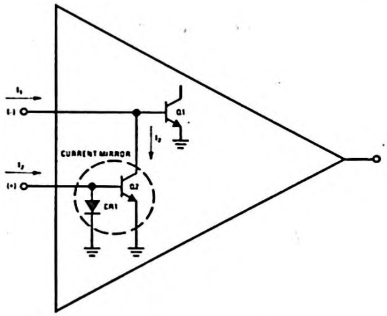


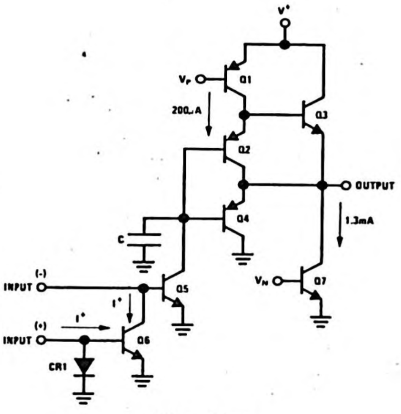
FIGURE 3. **Adding a Current Mirror to Achieve a Non-inverting Input**

This operates in the current mode as now input currents are compared or differenced (this can be thought of as a Norton differential amplifier). There is essentially no input common-mode voltage range directly at the input terminals (as both inputs will bias at one diode drop above ground) but if the input voltages are converted to currents (by use of input resistors), there is then no limit to the common-mode input voltage range. This is especially useful in high-voltage comparator applications. By making use of the input resistors, to convert input voltages to input currents, all of the standard op amp applications can be realized. Many additional applications are easily achieved, especially when operating with only a single power supply voltage. This results from the built-in voltage biasing that exists at both inputs (each input biases at + V_{BE}) and additional resistors are not required to provide a suitable common-mode input DC biasing voltage level. Further, input summing can be performed at the relatively low impedance level of the input diode of the current-mirror circuit.

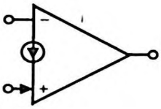
1.3 The Complete Single-supply Amplifier

The circuit schematic for a single amplifier stage is shown in Figure 4a). Due to the circuit simplicity, four of these amplifiers can be fabricated on a single chip. One common biasing circuit is used for all of the individual amplifiers.

A new symbol for this "Norton" amplifier is shown in Figure 4b). This is recommended to avoid using the standard op amp symbol as the basic operation is different. The current source symbol between the inputs implies this new current-mode of operation. In addition, it signifies that current is removed from the (–) input terminal. Also, the current arrow on the (+) input lead is used to indicate that this functions as a current input. The use of this symbol is helpful in understanding the operation of the application circuits and also in doing additional design work with the LM3900.



(a) Circuit Schematic



(b) New "NORTON" Amplifier Symbol

FIGURE 4. The Amplifier Stage

The bias reference for the PNP current source, V_p which biases Q_1, is designed to cause the upper current source (200 µA) to change with temperature to give first order compensation for the β variations of the NPN output transistor, Q_3. The bias reference for the NPN "pull-down" current sink, V_n, (which biases Q_7) is designed to stabilize this current (1.3 mA) to reduce the variation when the temperature is changed. This provides a more constant pull-down capability for the amplifier over the temperature range. The transistor, Q_4, provides the class B action which exists under large signal operating conditions.

The performance characteristics of each amplifier stage are summarized below:

Power-supply voltage range	4 to 36V_{DC} or ±2 to ±18 V_{DC}
Bias current drain per amplifier stage	1.3 mA_{DC}
Open loop:	
Voltage gain (R_L = 10k)	70 dB
Unity-gain frequency	2.5 MHz
Phase margin	40 degrees
Input resistance	1 MΩ
Output resistance	8 kΩ
Output voltage swing	(V_{cc} – 1) V_{pp}
Input bias current	30 nA_{DC}
Slew rate	0.5V/ µs

As the bias currents are all derived from diode forward voltage drops, there is only a small change in bias current magnitude as the power-supply voltage is varied. The open-loop gain changes only slightly over the complete power supply voltage range and is essentially independent of temperature changes. The open-loop frequency response is compared with the "741" op amp in Figure 5. The higher unity-gain crossover frequency is seen to provide an additional 10 dB of gain for all frequencies greater than 1 kHz.

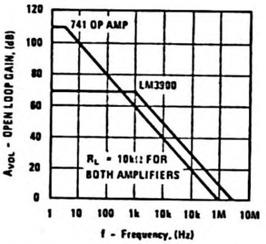


FIGURE 5. Open-loop Gain Characteristics

The complete schematic diagram of the LM3900 is shown in Figure 6. The one resistor, R_5, establishes the power consumption of the circuit as it controls the conduction of transistor Q_{28}. The emitter current of Q_{28} is used to bias the NPN output class-A biasing current sources and the collector current of Q_{28} is the reference for the PNP current source of each amplifier.

The biasing circuit is initially "started" by Q_{20}, Q_{30} and CR_6. After start-up is achieved, Q_{30} goes OFF and the current flow through the reference diodes: CR_5, CR_7 and CR_8, is dependent only on $V_{BE}/(R_6 + R_7)$. This guarantees that the power supply current drain is essentially independent of the magnitude of the power supply voltage.

The input clamp for negative voltages is provided by the multi-emitter NPN transistor Q_{21}.

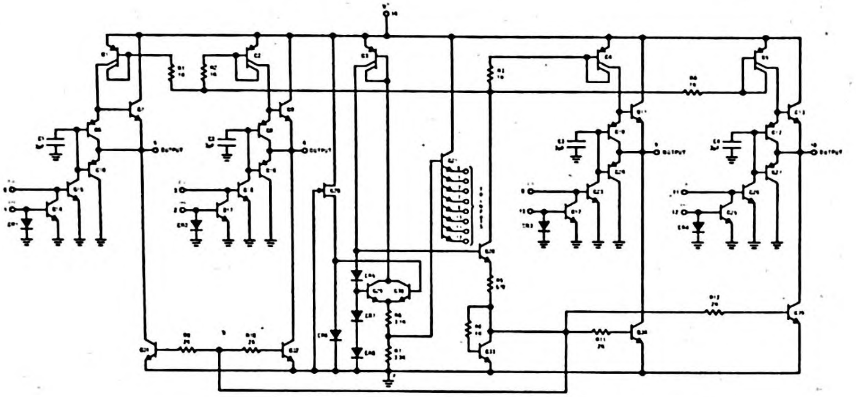


FIGURE 6. Schematic Diagram of the LM3900

One of the emitters of this transistor goes to each of the input terminals. The reference voltage for the base of Q_{21} is provided by R_6 and R_7 and is approximately $V_{BE}/2$.

2.0 INTRODUCTION TO APPLICATIONS OF THE LM3900

Like the standard IC op amp, the LM3900 has a wide range of applications. A new approach must be taken to design circuits with this "Norton" amplifier and the object of this note is to present a variety of useful circuits to indicate how conventional and unique new applications can be designed—especially when operating with only a single power supply voltage.

To understand the operation of the LM3900 we will compare it with the more familiar standard IC op amp. When operating on a single power supply voltage, the minimum input common-mode voltage range of a standard op amp limits the smallest value of voltage which can be applied to both inputs and still have the amplifier respond to a differential input signal. In addition, the output voltage will not swing completely from ground to the power supply voltage. The output voltage depends upon the difference between the input voltages and a bias current must be supplied to both inputs. A simplified diagram of a standard IC op amp operating from a single power supply is shown in Figure 7. The (+) and (−) inputs go only to current sources and therefore are free to be biased or operated at any voltage values which are within the input common-mode voltage range. The current sources at the input terminals, I_B^+ and I_B^-, represent the bias currents which must be supplied to both of the input transistors of the op amp (base currents). The output circuit is modeled as an active voltage source which depends upon the open-loop gain of the amplifier, A_V, and the difference which exists between the input voltages, $(V^+ - V^-)$.

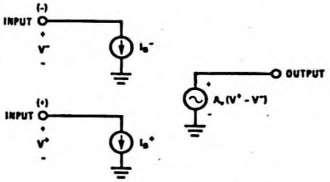


FIGURE 7. An Equivalent Circuit of a Standard IC Op Amp

An equivalent circuit for the "Norton" amplifier is shown in Figure 8. The (+) and (−) inputs are both clamped by diodes to force them to be one-diode drop above ground—always! They are not free to move and the "input common-mode voltage range" directly at these input terminals is very small—a few hundred mV centered about 0.5 V_{DC}. This is why external voltages must be first converted to currents (using resistors) before being applied to the inputs—and is the basis for the

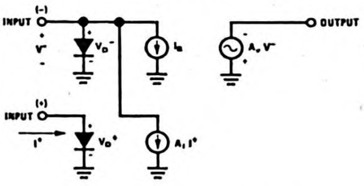


FIGURE 8. An Equivalent Circuit of the "Norton" Amplifier

current-mode (or Norton) type of operation. With external input resistors—there is *no limit* to the "input common-mode voltage range". The diode shown across the (+) input actually exists as a diode in the circuit and the diode across the (−) input is used to model the base-emitter junction of the transistor which exists at this input.

Only the (−) input must be supplied with a DC biasing current, I_B. The (+) input couples only to the (−) input and then to extract from this (−) input terminal the same current (A_I, the mirror gain, is approximately equal to 1) which is entered (by the external circuitry) into the (+) input terminal. This operation is described as a "current-mirror" as the current entering the (+) input is "mirrored" or "reflected" about ground and is then extracted from the (−) input. There is a maximum or near saturation value of current which the "mirror" at the (+) input can handle. This is listed on the data sheet as "maximum mirror current" and ranges from approximately 6 mA at 25°C to 3.8 mA at 70°C.

This fact that the (+) input current modulates or effects the (−) input current causes this amplifier to pass currents between the input terminals and is the basis for many new application circuits—especially when operating with only a single power supply voltage.

The output is modeled as an active voltage source which also depends upon the open-loop voltage gain, A_V, but only the (−) input voltage, V^-, (not the differential input voltage). Finally, the output voltage of the LM3900 can swing from essentially ground (+90 mV) to within one V_{BE} of the power supply voltage.

As an example of the use of the equivalent circuit of the LM3900, the AC coupled inverting amplifier of Figure 9a will be analyzed. Figure 9b shows the complete equivalent circuit which, for convenience, can be separated into a biasing equivalent circuit (Figure 10) and an AC equivalent circuit (Figure 11). From the biasing model of Figure 10 we find the output quiescent voltage, V_O, is:

$$V_O = V_D^- + (I_B + I^+)\, R_2\,, \qquad (1)$$

and

$$I^+ = \frac{V^+ - V_D^+}{R_3} \qquad (2)$$

where

$$V_D^+ \cong V_D^- \cong 0.5\, V_{DC}$$

I_B = INPUT bias current (30 nA)

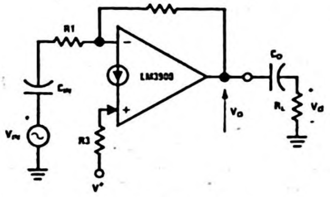
and

V^+ = Power supply voltage.

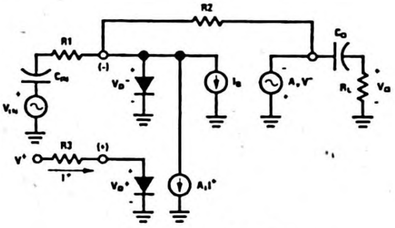
If (2) is substituted into (1)

$$V_O = V_D^- + \left(I_B + \frac{V^+ - V_D^+}{R_3}\right) R_2 \qquad (3)$$

which is an exact expression for V_O.



(a) A Typical Biased Amplifier



(b) Using the LM3900 Equivalent Circuit

FIGURE 9. Applying the LM3900 Equivalent Circuit

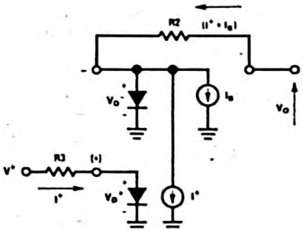


FIGURE 10. Biasing Equivalent Circuit

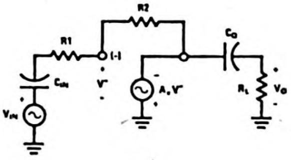


FIGURE 11. AC Equivalent Circuit

As the second term usually dominates ($V_O \gg V_D^-$) and $I^+ \gg I_B$ and $V^+ \gg V_D^+$ we can simplify (3) to provide a more useful design relationship

$$V_O \cong \frac{R_2}{R_3} V^+. \quad (4)$$

Using (4), if $R_3 = 2R_2$ we find

$$V_O \cong \frac{R_2}{2R_2} V^+ = \frac{V^+}{2}. \quad (5)$$

which shows that the output is easily biased to one-half of the power supply voltage by using V^+ as a biasing reference at the (+) input.

The AC equivalent circuit of Figure 11 is the same as that which would result if a standard IC op amp were used with the (+) input grounded. The closed-loop voltage gain $A_{V_{CL}}$, is given by:

$$A_{V_{CL}} \equiv \frac{V_O}{V_{IN}} \cong -\frac{R_2}{R_1} \quad (6)$$

If A_v (open-loop) $> \frac{R_2}{R_1}$.

The design procedure for an AC coupled inverting amplifier using the LM3900 is therefore to first select R_1, C_{IN}, R_2, and C_O as with a standard IC op amp and then to simply add $R_3 = 2R_2$ as a final biasing consideration. Other biasing techniques are presented in the following sections of this note. For the switching circuit applications, the biasing model of Figure 10 is adequate to predict circuit operation.

Although the LM3900 has four independent amplifiers, the use of the label "¼LM3900" will be shortened to simply "LM3900" for the application drawings contained in this note.

3.0 DESIGNING AC AMPLIFIERS

The LM3900 readily lends itself to use as an AC amplifier because the output can be biased to any desired DC level within the range of the output voltage swing and the AC gain is independent of the biasing network. In addition, the single power supply requirement makes the LM3900 attractive for any low frequency gain application. For lowest noise performance, the (+) input should be grounded (Figure 9a) and the output will then bias at $+V_{BE}$. Although the LM3900 is not suitable as an ultra low noise tape pre-amp, it is useful in most other applications. The restriction to only shunt feedback causes a small input impedance. Transducers which can be loaded can operate with this low input impedance. The noise degradation which would result from the use of a large input resistor limits the usefulness where low noise and high input impedance are both required.

3.1 Single Power Suply Biasing

The LM3900 can be biased in several different ways. The circuit in Figure 12 is a standard inverting AC amplifier which has been biased from the same power supply which is used to operate the amplifier. (The design of this amplifier has been presented in the previous section.) Notice that if AC ripple voltages are present on the V^+ power supply line they will couple to the output with a "gain" of 1/2. To eliminate this, one source of ripple filtered voltage can be provided and then used for many amplifiers. This is shown in the next section.

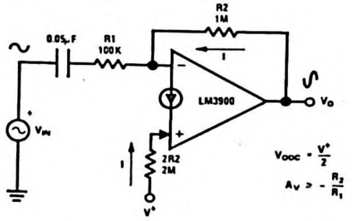


FIGURE 12. Inverting AC Amplifier Using Single-supply Biasing

3.2 A Non-inverting Amplifier

The amplifier in Figure 13 shows both a non-inverting AC amplifier and a second method for DC biasing. Once again the AC gain of the amplifier is set by the ratio of feedback resistor to input resistor. The small signal impedance of the diode at the (+) input should be added to the value of R_1 when calculating gain, as shown in Figure 13.

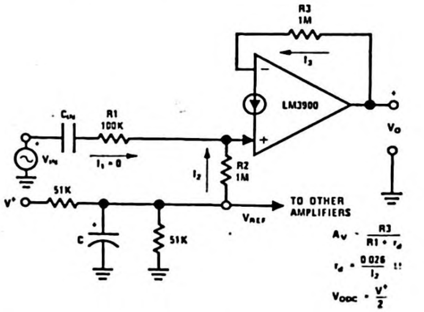


FIGURE 13. Non-inverting AC Amplifier Using Voltage Reference Biasing

By making $R_2 = R_3$, V_{ODC} will be equal to the reference voltage which is applied to the resistor R_2. The filtered $V^+/2$ reference shown can also be used for other amplifiers.

3.3 "N V_{BE}" Biasing

A third technique of output DC biasing is best described as the "N V_{BE}" method. This technique is shown in Figure 14 and is most useful with inverting AC amplifier applications. The input bias voltage (V_{BE}) at the inverting input establishes a current through resistor R_3 to ground. This current must come from the output of the amplifier. Therefore, V_O must rise to a level which will cause this current to flow through R_2. The bias voltage, V_O, may be calculated from the ratio of R_2 to R_3 as follows:

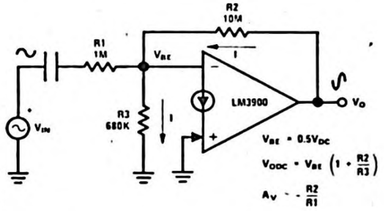

R2
10M
R1
1M
V_{BE}
I
LM3900
V_O
R3
680K
I
V_{IN}
$V_{BE} = 0.5V_{DC}$
$V_{ODC} = V_{BE}\left(1 + \frac{R2}{R3}\right)$
$A_V \approx -\frac{R2}{R1}$

FIGURE 14. Inverting AC Amplifier Using N V_{BE} Biasing

$$V_{ODC} = V_{BE}\left(1 + \frac{R_2}{R_3}\right)$$

When NV_{BE} biasing is employed, values for resistors R_1 and R_2 are first established and then resistor R_3 is added to provide the desired DC output voltage.

For a design example (Figure 14), a Z in = 1M and $A_v \cong 10$ are required.

Select R_1 = 1M.

Calculate $R_2 \cong A_vR_1$ = 10M.

To bias the output voltage at 7.5 V_{DC}, R_3 is found as:

$$R_3 = \frac{R_2}{\frac{V_O}{V_{BE}} - 1} = \frac{10M}{\frac{7.5}{0.5} - 1}$$

or

$$R_3 \cong 680\ k\Omega\ .$$

3.4 Biasing Using a Negative Supply

If a negative power supply is available, the circuit of Figure 15 can be used. The DC biasing current, I, is established by the negative supply voltage via R_3 and provides a very stable output quiescent point for the amplifier.

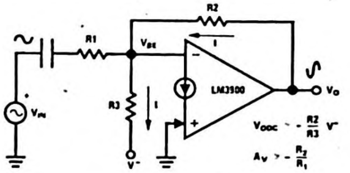

R2
I
R1
V_{BE}
LM3900
V_O
V_{IN}
R3
I
V^-
$V_{ODC} \approx -\frac{R2}{R3} V^-$
$A_V \approx -\frac{R_2}{R_1}$

FIGURE 15. Negative Supply Biasing

3.5 Obtaining High Input Impedance and High Gain

For the AC amplifiers which have been presented, a designer is able to obtain either high gain or high input impedance with very little difficulty. The application which requires both and still employs only one amplifier presents a new problem. This can be achieved by the use of a circuit similar to the one shown in Figure 16. When the A_v from the input to point A is unity ($R_1 = R_3$), the A_v of the complete stage will be set by the voltage divider network composed of R_4, R_5, and C_2. As the value of R_5 is decreased, the A_v of the stage will approach the AC open loop limit of the amplifier. The insertion of capacitor C_2 allows the DC bias to be controlled by the series combination of R_3 and R_4 with no effect from R_5. Therefore, R_2 may be selected to obtain the desired output DC biasing level using any of the methods which have been discussed. The circuit in Figure 16 has an input impedance of 1M and a gain of 100.

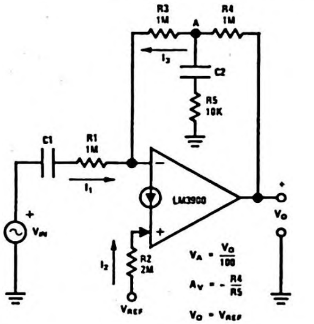


FIGURE 16. A High Z_{IN} High Gain Inverting AC Amplifier

3.6 An Amplifier with a DC Gain Control

A DC gain control can be added to an amplifier as shown in Figure 17. The output of the amplifier is kept from being driven to saturation as the DC gain control is varied by providing a minimum biasing current via R_3. For

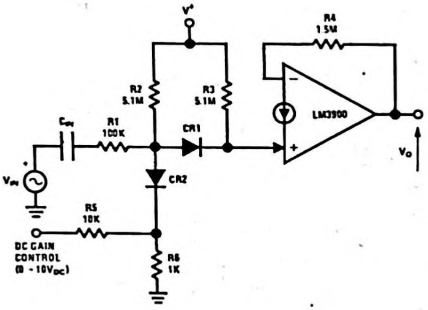


FIGURE 17. An Amplifier with a DC Gain Control

maximum gain, CR_2 is OFF and both the current through R_2 and R_3 enter the (+) input and cause the output of the amplifier to bias at approximately 0.6 V^+. For minimum gain, CR_2 is ON and only the current through R_3 enters the (+) input to bias the output at approximately 0.3 V^+. The proper output bias for large output signal accomodation is provided for the maximum gain situation. The DC gain control input ranges from $0V_{DC}$ for minimum gain to less than $10V_{DC}$ for maximum gain.

3.7 A Line-receiver Amplifier

A line-receiver amplifier is shown in Figure 18. The use of both inputs cancels out common-mode signals. The line is terminated by R_{LINE} and the larger input impedance of the amplifier will not effect this matched loading.

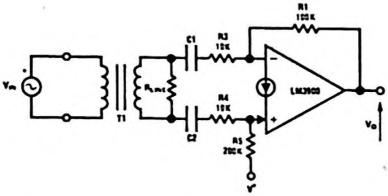


FIGURE 18. A Line-receiver Amplifier

4.0 DESIGNING DC AMPLIFIERS

The design of DC amplifiers using the LM3900 tends to be more difficult than the design of AC amplifiers. These difficulties occur when designing a DC amplifier which will operate from only a single power supply voltage and yet provide an output voltage which goes to zero volts DC and also will accept input voltages of zero volts DC. To accomplish this, the inputs must be biased into the linear region ($+V_{BE}$) with DC input signals of zero volts and the output must be modified if operation to actual ground (and not V_{SAT}) is required. Therefore, the problem becomes one of determining what type of network is necessary to provide an output voltage (V_O) equal to zero when the input voltage (V_{IN}) is equal to zero. (See also section 10.16, "adding a Differential Input Stage").

We will start with a careful evaluation of what actually takes place at the amplifier inputs. The mirror circuit demands that the current flowing into the positive input (+) be equaled by a current flowing into the negative input (-). The difference between the current demanded and the current provided by an external source must flow in the feedback circuit. The output voltage is then forced to seek the level required to cause this amount of current to flow. If, in the steady state condition $V_O = V_{IN} = 0$, the amplifier will operate in the desired manner. This condition can be established by the use of common-mode biasing at the inputs.

4.1 Using Common-mode Biasing for V_{IN} = 0 V_{DC}

Common-mode biasing is achieved by placing equal resistors between the amplifier input terminals and the supply voltage (V^+), as shown in Figure 19. When V_{IN} is set to 0 volts the circuit can be modeled as shown in Figure 20, where:

$$R_{EQ_1} = R_1 \parallel R_5 ,$$

$$R_{EQ_2} = R_2 \parallel R_6 ,$$

and

$$R_3 = R_4 .$$

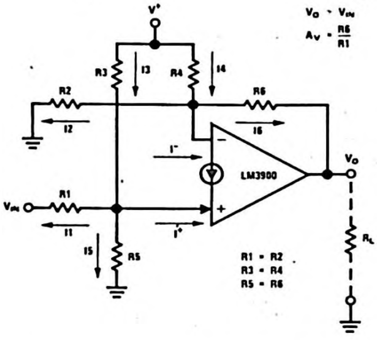


FIGURE 19. A DC Amplifier Employing Common-mode Biasing

Because the current mirror demands that the two current sources be equal, the current in the two equivalent resistors must be identical.

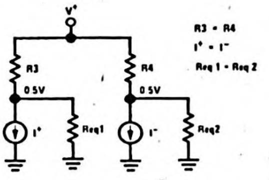

V+
R3 = R4
I+ = I−
Req 1 = Req 2
R3
R4
0.5V
0.5V
I+
Req1
I−
Req2

FIGURE 20. An Ideal Circuit Model of a DC Amplifier with Zero Input Voltage

If this is true, both R_2 and R_6 must have a voltage drop of 0.5 volt across them, which forces V_O to go to $V_{O\,MIN}$ (V_{SAT}).

4.2 Adding an Output Diode for V_O = 0 V_{DC}

For many applications a $V_{O\,MIN}$ of 100 mV may not be acceptable. To overcome this problem a diode can be added between the output of the amplifier and the output terminal (Figure 21).

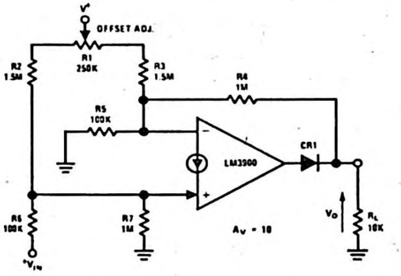

V+
OFFSET ADJ.
R1
250K
R2
1.5M
R3
1.5M
R4
1M
R5
100K
LM3900
CR1
R6
100K
R7
1M
Av = 10
VO
RL
10K
+VIN

FIGURE 21. A Non-inverting DC Amplifier with Zero Volts Output for Zero Volts Input

The function of the diode is to provide a DC level shift which will allow V_O to go to ground. With a load impedance (R_L) connected, V_O becomes a function of the voltage divider formed by the series connection of R_4 and R_L.

If $R_4 = 100 R_L$, then $V_{O\,MIN} = \frac{0.5 R_L}{101 R_l}$,

or $V_{O\,MIN} \cong 5\ mV_{DC}$.

An offset voltage adjustment can be added as shown (R_1) to adjust V_O to $0V_{DC}$ with V_{IN} = 0 V_{DC}.

The voltage transfer functions for the circuit in Figure 21, both with and without the diode, are shown in Figure 22. While the diode greatly improves the operation around 0 volts, the voltage drop across the diode will reduce the peak output voltage swing of the stage by approximately 0.5 volt.

When using a DC amplifier similar to the one in Figure 21, the load impedance should be large enough to avoid excessively loading the amplifier. The value of R_L may be significantly reduced by replacing the diode with an NPN transistor.

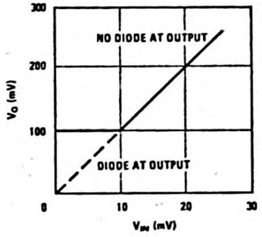


FIGURE 22. Voltage Transfer Function for a DC Amplifier with a Voltage Gain of 10

4.3 A DC Coupled Power Amplifier ($I_L \leq$ 3 Amps)

The LM3900 may be used as a power amplifier by the addition of a Darlington pair at the output. The circuit shown in Figure 23 can deliver in excess of 3 amps to the load when the transistors are properly mounted on heat sinks.

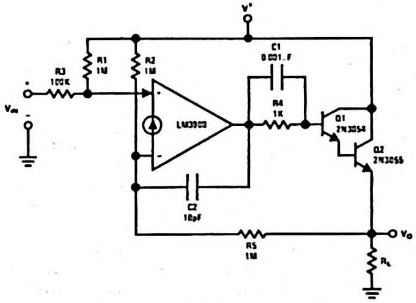

V+
R1
1M
R2
1M
C1
0.001 µF
R3
100K
VIN
+
−
LM3900
R4
1K
Q1
2N3054
Q2
2N3055
C2
10pF
R5
1M
VO
RL

FIGURE 23. A DC Power Amplifier

4.4 Ground Referencing a Differential Voltage

The circuit in Figure 24 employs the LM3900 to ground reference a DC differential input voltage. Current I_1 is larger than current I_3 by a

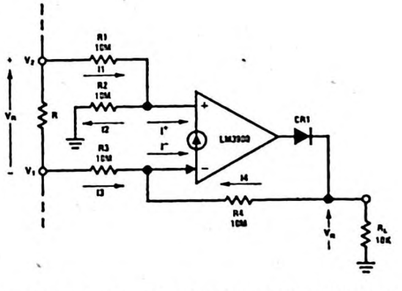

R1
10M
I1
R2
10M
I2
R3
10M
I3
V2
V1
+
−
VIN
R
I+
I−
LM3900
CR1
I4
R4
10M
VO
RL
10K

FIGURE 24. Ground Referencing a Differential Input DC Voltage

factor proportional to the differential voltage, V_R. The currents labeled on Figure 24 are given by:

$$I_1 = \frac{V_1 + V_R - \phi}{R_1}$$

$$I_2 = \phi / R_2$$

$$I_3 = \frac{(V_1 - \phi)}{R_3}$$

and

$$I_4 = \frac{V_O - \phi}{R_4}$$

where

$\phi \equiv V_{BE}$ at either input terminal of the LM3900.

Since the input current mirror demands that

$$I^- = I^+;$$

and

$$I^+ = I_1 - I_2$$

and

$$I^- = I_3 + I_4$$

Therefore

$$I_4 = I_1 - I_2 - I_3 .$$

Substituting in from the above equation

$$\frac{V_O - \phi}{R_4} = \frac{(V_1 + V_R - \phi)}{R_1} - \frac{(\phi)}{R_2} - \frac{(V_1 - \phi)}{R_3}$$

and as $R_1 = R_2 = R_3 = R_4$

$$V_O = (V_1 + V_R - \phi) - (\phi) - V_1 + \phi + \phi$$

or

$$V_O = V_R .$$

The resistors are kept large to minimize loading. With the 10 MΩ resistors which are shown on the figure, an error exists at small values of V_1 due to the input bias current at the (-) input. For simplicity this has been neglected in the circuit description. Smaller R values reduce the percentage error or the bias current can be supplied by an additional amplifier (see Section 10.7.1).

For proper operation, the differential input voltage must be limited to be within the output dynamic voltage range of the amplifier and the input voltage V_2 must be greater than 1 volt. For example; if V_2 = 1 volt, the input voltage V_1 may vary over the range of 1 volt to −13 volts when operating from a 15 volt supply. Common-mode biasing may be added as shown in Figure 25 to allow both V_1 and V_2 to be negative.

4.5 A Unity Gain Buffer Amplifier

The buffer amplifier with a gain of one is the simplest DC application for the LM3900. The voltage applied to the input (Figure 26) will be reproduced at the output. However, the input voltage must be greater than one V_{BE} but less than the maximum output swing. Common-mode biasing can be added to extend V_{IN} to 0 V_{DC}, if desired.

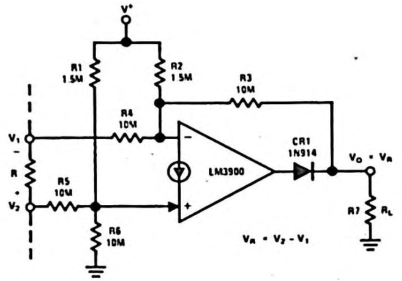


FIGURE 25. A Network to Invert and to Ground Reference a Negative DC Differential Input Voltage

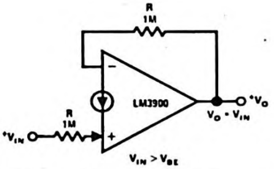
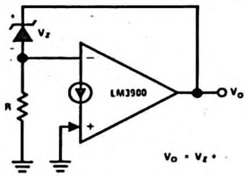


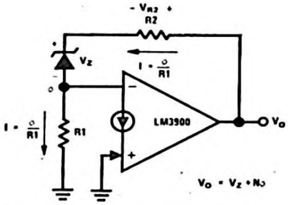
FIGURE 26. A Unity-gain DC Buffer Amplifier

5.0 DESIGNING VOLTAGE REGULATORS

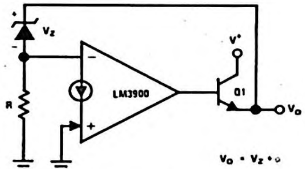
Many voltage regulators can be designed which make use of the basic amplifier of the LM3900. The simplest is shown in Figure 27a where only a Zener diode and a resistor are added. The voltage at the (-) input (one $V_{BE} \cong 0.5\ V_{DC}$) appears across R and therefore a resistor value of 510Ω will cause approximately 1 mA of bias current to be drawn through the Zener. This biasing is used to reduce the noise output of the Zener as the 30 nA input current is too small for proper Zener biasing. To compensate for a positive temperature coefficient of the Zener, an additional resistor can be added, R_2, (Figure 27b) to introduce an arbitrary number, N, of "effective" V_{BE} drops into the expression for the output voltage. The negative temperature coefficient of these diodes will also be added to temperature compensate the DC output voltage. For a larger output current, an emitter follower (Q_1 of Figure 27c) can be added. This will multiply the 10 mA (max.) output current of the LM3900 by the β of the added transistor. For example, a β = 30 will provide a max. load current of 300 mA. This added transistor also reduces the output impedance. An output frequency compensation capacitor is generally not required but may be added, if desired, to reduce the output impedance at high frequencies.



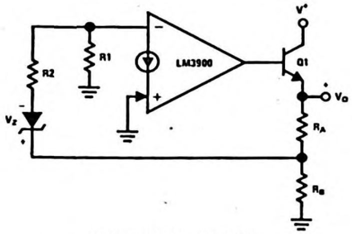
(a) Basic Circuit



(b) Temperature Compensating



(c) Current Boosting



(d) Raising V_O Without Disturbing Temperature Compensation

FIGURE 27. Simple Voltage Regulators

The DC output voltage can be increased and still preserve the temperature compensation of Figure 27b by adding resistors R_A and R_B as shown in Figure 27d. This also can be accomplished without the added transistor, Q_1. The unregulated input voltage, which is applied to pin 14 of the LM3900 (and to the collector of Q_1, if used) must always exceed the regulated DC output voltage by approximately 1V, when the unit is not current boosted or approximately 2V when the NPN current boosting transistor is added.

5.1 Reducing the Input-output Voltage

The use of an external PNP transistor will reduce the required (V_{IN} - V_{OUT}) to a few tenths of a volt. This will depend on the saturation characteristics of the external transistor at the operating current level. The circuit, shown in Figure 28, uses the LM3900 to supply base drive to the PNP transistor. The resistors R_1 and R_2 are used to allow the output of the amplifier to turn OFF the PNP transistor. It is important that pin 14 of the LM3900 be tied to the $+V_{IN}$ line to allow this OFF control to properly operate. Larger voltages are permissable (if the base-emitter junction of Q_1 is prevented from entering a breakdown by a shunting diode, for example), but smaller voltages will not allow the output of the amplifier to raise enough to give the OFF control.

The resistor, R_3, is used to supply the required bias current for the amplifier and R_4 is again used to bias the Zener diode. Due to a larger gain, a compensation capacitor, C_O, is required. Temperature compensation could be added as was shown in Figure 27b.

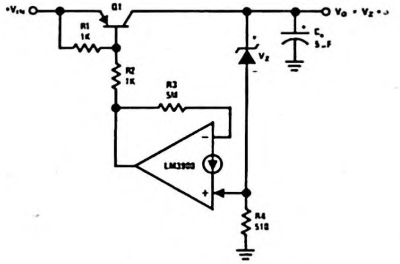


FIGURE 28. Reducing (V_{IN} – V_{OUT})

5.2 Providing High Input Voltage Protection

One of the four amplifiers can be used to regulate the supply line for the complete package (pin 14), to provide protection against large input voltage conditions, and in addition, to supply current to an external load. This circuit is shown in Figure 29. The regulated output voltage is the sum of the Zener voltage, CR_2, and the V_{BE} of the inverting input terminal. Again, temperature compensation can be added as in Figure 27b. The second Zener, CR_1, is a low tolerance component which simply serves as a DC level shift to allow the output voltage of the amplifier to control the conduction of the external transistor, Q_1. This Zener voltage should be approximately one-half of the CR_2 voltage to position the DC output voltage level of the amplifier approximately in the center of the dynamic range.

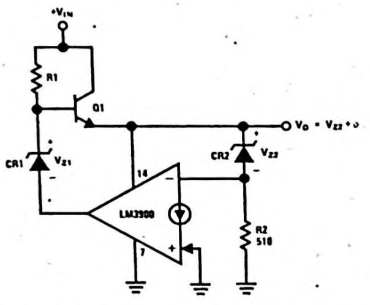


FIGURE 29. High V_{IN} Protection and Self-regulation

The base drive current for Q_1 is supplied via R_1. The maximum current through R_1 should be limited to 10 mA as

$$I_{MAX} = \frac{V_{IN\,(MAX)} - (V_O + V_{BE})}{R_1}$$

To increase the maximum allowed input voltage, reduce the output ripple, or to reduce the $(V_{IN} - V_{OUT})$ requirements of this circuit, the connection described in the next section is recommended.

5.3 High Input Voltage Protection and Low $(V_{IN} - V_{OUT})$

The circuit shown in Figure 30 basically adds one additional transistor to the circuit of Figure 29 to improve the performance. In this circuit both transistors (Q_1 and Q_2) absorb any high input voltages (and therefore need to be high voltage devices) without any increases in current (as with R_1 of Figure 29). The resistor R_1 (of Figure 30) provides a "start-up" current into the base of Q_2.

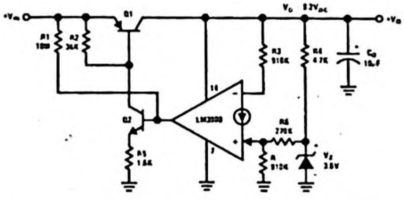


FIGURE 30. A High V_{IN} Protected, Low (V_{IN} − V_{OUT}) Regulator

A new input connection is shown on this regulator (the type on Figure 29 could also be used) to control the DC output voltage. The Zener is biased via R_4 (at approximately 1 mA). The resistors R_3 and R_6 provide gain (non-inverting) to allow establishing V_O at any desired voltage larger than V_Z. Temperature compensation of either sign (±TC) can be obtained by shunting a resistor from either the (+) input to ground (to add + TC to V_O) or from the (-) input to ground (to add − TC to V_O). To understand this, notice that the resistor, R, from the (+) input to ground will add $-N\ V_{BE}$ to V_O where

$$N = 1 + \frac{R_3}{R},$$

and V_{BE} is the base emitter voltage of the transistor at the (+) input. This then also adds a positive temperature change at the output to provide the desired temperature correction.

The added transistor, Q_2, also increases the gain (which reduces the output impedance) and if a power device is used for Q_1 large load currents (amps) can be supplied. This regulator also supplies the power to the other three amplifiers of the LM3900.

5.4 Reducing Input Voltage Dependence and Adding Short-circuit Protection

To reduce ripple feedthrough and input voltage dependence, diodes can be added as shown in Figure 31 to drop-out the start circuit once start-up has been achieved. Short-circuit protection can also be added as shown in Figure 32.

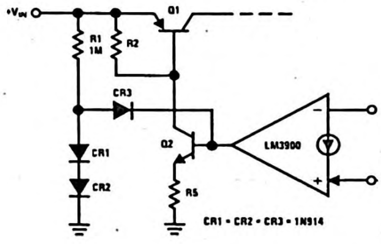


FIGURE 31. Reducing V_{IN} Dependence

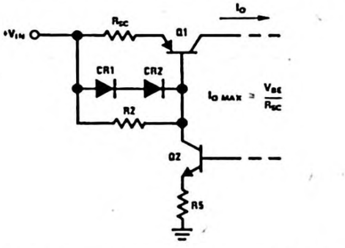


FIGURE 32. Adding Short-circuit Current Limiting

The emitter resistor of Q_2 will limit the maximum current of Q_2 to $(V_O - 2\ V_{BE})/R_5$.

6.0 DESIGNING RC ACTIVE FILTERS

Recent work in RC active filters has shown that the performance characteristics of multiple-amplifier filters are relatively insensitive to the tolerance of the RC components used. This makes the performance of these filters easier to control in production runs. In many cases where gain is needed in a system design it is now relatively easy to also get frequency selectivity.

The basis of active filters is a gain stage and therefore a multiple amplifier product is a valuable addition to this application area. When additional amplifiers are available, less component selection and trimming is needed as the performance of the filter is less disturbed by the tolerance and temperature drifts of the passive components.

The *passive components* do *control* the *performance* of the filter and for this reason carbon composition resistors are useful mainly for room temperature breadboarding or for final trimming of the more stable metal film or wirewound resistors. Capacitors present more of a problem in range of values available, tolerance and stability (with temperature, frequency, voltage and time). For example, the disk ceramic type of capacitors are generally not suited to active filter applications due to their relatively poor performance.

The impedance level of the passive components can be scaled without (theoretically) affecting the filter characteristics. In an actual circuit; if the resistor values become too small ($\leq$10 kΩ) an excessive loading may be placed on the output of the amplifier which will reduce gain or actually exceed either the output current or the package dissipation capabilities of the amplifier. This can easily be checked by calculating (or noticing) the impedance which is presented to the output terminal of the amplifier at the highest operating frequency. A second limit sets the upper range of impedance levels, this is due to the DC bias currents ($\cong$30 nA) and the input impedance of actual amplifiers. The solution to this problem is to reduce the impedance levels of the passive components ($\leq$10 MΩ). In general, better performance is obtained with relatively low passive component impedance levels and in filters which do not demand high gain, high Q ($Q \geq 50$) and high frequency (f_o >1 kHz) simultaneously.

A measure of the effects of changes in the values of the passive components on the filter performance has been given by "sensitivity functions". These assume infinite amplifier gain and relate the percentage change in a parameter of the filter, such as center frequency (f_o), Q, or gain to a percentage change in a particular passive component. Sensitivity functions which are small are desirable (as 1 or 1/2). Negative signs simply mean an increase in the value of a passive component causes a decrease in that filter performance characteristic. As an example, if a bandpass filter listed the following sensitivity factor

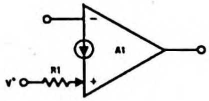
$$S_{C_3}^{\omega_o} = -\frac{1}{2}.$$

This states that "if C_3 were to increase by 1%, the center frequency, ω_o, would decrease by 0.5%." Sensitivity functions are tabulated in the reference listed at the end of this section and will therefore not be included here.

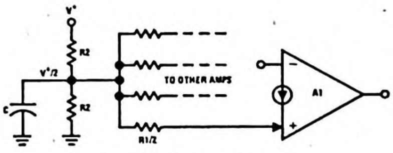
A brief look at low pass, high pass and bandpass filters will indicate how the LM3900 can be applied in these areas. A recommended text (which provided these circuits) is, "Operational Amplifiers", Tobey, Graeme, and Huelsman, McGraw Hill, 1971.

6.1 Biasing the Amplifiers

Active filters can be easily operated off of a single power supply when using these multiple single supply amplifiers. The general technique is to use the (+) input to accomplish the biasing function. The power supply voltage, V^+, is used as the DC reference to bias the output voltage of each amplifier at approximately $V^+/2$. As shown in Figure 33, undesired AC components on the power supply line may have to be removed (by a filter capacitor, Figure 31b) to keep the filter output free of this noise. One filtered DC reference can generally be used for all of the amplifiers as there is essentially no signal feedback to this bias point.



(a) Biasing From a "Noise Free" Power Supply



(b) Biasing From a "Noisy" Power Supply

FIGURE 33. Biasing Considerations

In the filter circuits presented here, all amplifiers will be biased at $V^+/2$ to allow the maximum AC voltage swing for any given DC power supply voltage. The inputs to these filters will also be assumed at a DC level of $V^+/2$ (for those which are direct coupled).

6.2 A High Pass Active Filter

A single amplifier high pass RC active filter is shown in Figure 34. This circuit is easily biased using the (+) input of the LM3900. The resistor, R_3, can be simply made equal to R_2 and a bias reference of $V^+/2$ will establish the output Q point at this value ($V^+/2$). The input is capacitively coupled (C_1) and there are therefore no further DC biasing problems.

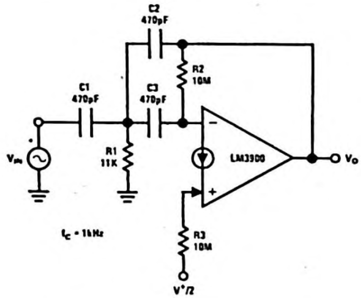


FIGURE 34. A High Pass Active Filter

The design procedure for this filter is to select the pass band gain, H_O, the Q and the corner frequency, f_c. A Q value of 1 gives only a slight peaking near the bandedge (<2 dB) and smaller Q values decrease this peaking. The slope of the skirt of this filter is 12 dB/octave (or 40 dB/decade). If the gain, H_O, is unity all capacitors have the same value. The design proceeds as:

Given: H_O, Q and $\omega_c = 2\pi f_c$

To find: R_1, R_2, C_1, C_2, and C_3

let $C_1 = C_3$ and choose a convenient starting value.

Then:

$$R_1 = \frac{1}{Q\,\omega_c C_1 (2H_O + 1)} \quad (1)$$

$$R_2 = \frac{Q}{\omega_c C_1}(2H_O + 1), \quad (2)$$

and

$$C_2 = \frac{C_1}{H_O} \quad (3)$$

As a design example,

Require: $H_O = 1$,

$Q = 10$,

and $f_c = 1\text{ kHz}$ ($\omega_c = 6.28 \times 10^3$ rps).

Start by selecting C_1 = 300 pF and then from equation (1)

$$R_1 = \frac{1}{(10)(6.28 \times 10^3)(3 \times 10^{-10})(3)}$$

$$R_1 = 17.7\text{ k}\Omega$$

and from equation (2)

$$R_2 = \frac{10 \quad (3)}{(6.28 \times 10^3)(3 \times 10^{-10})}$$

$$R_2 = 15.9\text{ M}\Omega$$

and from equation (3)

$$C_2 = \frac{C_1}{1} = C_1$$

Now we see that the value of R_2 is quite large; but the other components look acceptable. Here is where impedance scaling comes in. We can reduce R_2 to the more convenient value of 10 MΩ which is a factor of 1.59:1. Reducing R_1 by this same scaling factor gives:

$$R_{1_{NEW}} = \frac{17.7 \times 10^3}{1.59} = 11.1\text{ k}\Omega$$

and the capacitors are similarly reduced in impedance as:

$$\left(C_1 = C_2 = C_3\right)_{NEW} = (1.59)(300)\text{ pF}$$

$$C_{1_{NEW}} = 477\text{ pF}.$$

To complete the design, R_3 is made equal to R_2 (10 MΩ) and a V_{REF} of $V^+/2$ is used to bias the output for large signal accomodation.

Capacitor values should be adjusted to use standard valued components by using impedance scaling as a wider range of standard resistor values is generally available.

6.3 A Low Pass Active Filter

A single amplifier low pass filter is shown in Figure 35. The resistor, R_4, is used to set the output bias level and is selected after the other resistors have been established.

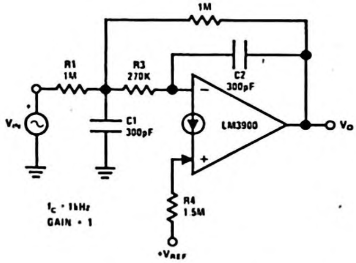


FIGURE 35. A Low Pass Active Filter

The design procedure is as follows:

Given: H_O, Q, and $\omega_c = 2\pi f_c$

To find: R_1, R_2, R_3, R_4, C_1, and C_2

Let C_1 be a convenient value,

then

$$C_2 = KC_1 \qquad (4)$$

where K is a constant which can be used to adjust component values. For example, with $K = 1$, $C_1 = C_2$. Larger values of K can be used to reduce R_2 and R_3 at the expense of a larger value for C_2.

$$R_1 = \frac{R_2}{H_O}, \qquad (5)$$

$$R_2 = \frac{1}{2Q\,\omega_c\,C_1}\left[1 \pm \sqrt{1 + \frac{4Q^2(H_O + 1)}{K}}\right] \qquad (6)$$

and

$$R_3 = \frac{1}{\omega_c^2 C_1^2 R_2(K)} \qquad (7)$$

As a design example;

Require: $H_O = 1$,
$Q = 1$,

and $f_c = 1$ kHz ($\omega_c = 6.28 \times 10^3$ rps).

Start by selecting $C_1 = 300$ pF and $K = 1$ so C_2 is also 300 pF (equation 4).

Now from equation (6)

$$R_2 = \frac{1}{2(1)\,(6.28 \times 10^3)\,(3 \times 10^{-10})}\left[1 \pm \sqrt{1 + 4\,(2)}\right]$$

$$R_2 = 1.06\ \text{M}\Omega$$

Then from equation (5)

$$R_1 = R_2 = 1.06\ \text{M}\Omega$$

and finally from equation (7)

$$R_3 = \frac{1}{(6.28 \times 10^3)^2\,(3 \times 10^{-10})^2\,(1.06 \times 10^6)\,(1)}$$

$$R_3 = 266\ \text{k}\Omega.$$

To select R_4, we assume the DC input level is 7 V_{DC} and the DC output of this filter is to also be 7 V_{DC}. This gives us the circuit of Figure 36. Notice that $H_O = 1$ gives us not only equal resistor values (R_1 and R_2) but simplifies the DC bias calculation as $I_1 = I_2$ and we have a DC amplifier with a gain of −1 (so if the DC input voltage increases 1 V_{DC} the output voltage decreases 1 V_{DC}). The resistors R_1 and R_2 are in parallel so that the circuit simplifies to that shown in Figure 37 where the actual resistance values have been added. The resistor R_4 is given by

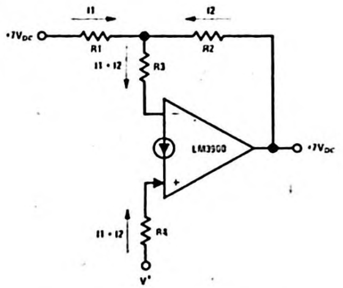


FIGURE 36. Biasing the Low Pass Filter

$$R_4 = 2\left(\frac{R_1}{2} + R_3\right) + R_3$$

or, using values

$$R_4 = 2\left(\frac{1\text{M}\Omega}{2} + 266\text{ k}\right) \cong 1.5\ \text{M}\Omega$$

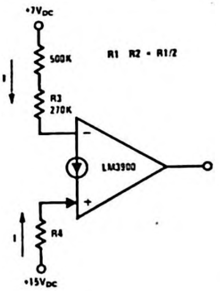


FIGURE 37. Biasing Equivalent Circuit

6.4 A Single-amplifier Bandpass Active Filter

The bandpass filter is perhaps the most interesting. For low frequencies, low gain and low Q (≤10) requirements, a single amplifier realization can be used. A one amplifier circuit is shown in Figure 38 and the design procedure is as follows:

Given: H_O, Q and $\omega_o = 2\pi f$.

To find: R_1, R_2, R_3, R_4, C_1 and C_2.

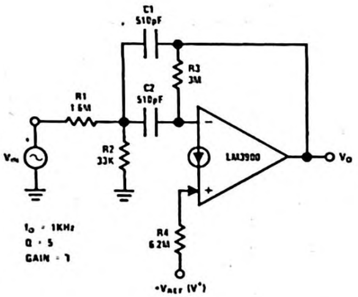


FIGURE 38. A One Op Amp Bandpass Filter

Let $C_1 = C_2$ and select a convenient starting value.

Then

$$R_1 = \frac{Q}{H_O \omega_o C_1}, \tag{8}$$

$$R_2 = \frac{Q}{(2Q^2 - H_O)\,\omega_o C_1} \tag{9}$$

$$R_3 = \frac{2Q}{\omega_o C_1}, \tag{10}$$

and

$$R_4 = 2R_3 \text{ (for } V_{REF} = V^+) \tag{11}$$

As a design example;

Require: $H_O = 1$
$Q = 5$
$f_o = 1 \text{ kHz } (\omega_o = 6.28 \times 10^3 \text{ rps})$.

Start by selecting

$$C_1 = C_2 = 510 \text{ pF}.$$

Then using equation (8)

$$R_1 = \frac{5}{(6.28 \times 10^3)(5.1 \times 10^{-10})}$$

$$R_1 = 1.57 \text{ M}\Omega,$$

and using equation (9)

$$R_2 = \frac{5}{[2(25) - 1](6.28 \times 10^3)(5.1 \times 10^{-10})}$$

$$R_2 = 32 \text{ k}\Omega$$

from equation (10)

$$R_3 = \frac{2(5)}{(6.28 \times 10^3)(5.1 \times 10^{-10})}$$

$$R_3 = 3.13 \text{ M}\Omega,$$

and finally, for biasing, using equation (11)

$$R_4 = 6.2 \text{ M}\Omega.$$

6.5 A Two-amplifier Bandpass Active Filter

To allow higher Q (between 10 and 50) and higher gain, a two amplifier filter is required. This circuit, shown in Figure 39, uses only two capacitors. It is similar to the previous single amplifier bandpass circuit and the added amplifier supplies a controlled amount of positive feedback to improve the response characteristics. The resistors R_5 and R_8 are used to bias the output voltage of the amplifiers at $V^+/2$.

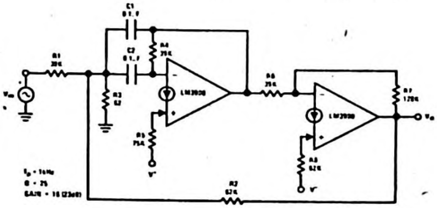


FIGURE 39. A Two Op Amp Bandpass Filter

Again, R_5 is simply chosen as twice R_4 and R_8 must be selected after R_6 and R_7 have been assigned values. The design procedure is as follows:

Given: Q and f_o

To find: R_1 through R_7, and C_1 and C_2

Let: $C_1 = C_2$ and choose a convenient starting value and choose a value for K to reduce the spread of element values or to optimize sensitivity ($1 \leq K_{Typically} \leq 10$).

Then

$$R_1 = R_4 = R_6 = \frac{Q}{\omega_o C_1} \tag{12}$$

$$R_2 = R_1 \frac{KQ}{(2Q - 1)} \tag{13}$$

$$R_3 = \frac{R_1}{Q^2 - 1 - 2/K + 1/KQ} \tag{14}$$

and

$$R_7 = KR_1 \tag{15}$$

$$H_O = \sqrt{Q}\; K. \tag{16}$$

As a design example:

Require: $Q = 25$ and $f_o = 1$ kHz.

Select: $C_1 = C_2 = 0.1\,\mu F$

and $K = 3$.

Then from equation (12)

$$R_1 = R_4 = R_6 = \frac{25}{(2\pi \times 10^3)(10^{-7})}$$

$$R_1 = 40\,k\Omega$$

and from equation (13)

$$R_2 = (40 \times 10^3)\,\frac{3(25)}{[2(25) - 1]}$$

$$R_2 = 61\,k\Omega$$

and from equation (14)

$$R_3 = \frac{40 \times 10^3}{(25)^2 - 1 - 2/3 + \dfrac{1}{3(25)}}$$

$$R_3 = 64\,\Omega$$

And R_7 is given by equation (15)

$$R_7 = 3\,(40\ \ k\Omega) = 120\,k\Omega,$$

and the gain is obtained from equation (16)

$$H_O = \sqrt{25}\,(3) = 15\,(23\,dB).$$

To properly bias the first amplifier

$$R_5 = 2R_4 = 80\,k\Omega$$

and the second amplifier is biased by R_8. Notice that the outputs of both amplifiers will be at $V^+/2$. Therefore R_6 and R_7 can be paralleled and

$$R_8 = 2(R_6 \parallel R_7)$$

or

$$R_8 = 2\left[\frac{(40)\,(120) \times 10^3}{160}\right] = 59\,k\Omega$$

These values, to the closest standard resistor values, have been added to Figure 39.

6.6 A Three-amplifier Bandpass Active Filter

To reduce Q sensitivity to element variation even further or to provide higher Q (Q > 50) a three amplifier bandpass filter can be used. This circuit, Figure 40, pre-dates most of the literature on RC active filters and has been used on analog computers. Due to the use of three amplifiers it often is considered too costly—especially for low Q applications. The multiple amplifiers of the LM3900 make this a very useful circuit. It has been called the "Bi-Quad" as it can produce a transfer function which is "Quad" — radic in both numerator and denominator (to give the "Bi"). A newer realization technique for this type of filter is the "second-degree state-variable network." Outputs can be taken at any of three points to give low pass, high pass or bandpass response characteristics (see the reference cited).

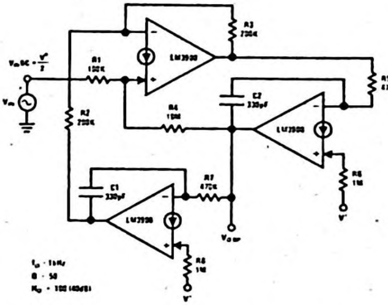


FIGURE 40. The "Bi-quad" RC Active Bandpass Filter

The bandpass filter is shown in Figure 40 and the design procedure is:

Given: Q and f_o.

To simplify: Let $C_1 = C_2$ and choose a convenient starting value and also let $2R_1 = R_2 = R_3$ and choose a convenient starting value.

Then:

$$R_4 = R_1\,(2Q - 1), \tag{17}$$

$$R_5 = R_7 = \frac{1}{\omega_o C_1}, \tag{18}$$

and for biasing the amplifiers we require

$$R_6 = R_8 = 2R_5. \tag{19}$$

The mid-band gain is:

$$H_O = \frac{R_4}{R_1}. \tag{20}$$

As a design example;

Require: $f_o = 1\,kHz$ and $Q = 50$.

To find: C_1, C_2 and R_1 through R_8.

Choose: $C_1 = C_2 = 330\,pF$

and $2R_1 = R_2 = R_3 = 360\,k\Omega$, and $R_1 = 180\,k\Omega$.

Then from equation (17),

$$R_4 = (1.8 \times 10^5)\,[2(50) - 1]$$

$$R_4 = 17.8\,M\Omega.$$

From equation (18),

$$R_5 = R_7 = \frac{1}{(2\pi \times 10^3)\,(3.3 \times 10^{-10})}$$

$$R_5 = 483\,k\Omega.$$

And from equation (19),

$$R_6 = R_8 \cong 1\,M\Omega.$$

From equation (20) the midband gain is 100 (40 dB). The value of R_4 is high and can be lowered by scaling only R_1 through R_4 by the factor 1.78 to give:

$$2R_1 = R_2 = R_3 = \frac{360 \times 10^3}{1.78} = 200\ \text{k}\Omega,\ R_1 = 100\ \text{k}\Omega$$

and

$$R_4 = \frac{17.8 \times 10^6}{1.78} = 10\ \text{M}\Omega.$$

These values (to the nearest 5% standard) have been added to Figure 40.

6.7 Conclusions

The unity-gain cross frequency of the LM3900 is 2.5 MHz which is approximately three times that of a "741" op amp. The performance of the amplifier does limit the performance of the filter. Historically, RC active filters started with little concern for these practical problems. The sensitivity functions were a big step forward as these demonstrated that many of the earlier suggested realization techniques for RC active filters had passive component sensitivity functions which varied as Q or even Q^2. The Bi-Quad circuit has reduced the problems with the passive components (sensitivity functions of 1 or 1/2) and recently the contributions of the amplifier on the performance of the filter are being investigated. An excellent treatment ("The Biquad: Part I — Some Practical Design Considerations," L.C. Thomas, IEEE Transactions on Circuit Theory, Vol. CT-18, No. 3, May 1971) has indicated the limits imposed by the characteristics of the amplifier by showing that the design value of Q (Q_D) will differ from the actual measured value of Q(Q_A) by the given relationship

$$Q_A = \frac{Q_D}{1 + \frac{2Q_D}{A_O\,\omega_a}\left(\omega_a - 2\omega_p\right)} \qquad (21)$$

where A_O is the open loop gain of the amplifier, ω_a is the dominant pole of the amplifier and ω_p is the resonant frequency of the filter. The result is that the trade-off between Q and center frequency (ω_p) can be determined for a given set of amplifier characteristics. When Q_A differs significantly from Q_D excessive dependence on amplifier characteristics is indicated. An estimate of the limitations of an amplifier can be made by arbitrarily allowing approximately a 10% effect on Q_A which results if

$$\frac{2Q_D}{A_O\omega_a}\left(\omega_a - 2\omega_p\right) = 0.1$$

or

$$\left(\frac{\omega_p}{\omega_a}\right) = 2.5 \times 10^{-2}\left(\frac{A_O}{Q_D}\right) + 0.5. \qquad (22)$$

As an example, using A_O = 2800 for the LM3900 we can estimate the maximum frequency where a Q_D = 50 would be reasonable as

$$\frac{f_p}{f_a} = 2.5 \times 10^{-2}\left(\frac{2.8 \times 10^3}{5 \times 10}\right) + 0.5$$

or

$$\frac{f_p}{f_a} = 1.9$$

therefore

$$f_p = 1.9\,f_a.$$

Again, using data of the LM3900, f_a = 1 kHz so this upper frequency limit is approximately 2 kHz for the assumed Q of 50. As indicated in equation (26) the value of Q_A can actually exceed the value of Q_D (Q enhancement) and, as expected, the filter can even provide its own input (oscillating). Excess phase shift in the high frequency characteristics of the amplifier typically cause unexpected oscillations. Phase compensation can be used in the Bi-Quad network to reduce this problem (see L.C. Thomas paper).

Designing for large passband gain also increases filter dependency on the characteristics of the amplifier and finally signal to noise ratio can usually be improved by taking gain in an input RC active filter (again see L.C. Thomas paper).

Somewhat larger Q's can be achieved by adding more filter sections in either a synchronously tuned cascade (filters tuned to same center frequency and taking advantage of the bandwidth shrinkage factor which results from the series connection) or as a standard multiple pole filter. All of the conventional filters can be realized and selection is based upon all of the performance requirements which the application demands. The cost advantages of the LM3900, the relatively large bandwidth and the ease of operation on a single power supply voltage make this product an excellent "building block" for RC active filters.

7.0 DESIGNING WAVEFORM GENERATORS

The multiple amplifiers of the LM3900 can be used to easily generate a wide variety of waveforms in the low frequency range (f ≤ 10 kHz). Voltage controlled oscillators (VCO's) are also possible and are presented in section 8.0 "Designing Phase-locked Loops and Voltage Controlled Oscillators." In addition, power oscillators (such as noise makers, etc.) are presented in section 10.11.3. The waveform generators which will be presented in this section are mainly of the switching type, but for completeness a sinewave oscillator has been included.

7.1 A Sinewave Oscillator

The design of a sinewave oscillator presents problems in both amplitude stability (and predictability) and output waveform purity (THD). If an RC bandpass filter is used as a high Q resonator for the oscillator circuit we can obtain an output waveform with low distortion and eliminate the problem of relative center frequency drift which exists if the active filter were used simply to filter the output of a separate oscillator.

A sinewave oscillator which is based on this principle is shown in Figure 41. The two-amplifier RC active filter is used as it requires only two capacitors and provides an overall non-inverting phase characteristic. If we add a non-inverting gain controlled amplifier around the filter we obtain the desired oscillator configuration. Finally, the sinewave output voltage is sensed and regulated as the average value is compared to a DC reference voltage, V_{REF}, by use of a differential averaging circuit. It can be shown that with the values selected for R_{15} and R_{16} (ratio of 0.64/1) that there is first order temperature compensation for CR_3 and the internal input diodes of the IC amplifier which is used for the "difference averager". Further, this also provides a simple way to regulate and to predict the magnitude of the output sinewave as

$$V_O\,\text{peak} = 2\,V_{REF}$$

which is essentially independent of both temperature and the magnitude of the power supply voltage (if V_{REF} is derived from a stable voltage source).

7.2 Squarewave Generator

The standard op amp squarewave generator has been modified as shown in Figure 42. The capacitor, C_1, alternately charges and discharges (via R_1) between the voltage limits which are established by the resistors R_2, R_3 and R_4. This combination produces a Schmitt-Trigger circuit and the operation can be understood by noticing that when the output is low (and if we neglect the current flow through R_4) the resistor R_2 (3M) will cause the trigger to fire when the current through this resistor equals the current which enters the (+) input (via R_3). This gives a firing voltage of approximately $R_2/(R_3)\ V^+$ (or $V^+/3$). The other trip point, when the output voltage is high, is approximately $[2(R_2/R_3)]\ V^+$, as $R_3 = R_4$, or $2/3(V^+)$. Therefore the voltage across the capacitor, C_1, will be the first one-half of an exponential waveform between these voltage trip limits and will have good symmetry and be essentially independent of the magnitude of the power supply voltage. If an unsymmetrical squarewave is desired, the trip points can be shifted to produce any desired mark/space ratio.

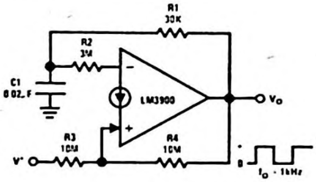
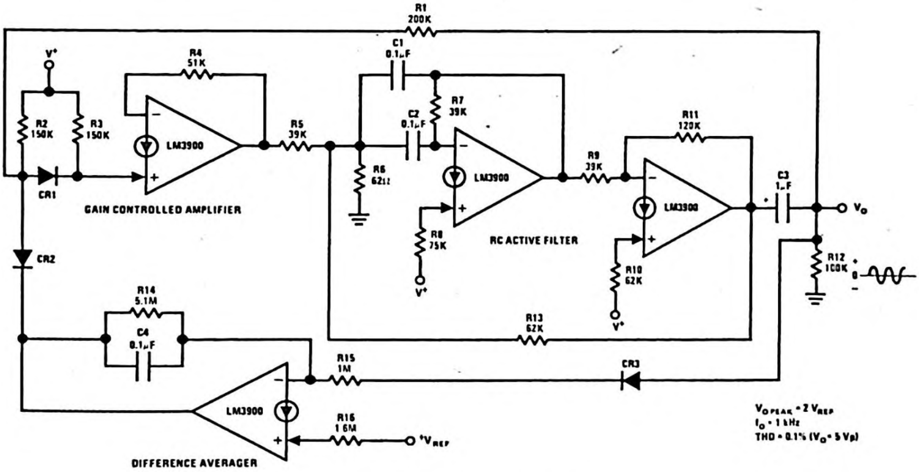

R1
30K
R2
3M
C1
0.02μF
LM3900
V_O
R3
10M
R4
10M
V+
+
0
f_O = 1kHz

FIGURE 42. A Squarewave Oscillator


R1
200K
V+
R4
51K
C1
0.1μF
R7
39K
R2
150K
R3
150K
LM3900
R5
39K
C2
0.1μF
R11
120K
CR1
GAIN CONTROLLED AMPLIFIER
R6
62Ω
LM3900
R9
39K
LM3900
C3
1μF
V_O
R8
75K
V+
RC ACTIVE FILTER
R10
62K
V+
R12
100K
+
0
−
CR2
R14
5.1M
C4
0.1μF
R13
62K
R15
1M
CR3
LM3900
R16
1.6M
+V_{REF}
DIFFERENCE AVERAGER

$V_{O\,PEAK} = 2\,V_{REF}$
$f_O = 1\ kHz$
THD = 0.1% (V_O = 5 V_p)

FIGURE 41. A Sinewave Oscillator

7.3 Pulse Generator

The squarewave generator can be slightly modified to provide a pulse generator. The slew rate limits of the LM3900 (0.5V/μsec) must be kept in mind as this limits the ability to produce a narrow pulse when operating at a high power supply voltage level. For example, with a +15 V_{DC} power supply the rise time, t_r, to change 15V is given by:

$$t_r = \frac{15V}{\text{Slew Rate}} = \frac{15V}{0.5V/\mu\text{sec}}$$

$$t_r = 30\,\mu\text{sec}.$$

The schematic of a pulse generator is shown in Figure 43. A diode has been added, CR_1, to allow separating the charge path to C_1 (via R_1) from the discharge path (via R_2). The circuit operates as follows, assume first that the output voltage has just switched low (and we will neglect the current flow through R_4). The voltage across C_1 is high and the magnitude of the discharge current (through R_2) is given by

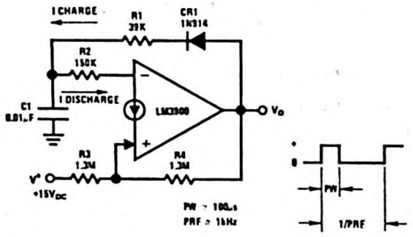


FIGURE 43. A Pulse Generator

$$I_{\text{Discharge}} \cong \frac{V_{C_1} - V_{BE}}{R_2}.$$

This current is larger than that entering the (+) input which is given by

$$I_{R_3} = \frac{V^+ - V_{BE}}{R_3}.$$

The excess current entering the (−) input terminal causes the amplifier to be driven to a low output voltage state (saturation). This condition remains for the long time interval (1/Pulse Repetition Frequency) until the R_2C_1 discharge current equals the I_{R_3} value (as CR_1 is OFF during this interval). The voltage across C_1 at the trip point, V_L, is given by

$$V_L = (I_{R_3})(R_2),$$

or

$$V_L = (V^+ - V_{BE})\left(\frac{R_2}{R_3}\right). \qquad (1)$$

At this time the output voltage will switch to a high state, V_{OHi}, and the current entering the (+) input will increase to

$$I_M^+ = \frac{V^+ - V_{BE}}{R_3} + \frac{V_{OHi} - V_{BE}}{R_4}.$$

Also CR_1 goes ON and the capacitor, C_1, charges via R_1. Some of this charge current is diverted via R_2 to ground (the (−) input is at $V_{CE_{SAT}}$ during this interval as the current mirror is demanding more current than the (−) input terminal can provide). The high trip voltage, V_H, is given by

$$V_H = (I_M^+)R_2 \quad \text{or}$$

$$V_H = \left(\frac{V^+ - V_{BE}}{R_3} + \frac{V_{OHi} - V_{BE}}{R_4}\right) R_2. \qquad (2)$$

A design proceeds by first choosing the trip points for the voltage across C_1. The resistors R_3 and R_4 are used only for this trip voltage control. The resistor R_2 affects the discharge time (the long interval) and also both of the trip voltages so this resistor is determined first from the required pulse repetition frequency (PRF). The value of R_2 is determined by the RC exponential discharge from V_H to V_L as this time interval, T_1, controls the PRF (T_1 = 1/PRF). If we start with the equation for the RC discharge we have

$$V_L = V_H\, e^{-\frac{T_1}{R_2C_1}}$$

or

$$\ell n \frac{V_L}{V_H} = -\frac{T_1}{R_2C_1}$$

or

$$T_1 = R_2C_1\, \ell n \frac{V_H}{V_L} \qquad (3)$$

To provide a low duty cycle pulse train we select small values for both V_H and V_L (such as 3V and 1.5V) and choose a starting value for C_1. Then R_2 is given by

$$R_2 = \frac{T_1}{C_1\, \ell n \frac{V_H}{V_L}}. \qquad (4)$$

If R_2 from (4) is not in the range of approximately 100 kΩ to 1 MΩ, choose another value for C_1. Now equation (1) can be used to find a value for R_3 to provide the V_L which was initially assumed. Similarly equation (2) allows R_4 to be calculated. Finally R_1 is determined by the required pulse width (PW) as the capacitor, C_1, must be charged from V_L to V_H by R_1.

This RC charging is given by (neglecting the loading due to R_2)

$$V_H \cong (V_{OHi} - V_D)\left(1 - e^{-\frac{T_2}{R_1C_1}}\right)$$

or

$$T_2 \cong - R_1C_1 \ln\left[1 - \frac{V_H}{V_{OHi} - V_D}\right], \text{ and finally}$$

$$R_1 \cong \frac{T_2}{-C_1 \ln\left[1 - \dfrac{V_H}{V_{OHi} - V_D}\right]} \qquad (5)$$

where T_2 is the pulse width desired and V_D is the forward voltage drop across CR_1.

As a design example:

Required: Provide a 100µs pulse every 1 ms. The power supply voltage is +15 V_{DC}

1.0 Start by choosing $V_L = 1.5V$

and $V_H = 3.0V$

2.0 Find R_2 from equation (4) assuming $C_1 = 0.01\mu F$.

$$R_2 = \frac{10^{-3}}{10^{-8} \ln\left(\frac{3.0}{1.5}\right)}$$

$$R_2 = \frac{10^5}{0.694} = 144\ k\Omega\ .$$

3.0 Find R_3 from equation (1)

$$R_3 = \frac{(V^+ - V_{BE})\ R_2}{V_L}$$

$$R_3 = \frac{(15 - 0.5)\ 1.44 \times 10^5}{1.5}$$

$$R_3 = 1.39\ M\Omega$$

4.0 Find R_4 from equation (2).

$$R_4 = \frac{(V_{OHi} - V_{BE})}{\dfrac{V_H}{R_2} - \dfrac{V^+ - V_{BE}}{R_3}}$$

$$R_4 = \frac{(14.2 - 0.5)}{\dfrac{3}{1.44 \times 10^5} - \dfrac{15 - 0.5}{1.39 \times 10^6}}$$

$$R_4 = 1.32\ M\Omega$$

5.0 Find R_1 from equation (5).

$$R_1 = \frac{10^{-4}}{-10^{-8} \ln\left(1 - \dfrac{3}{(14.2 - 0.7)}\right)}$$

$$R_1 = \frac{10^4}{-\ln\left(1 - \dfrac{3}{13.5}\right)}$$

$$R_1 = \frac{10^4}{0.252} = 39.7\ k\Omega\ .$$

These values (to the nearest 5% standard) have been added to Figure 43.

7.4 Triangle Waveform Generator

Triangle waveforms are usually generated by an integrator which receives first a positive DC input voltage then a negative DC input voltage. The LM3900 easily provides this operation in a system which operates with only a single power supply voltage by making use of the current mirror which exists at the (+) input. This allows the generation of a triangle waveform without requiring a negative DC input voltage.

The schematic diagram of a triangle waveform generator is shown in Figure 44. One amplifier is doing the integration by operating first with the current through R_1, to produce the negative output voltage slope, and then when the output of the second amplifier (the Schmitt-Trigger) is high, the current through R_2 causes the output voltage to increase. If $R_1 = 2R_2$, the output waveform will have good symmetry. The timing for one-half of the period (T/2) is given by

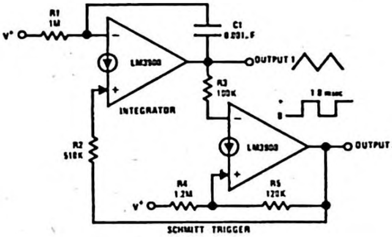


FIGURE 44. A Triangle Waveform Generator

$$\frac{T}{2} = \frac{(R_1C_1)\ \Delta V_O}{V^+ - V_{BE}}$$

or the output frequency becomes

$$f_o = \frac{V^+ - V_{BE}}{2R_1C_1\ \Delta V_O}$$

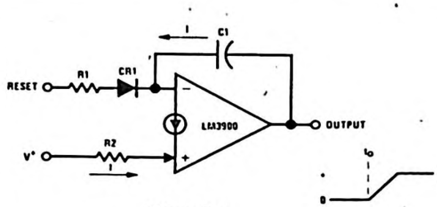
where we have assumed $R_1 = 2R_2$, V_{BE} is the DC voltage at the (−) input (0.5 V_{DC}), and ΔV_O

is the difference between the trip points of the Schmitt-Trigger. The design of the Schmitt-Trigger has been presented in the section on Digital and Switching Circuits (9.0) and the trip voltages control the peak-to-peak excursion of the triangle output voltage waveform. The output of the Schmitt circuit provides a squarewave of the same frequency.

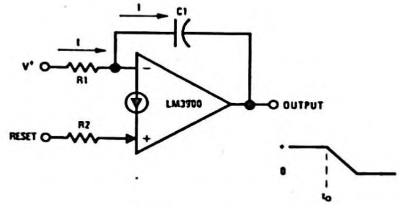
7.5 Sawtooth Waveform Generator

The previously described triangle waveform generator, Figure 44, can be modified to produce a sawtooth waveform. Two types of waveforms can be provided, both a positive ramp and a negative ramp sawtooth waveform by selecting R_1 and R_2. The reset time is also controlled by the ratio of R_1 to R_2. For example, if $R_1 = 10\ R_2$ a positive ramp sawtooth results and if $R_2 = 10\ R_1$ a negative ramp sawtooth can be obtained. Again, the slew rate limits of the amplifier (0.5V/µs) will limit the minimum retrace time, and the increased slew rate of a negative going output will allow a faster retrace for a positive ramp sawtooth waveform.

To provide a gated sawtooth waveform, the circuits shown in Figure 45 can be used. In Figure 45(a), a positive ramp is generated by integrating the current, I, which is entering the (+) input. Reset is provided via R_1 and CR_1 keeps R_1 from loading at the (−) input during the sweep interval. This will sweep from $V_{O\ MIN}$ to $V_{O\ MAX}$ and will remain at $V_{O\ MAX}$ until reset. The interchange of the input leads, Figure 45(b), will generate a negative ramp, from $V_{O\ MAX}$ to $V_{O\ MIN}$.


I
C1
RESET
R1
CR1
−
LM3900
OUTPUT
V+
R2
+
I
t0
+
0

(a) Positive Ramp


I
C1
I
V+
R1
−
LM3900
OUTPUT
R2
RESET
+
+
0
t0

(b) Negative Ramp

FIGURE 45. Gated Sawtooth Generators

7.5.1 Generating a Very Slow Sawtooth Waveform

The LM3900 can be used to generate a very slow sawtooth waveform which can be used to generate long time delay intervals. The circuit is shown in Figure 46 and uses four amplifiers. Amps 1 and 2 are cascaded to increase the gain of the integrator and the output is the desired very slow sawtooth waveform. Amp 3 is used to exactly supply the bias current to Amp 1.

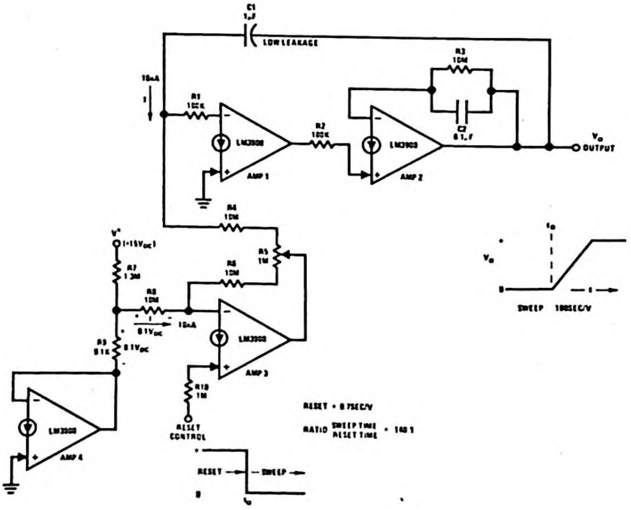

C1
1µF
LOW LEAKAGE
10nA
I
R1
100K
−
LM3900
+
AMP 1
R2
100K
R3
10M
C2
0.1µF
LM3900
AMP 2
Vo
OUTPUT
R4
10M
R5
1M
V+
(+15VDC)
R7
1.3M
R6
10M
R8
10M
+
I
−
0.1VDC
10nA
R9
91K
0.1VDC
LM3900
AMP 3
R10
1M
RESET CONTROL
LM3900
AMP 4
RESET = 0.75SEC/V
RATIO SWEEP TIME / RESET TIME = 140:1
+
RESET
SWEEP
0
t0
Vo
t0
+
0
t
SWEEP 100SEC/V

FIGURE 46. Generating Very Slow Sawtooth Waveforms

With resistor R_8 opened up and the reset control at zero volts, the potentiometer, R_5, is adjusted to minimize the drift in the output voltage of Amp 2 (this output must be kept in the linear range to insure that Amp 2 is not in saturation). Amp 4 is used to provide a bias reference which equals the DC voltage at the (-) input of Amp 3. The resistor divider, R_7 and R_9, provides a 0.1 V_{DC} reference voltage across R_9 which also appears across R_8. The current which flows through R_8, I, enters the (-) input of Amp 3 and causes the current through R_6 to drop by this amount. This causes an imbalance as now the current flow through R_4 is no longer adequate to supply the input current of Amp 1. The net result is that this same current, I, is drawn from capacitor C_1 and causes the output voltage of Amp 2 to sweep slowly positive. As a result of the high impedance values used, the PC component board used for this circuit must first be cleaned and then coated with silicone rubber to eliminate the effects of leakage currents across the surface of the board. The DC leakage currents of the capacitor, C_1, must also be small compared to the 10 nA charging current. For example, an insulation resistance of 100,000 MΩ will leak 0.1 nA with 10 V_{DC} across the capacitor and this leakage rapidly increases at higher temperatures. Dielectric polarization of the dielectric material may not cause problems if the circuit is not rapidly cycled. The resistor, R_8, and the capacitor, C_1, can be scaled to provide other basic sweep rates. For the values shown on Figure 46 the 10 nA current and the 1µF capacitor establish a sweep rate of 100 sec/volt. The reset control pulse (Amp 3 (+) input) causes Amp 3 to go to the positive output saturation state and the 10 MΩ (R_4) gives a reset rate of 0.7 sec/volt. The resistor, R_1, prevents a large discharge current of C_1 from overdriving the (-) input and overloading the input clamp device. For larger charging currents, a resistor divider can be placed from the output of Amp 4 to ground and R_8 can tie from this tap point directly to the (-) input of Amp 1.

7.6 Staircase Waveform Generators

A staircase generator can be realized by supplying pulses to an integrator circuit. The LM-3900 also can be used with a squarewave input signal and a differentiating network where each transition of the input squarewave causes a step in the output waveform (or two steps per input cycle). This is shown in Figure 47. These pulses of current are the charge and discharge currents of the input capacitor, C_1. The charge current, I_C, enters the (+) input and is mirrored about ground and is "drawn into" the (-) input. The discharge current, I_D, is drawn through the diode at the input, CR_1, and therefore also causes a step on the output staircase.

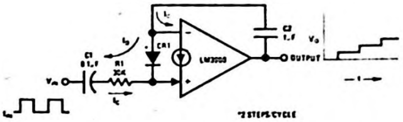


FIGURE 47. Pumping the Staircase Via Input Differentiator

A free running staircase generator is shown in Figure 48. This uses all four of the amplifiers which are available in one LM3900 package.

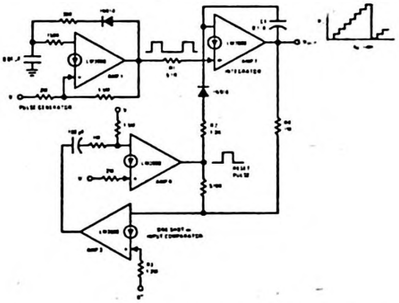


FIGURE 48. A Free Running Staircase Generator

Amp 1 provides the input pulses which "pump up" the staircase via resistor R_1 (see section 7.3 for the design of this pulse generator). Amp 2 does the integrate and hold function and also supplies the output staircase waveform. Amps 3 and 4 provide both a compare and a one-shot multivibrator function (see the section on Digital and Switching Circuits for the design of this dual function one-shot). Resistor R_4 is used to sample the staircase output voltage and to compare it with the power supply voltage (V^+) via R_3. When the output exceeds approximately 80% of V^+ the connection of Amps 3 and 4 cause a 100 µ sec reset pulse to be generated. This is coupled to the integrator (Amp 2) via R_2 and causes the staircase output voltage to fall to approximately zero volts. The next pulse out of Amp 1 then starts a new stepping cycle.

7.7 A Pulse Counter and a Voltage Variable Pulse Counter

The basic circuit of Figure 48 can be used as a pulse counter simply by omitting Amp 1 and feeding input voltage pulses directly to R_1. A simpler one-shot/comparator which requires only one amplifier can also be used in place of Amps 3 and 4 (again, see the section on Digital and Switching Circuits). To extend the time interval between pulses, an additional amplifier can be used to supply base current to

Amp 2 to eliminate the tendency for the output voltage to drift up due to the 30 nA input current (see section 7.5.1). The pulse count can be made voltage variable simply by removing the comparator reference (R_3) from V^+ and using this as a control voltage input. Finally, the input could be derived from differentiating a squarewave input as was shown in Figure 47 and if only one step per cycle were desired, the diode, CR_1 of Figure 47, can be eliminated.

7.8 An Up-down Staircase Waveform Generator

A staircase waveform which first steps up and then steps down is provided by the circuit shown in Figure 49. An input pulse generator provides the pulses which cause the output to step up or down depending on the conduction of the clamp transistor, Q_1. When this is ON, the "down" current pulse is diverted to ground and the staircase then steps "up". When the upper voltage trip point of Amp 2 (Schmitt-Trigger—see section on Digital and Switching Circuits) is reached, Q_1 goes OFF and as a result of the smaller "down" input resistor (one-half the value of the "up" resistor, R_1) the staircase steps "down" to the low voltage trip point of Amp 2. The output voltage therefore steps up and down between the trip voltages of the Schmitt-Trigger.

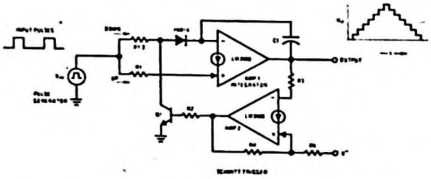


FIGURE 49. An Up-down Staircase Generator

8.0 DESIGNING PHASE-LOCKED LOOPS AND VOLTAGE CONTROLLED OSCILLATORS

The LM3900 can be connected to provide a low frequency (f < 10 kHz) phase-locked loop (PL^2). This is a useful circuit for many control applications. Tracking filters, frequency to DC converters, FM modulators and demodulators are applications of a PL^2.

8.1 Voltage Controlled Oscillators (VCO)

The heart of a PL^2 is the voltage controlled oscillator (VCO). As the PL^2 can be used for many functions, the required linearity of the transfer characteristic (frequency out to DC voltage in) depends upon the application. For low distortion demodulation of an FM signal, a high degree of linearity is necessary whereas a tracking filter application would not require this performance in the VCO.

A VCO circuit is shown in Figure 50. Only two amplifiers are required, one is used to integrate the DC input control voltage, V_C, and the other is connected as a Schmitt-trigger which monitors the output of the integrator. The trigger circuit is used to control the clamp transistor, Q_1. When Q_1 is conducting, the input current, I_2, is shunted to ground. During this one-half cycle the input current, I_1, causes the output voltage of the integrator to ramp down. At the minimum point of the triangle waveform (output 1), the Schmitt circuit changes state and transistor Q_1 goes OFF. The current, I_2, is exactly twice the value of I_1 ($R_2 = R_1/2$) such that a charge current (which is equal to the magnitude of the discharge current) is drawn through the capacitor, C, to provide the increasing portion of the triangular waveform (output 1).

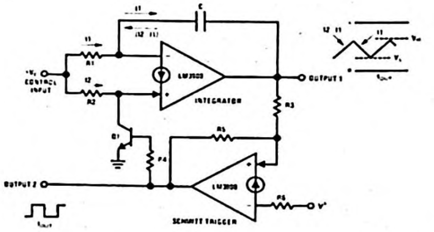


FIGURE 50. A Voltage Controlled Oscillator

The output frequency for a given DC input control voltage depends on the trip voltages of the Schmitt circuit (V_H and V_L) and the components R_1 and C_1 (as $R_2 = R_1/2$). The time to ramp down from V_H to V_L corresponds to one-half the period (T) of the output frequency and can be found by starting with the basic equation of the integrator

$$V_O = -\frac{1}{C} \int I_1 \, dt \tag{1}$$

as I_1 is a constant (for a given value of V_C) which is given by

$$I_1 = \frac{V_C - V_{BE}}{R_1} \tag{2}$$

equation (1) simplifies to

$$\Delta V_O = -\frac{I_1}{C}(\Delta t)$$

or

$$\frac{\Delta V_O}{\Delta t} = -\frac{I_1}{C} \qquad (3)$$

Now the time, Δt, to sweep from V_H to V_L becomes

$$\Delta t_1 = \frac{(V_H - V_L)C}{I_1} \quad \text{or}$$

$$T = \frac{2(V_H - V_L)C}{I_1} \quad \text{and}$$

$$f = \frac{1}{T} = \frac{I_1}{2(V_H - V_L)C}. \qquad (4)$$

Therefore, once V_H, V_L, R_1 and C are fixed in value, the output frequency, f, is a linear function of I_1 (as desired for a VCO).

The circuit shown in Figure 50 will require $V_C > V_{BE}$ to oscillate. A value of $V_C = 0$ provides $f_{OUT} = 0$, which may or may not be desired. Two common-mode input biasing resistors can be added as shown in Figure 51 to allow $f_{OUT} = f_{MIN}$ for $V_C = 0$. In general, if these resistors are a factor of 10 larger than their corresponding resistor (R_1 or R_2) a large control frequency ratio can be realized. Actually, V_C could range outside the supply voltage limit of V^+ and this circuit will still function properly.

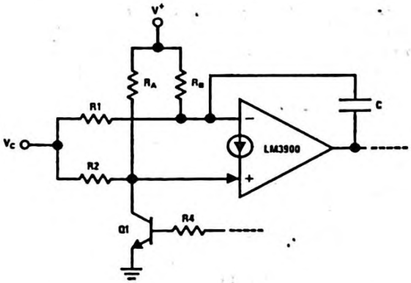


FIGURE 51. Adding Input Common-mode Biasing Resistors

The output frequency of this circuit can be increased by reducing the peak-to-peak excursion of the triangle waveform (output 1) by design of the trip points of the Schmitt circuit. A limit is reached when the triangular sweep output waveform exceeds the slew rate limit of the LM3900 (0.5V/µs). Note that the output of the Schmitt circuit has to move up only one V_{BE} to bring the clamp transistor, Q_1, ON, and therefore output slew rate of this circuit is not a limit.

To improve the temperature stability of the VCO, a PNP emitter follower can be used to give approximate compensation for the V_{BE}'s at the inputs to the amplifier (see Figure 52). Finally to improve the mark to space ratio accuracy over temperature and at low control voltages, an additional amplifier can be added such that both reference currents are applied to the same type of (inverting) inputs of the LM3900. The circuit to accomplish this is shown within dotted lines in Figure 53.

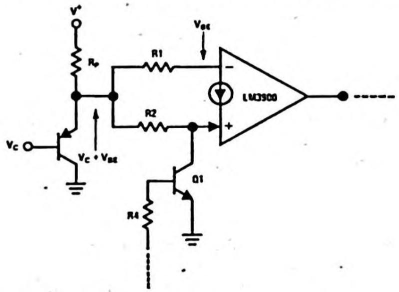


FIGURE 52. Reducing Temperature Drift

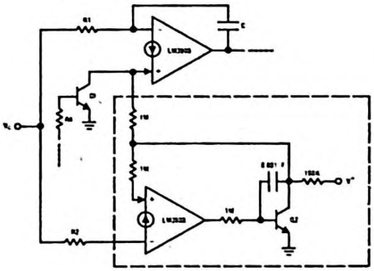


FIGURE 53. Improving Mark/Space Ratio

8.2 Phase Comparator

A basic phase comparator is shown in Figure 54. This circuit provides a pulse-width modulated output voltage waveform, $V_O{}^1$, which must be filtered to provide a DC output voltage (this filter can be the same as the one needed in the PL²). The resistor R_2 is made smaller than R_1 so the (+) input serves to inhibit the (–) input signal. The center of the dynamic range is indicated by the waveforms shown on the figure (90° phase difference between f_{IN} and f_{VCO}).

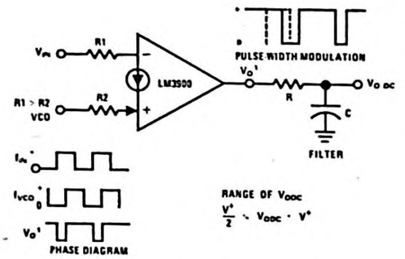


FIGURE 54. Phase Comparator

The filtered DC output voltage will center at $3V^+/4$ and can range from $V^+/2$ to V^+ as the phase error ranges from 0 degrees to 180 degrees.

8.3 A Complete Phase-locked Loop

A phase-locked loop can be realized with three of the amplifiers as shown in Figure 55. This has a center frequency of approximately 3 kHz.

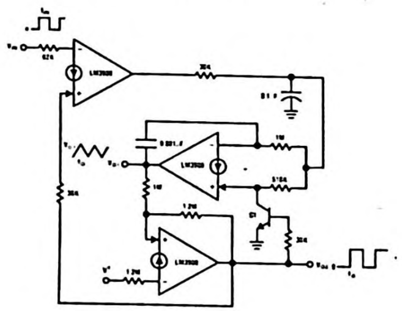


FIGURE 55. A Phase-locked Loop

To increase the lock range, DC gain can be added at the input to the VCO by using the fourth amplifier of the LM3900. If the gain is inverting, the limited DC dynamic range out of the phase detector can be increased to improve the frequency lock range. With inverting gain, the input to the VCO could go to zero volts. This will cause the output of the VCO to go high (V^+) and will latch if applied to the (+) input of the phase comparator. Therefore apply the VCO signal to the (-) input of the phase comparator or add the common-mode biasing resistors of Figure 51.

8.4 Conclusions

One LM3900 package (4 amplifiers) can provide all of the operations necessary to make a phase-locked loop. In addition, a VCO is a generally useful component for other system applications.

9.0 DESIGNING DIGITAL AND SWITCHING CIRCUITS

The amplifiers of the LM3900 can be overdriven and used to provide a large number of low speed digital and switching circuit applications for control systems which operate off of single power supply voltages larger than the standard +5 V_{DC} digital limit. The large voltage swing and slower speed are both advantages for most industrial control systems. Each amplifier of the LM3900 can be thought of as "a super transistor" with a β of 1,000,000 (25 nA input current and 25 mA output current) and with a non-inverting input feature. In addition, the active pull-up and pull-down which exists at the output will supply larger currents than the simple resistor pull-ups which are used in digital logic gates. Finally, the low input currents allow timing circuits which minimize the capacitor values as large impedance levels can be used with the LM3900.

9.1 An "OR" GATE

An OR gate can be realized by the circuit shown in Figure 56. A resistor (150 kΩ) from V^+ to the (-) input keeps the output of the amplifier in a low voltage saturated state for all inputs A, B, and C at 0V. If any one of the input signals were to go high ($\cong V^+$) the current flow through the 75 kΩ input resistor will cause the amplifier to switch to the positive output saturation state ($V_O \cong V^+$). The current loss through the other input resistors (which have an input in the low voltage state) represents an insignificant amount of the total input current which is provided by the, at least one, high voltage input. More than three inputs can be OR'ed if desired.

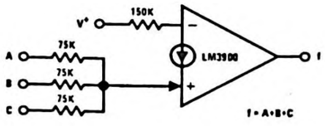


FIGURE 56. An "OR" Gate

The "fan-out" or logical drive capability is large (50 gates if each gate input has a 75 kΩ resistor) due to the 10 mA output current capability of the LM3900. A NOR gate can be obtained by interchanging the inputs to the LM3900.

9.2 An "AND" Gate

A three input AND gate is shown in Figure 57. This gate requires all three inputs to be high in order to have sufficient current entering the (+) input to cause the output of the amplifier to switch high. The addition of R_2 causes a smaller current to enter the (+) input when only two of the inputs are high. (A two input AND gate would not require a resistor as R_2). More than three inputs becomes difficult with this resistor summing approach as the (+) input is too close to having the necessary current to switch just prior to the last input going high. For a larger fan-in an input diode network (similar to DTL) is recommended as shown in Figure 58. Interchange the inputs for a NAND gate.

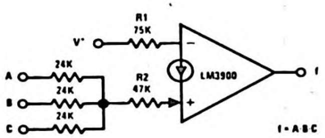

R1
75K
V+
24K
A
24K
B
24K
C
R2
47K
LM3900
f
f = A·B·C

FIGURE 57. An "AND" Gate

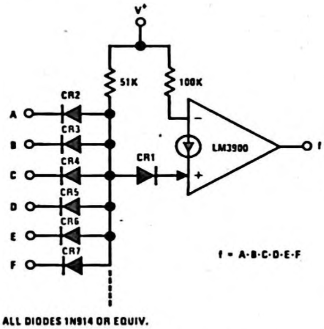

V+
51K
100K
CR2
A
CR3
B
CR4
C
CR1
CR5
D
CR6
E
CR7
F
LM3900
f
f = A·B·C·D·E·F
ALL DIODES 1N914 OR EQUIV.

FIGURE 58. A Large Fan-in "AND" Gate

9.3 A Bi-stable Multivibrator

A bi-stable multivibrator (an asynchronous RS flip-flop) can be realized as shown in Figure 59. Positive feedback is provided by resistor R_4 which causes the latching. A positive pulse at the "set" input causes the output to go high and a "reset" positive pulse will return the output to essentially $0V_{DC}$

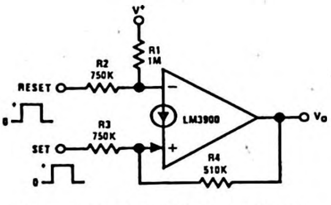

V+
R1
1M
R2
750K
RESET
0
R3
750K
SET
0
LM3900
Vo
R4
510K

FIGURE 59. A Bi-stable Multivibrator

9.4 Trigger Flip Flops

Trigger flip flops are useful to divide an input frequency as each input pulse will cause the output of a trigger flip flop to change state. Again, due to the absence of a clocking signal input, this is for an asynchronous logic application. A circuit which uses only one amplifier is shown in Figure 60. Steering of the differentiated positive input trigger is provided by the diode CR2. For a low output voltage state, CR2 shunts the trigger away from the (–) input and resistor R_3 couples this positive input trigger to the (+) input terminal. This causes the output to switch high. The high voltage output state now keeps CR2 OFF and the smaller value of (R_5 + R_6) compared with R_3 causes a larger positive input trigger to be coupled to the (–) input which causes the output to switch to the low voltage state.

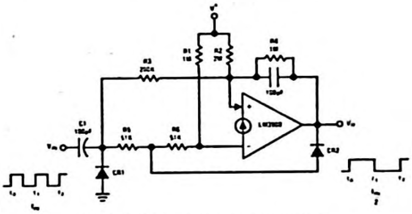

V+
R3
R1
R2
R4
C1
R5
R6
CR1
CR2

FIGURE 60. A Trigger Flip Flop

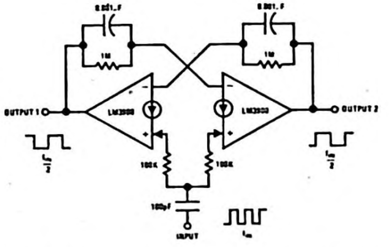

0.001 μF
0.001 μF
1M
1M
OUTPUT 1
OUTPUT 2
100K
100K
100pF
INPUT

FIGURE 61. A Two-amplifier Trigger Flip Flop

A second trigger flip flop can be made which consists of two amplifiers and also provides a complimentary output. This connection is shown in Figure 61.

9.5 Monostable Multivibrators (One-shots)

Monostable multivibrators can be made using one or two of the amplifiers of the LM3900. In addition, the output can be designed to be either high or low in the quiescent state. Further, to increase the usefulness, a one-shot can be designed which triggers at a particular DC input voltage level to serve the dual role of providing first a comparator and then a pulse generator.

9.5.1 A Two-amplifier One-shot

A circuit for a two-amplifier one-shot is shown in Figure 62. As the resistor, R_2, from V^+ to the (-) input is smaller than R_5 (from V^+ to the (+) input), amplifier 2 will be biased to a low-voltage output in the quiescent state. As a result, no current is supplied to the (-) input of amplifier 1 (via R_3) which causes the output of this amplifier to be in the high voltage state. Capacitor C_1 therefore has essentially the full V^+ supply voltage across it ($V^+ - 2\,V_{BE}$). Now when a differentiated trigger (due to C_2) causes amplifier 1 to be driven ON (output voltage drops to essentially zero volts) this negative transient is coupled (via C_1) to the (-) input of amplifier 2 which causes the output of this amplifier to be driven high (to positive saturation). This condition remains while C_1 discharges via (R_1) from approximately V^+ to approximately $V^+/2$. This time interval is the pulse width (PW). After C_1 no longer diverts sufficient current of R_2 away from the (-) input of amplifier 2 (i.e., C_1 is discharged to approximately $V^+/2$ V) the stable DC state is restored—amplifier 2 output low and amplifier 1 output high.

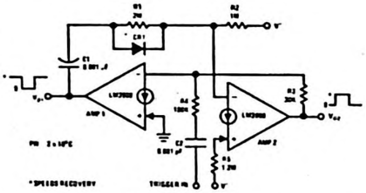


FIGURE 62. A One-shot Multivibrator

This circuit can be rapidly re-triggered due to the action of the diode, CR_1. This re-charges C_1 as amplifier 1 drives full output current capability (approximately 10 mA) through C_1, CR_1 and into the saturated (-) input of amplifier 2 to ground. The only time limit is the 10 mA available from amplifier 1 and the value of C_1. If a rapid reset is not required, CR_1 can be omitted.

9.5.2 A Combination One-shot/Comparator Circuit

In many applications a pulse is required if a DC input signal exceeds a predetermined value. This exists in free-running oscillators where after a particular output level has been reached a reset pulse must be generated to recycle the oscillator. This double function is provided with the circuit of Figure 63. The

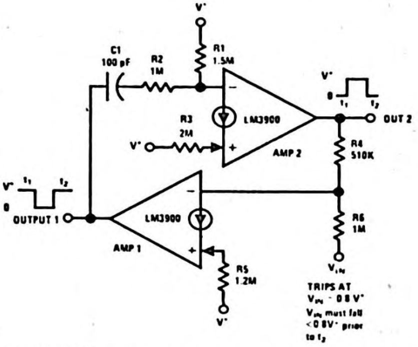


FIGURE 63. A One-shot Multivibrator with an Input Comparator

resistors R_5 and R_6 of amplifier 1 provide the inputs to a comparator and, as shown, an input signal, V_{IN}, is compared with the supply voltage, V^+. The output voltage of amplifier 1 is normally in a high voltage state and will fall and initiate the generation of the output pulse when V_{IN} is R_6/R_5 V^+ or approximately 80% of V^+. To keep V_{IN} from disturbing the pulse generation it is required that V_{IN} fall to less than the trip voltage prior to the termination of the output pulse. This is the case when this circuit is used to generate a reset pulse and therefore this causes no problems.

9.5.3 A One-amplifier One-shot (Positive Pulse)

A one-shot circuit can be realized using only one amplifier as shown in Figure 64.

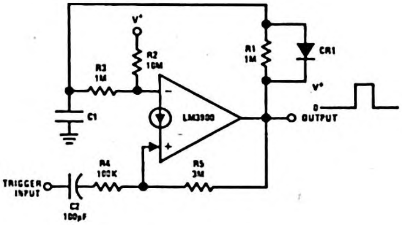


FIGURE 64. A One-amplifier One-shot (Positive Output)

The resistor R_2 keeps the output in the low voltage state. A differentiated positive trigger causes the output to switch to the high voltage state and resistor R_5 latches this state. The capacitor, C_1, charges from essentially ground to approximately $V^+/4$ where the circuit latches back to the quiescent state. The diode, CR_1, is used to allow a rapid re-triggering.

9.5.4 A One-amplifier One-shot (Negative Pulse)

A one-amplifier one-shot multivibrator which has a quiescent state with the output high and which falls to zero volts for the pulse duration is shown in Figure 65.

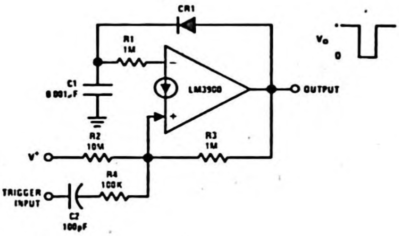


FIGURE 65. A One-amplifier One-shot (Negative Output)

The sum of the currents through R_2 and R_3 keeps the (–) input at essentially ground. This causes V_O to be in the high voltage state. A differentiated negative trigger waveform causes the output to switch to the low voltage state. The large voltage across C_1 now provides input current via R_1 to keep the output low until C_1 is discharged to approximately $V^+/10$. At this time the output switches to the stable high voltage state.

If the R_4 C_2 network were moved to the (–) input terminal, the circuit will trigger on a differentiated positive trigger waveform.

9.6 Comparators

The voltage comparator is a function required for most system operations and can easily be performed by the LM3900. Both an inverting and a non-inverting comparator can be obtained.

9.6.1 A Comparator for Positive Input Voltages

The circuit in Figure 66 is an inverting comparator. To insure proper operation, the reference voltage must be larger than V_{BE}, but there is no upper limit as long as the input resistor is large enough to guarantee that the input current will not exceed 200µA.

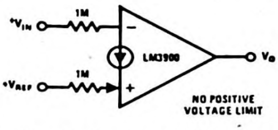


FIGURE 66. An Inverting Voltage Comparator

9.6.2 A Comparator for Negative Input Voltages

Adding a common-mode biasing network to the comparator in Figure 66 makes it possible to compare voltages between zero and one volt as well as the comparison of rather large negative voltages, Figure 67. When working with negative voltages, the current supplied by the common-mode network must be large enough to satisfy both the current drain demands of the input voltages and the bias current requirement of the amplifier.

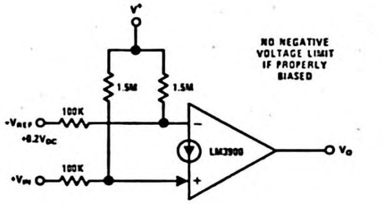


FIGURE 67. A Non-inverting Low-voltage Comparator

9.6.3 A Power Comparator

When used in conjunction with an external transistor, this power comparator will drive loads which require more current than the IC amplifier is capable of supplying. Figure 68 shows a non-inverting comparator which is capable of driving a 12V, 40 mA panel lamp.

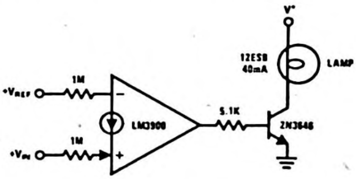


FIGURE 68. A Non-inverting Power Comparator

9.6.4 A More Precise Comparator

A more precise comparator can be designed by using a second amplifier such that the input voltages of the same type of inputs are compared. The (–) input voltages of two amplifiers are naturally more closely matched initially and track well with temperature changes. The comparator of Figure 69 uses this concept.

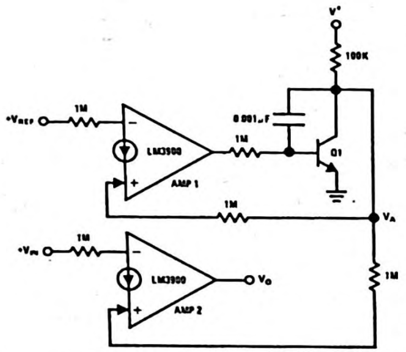


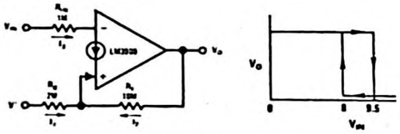
FIGURE 69. A More Precise Comparator

The current established by V_{REF} at the inverting input of amplifier 1 will cause transistor Q_1 to adjust the value of V_A to supply this current. This value of V_A will cause an equal current to flow into the non-inverting input of amplifier 2. This current corresponds more exactly to the reference current of amplifier 1.

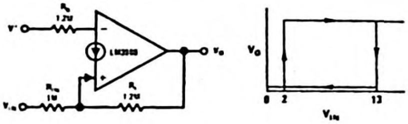
A differential input stage can also be added to the LM3900 (see section 10.16) and the resulting circuit can provide a precision comparator circuit.

9.7 Schmitt-Triggers

Hysteresis may be designed into comparators which use the LM3900 as shown in Figure 70.



(a) INVERTING



(b) NON-INVERTING

FIGURE 70. Schmitt-Triggers

The lower switch point for the inverting Schmitt-Trigger is determined by the amount of current flowing into the positive input with the output voltage low. When the input current, I_3, drops below the level required by the current mirror, the output will switch to the high limit. With V_O high, the current demanded by the mirror is increased by a fixed amount, I_2. As a result, the I_3 required to switch the output increases this same amount. Therefore, the switch points are determined by selecting resistors which will establish the required currents at the desired input voltages. Reference current (I_1) and feedback current (I_2) are set by the following equation.

$$I_1 = \frac{V^+ - \phi}{R_B}$$

$$I_2 = \frac{V_{O\,MAX} - \phi}{R_F}$$

By adjusting the values of R_B, R_F, and R_{IN}, the switching values of V_{IN} may be set to any levels desired.

The non-inverting Schmitt-Trigger works in the same way except that the input voltage is applied to the (+) input. The range of V_{IN} may be very large when compared with the operating voltage of the amplifier.

10.0 SOME SPECIAL CIRCUIT APPLICATIONS

This section contains various special circuits which did not fit the order of things or which are one-of-a-kind type of applications.

10.1 Current Sources and Sinks

The amplifiers of the LM3900 can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks. These can be multiple sources or single sources which are fixed in value or made voltage variable.

10.1.1 A Fixed Current Source

A multiple fixed current source is provided by the circuit of Figure 71. A reference voltage (1 V_{DC}) is established across resistor R_3 by the resistive divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to also be 1 V_{DC}. This controls the emitter current of transistor Q_1 and if we neglect the small current diverted into the (–) input via the 1M input resistor (13.5 μA) and the base current of Q_1 and Q_2 (an additional 2% loss if the β of these transistors is 100), essentially this same current is available out of the collector of Q_1.

Larger input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.

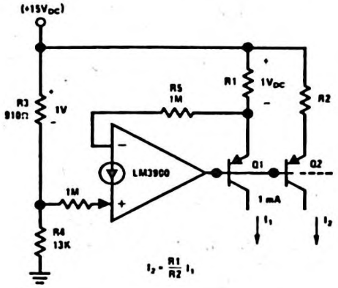

(+15V$_{DC}$)
R3
910Ω
1V
R5
1M
R1
1V$_{DC}$
R2
LM3900
Q1
Q2
1M
1 mA
I_1
I_2
R4
13K
$I_2 = \frac{R1}{R2} I_1$

FIGURE 71. Fixed Current Sources

The resistor, R_2, can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

10.1.2 A Voltage Variable Current Source

A voltage variable current source is shown in Figure 72. The transconductance is $-(1/R_2)$ as the voltage gain from the input terminal to the emitter of Q_1 is -1. For a V_{IN} = 0 V_{DC} the output current is essentially zero mA DC. The resistors R_1 and R_6 guarantee that the amplifier can turn OFF transistor Q_1.

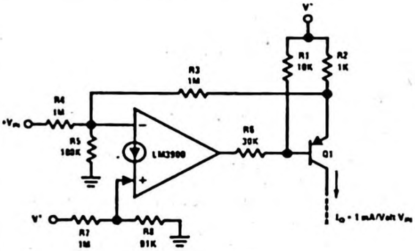
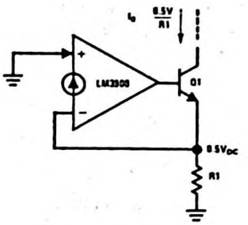

V+
R1
10K
R2
1K
R3
1M
R4
1M
+V$_{IN}$
R5
100K
R6
30K
LM3900
Q1
V+
R7
1M
R8
91K
I_O = 1 mA/Volt V_{IN}

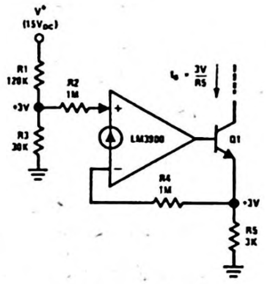
FIGURE 72. A Voltage Controlled Current Source

10.1.3 A Fixed Current Sink

Two current sinks are shown in Figure 73. The circuit of Figure 73(a) requires only one resistor and supplies an output current which is directly proportional to this R value. A negative temperature coefficient will result due to the 0.5 V_{DC} reference being the base-emitter junction voltage of the (–) input transistor. If this temperature coefficient is objectionable, the circuit of Figure 73(b) can be employed.


I_O $\frac{0.5V}{R1}$
LM3900
Q1
0.5V$_{DC}$
R1

(a) A SIMPLE CURRENT SINK


V+
(15V$_{DC}$)
R1
120K
R2
1M
+3V
R3
30K
$I_O = \frac{3V}{R5}$
LM3900
Q1
R4
1M
+3V
R5
3K

(b) REDUCING TEMPERATURE DRIFT OF I_O

FIGURE 73. Fixed Current Sinks

10.1.4 A Voltage Variable Current Sink

A voltage variable current sink is shown in Figure 74. The output current is 1 mA per volt of V_{IN} (as R_5 = 1 kΩ and the gain is +1). This circuit provides approximately 0 mA output current for V_{IN} = 0 V_{DC} .

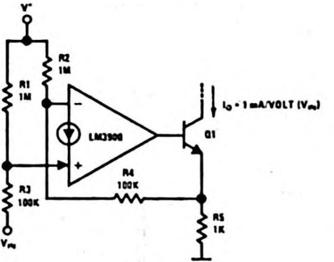

V+
R2
1M
R1
1M
I_O = 1 mA/VOLT (V_{IN})
LM3900
Q1
R4
100K
R3
100K
+V$_{IN}$
R5
1K

FIGURE 74. A Voltage Controlled Current Sink

10.2 Operation From ±15 V_{DC} Power Supplies

If the ground pin (no. 7) is returned to a negative voltage and some changes are made in the biasing circuits, the LM3900 can be operated from ±15V_{DC} power supplies.

10.2.1 An AC Amplifier Operating with ±15 V_{DC} Power Supplies

An AC coupled amplifier is shown in Figure 75. The biasing resistor, R_B, is now returned to ground and both inputs bias at one V_{BE} above the $-V_{EE}$ voltage (approximately $-15\ V_{DC}$).

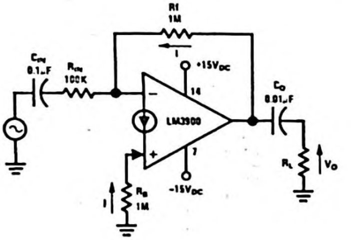
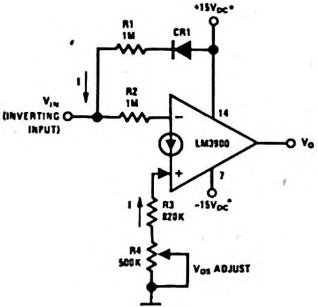


FIGURE 75. An AC Amplifier Operating with ± 15 V_{DC}

With $R_f = R_B$, V_O will bias at approximately 0 V_{DC} to allow a maximum output voltage swing. As pin 7 is common to all four of the amplifiers which are in the same package, the other amplifiers are also biased for operation off of ±15 V_{DC}.

10.2.2 A DC Amplifier Operating with ±15 V_{DC} Power Supplies

Biasing a DC amplifier is more difficult and requires that the ± power supplies be complementary tracking (i.e., $|+V_{CC}| = |-V_{EE}|$). The operation of this biasing can be easier understood if we start by first considering the amplifier without including the feedback resistors, as shown in Figure 76. If $R_1 = R_2 = R_3 + R_4 = 1\ M\Omega$ and $|+V_{CC}| = |-V_{EE}|$, then the current, I, will bias V_{IN} at zero volts DC (resistor R_4 can be used to adjust this). The diode, CR_1, has been added for temperature compensation of this biasing. Now, if we include these biasing resistors, we have a DC amplifier with the input biased at approximately zero volts. If feedback resistors are added around this biased amplifier we get the schematic shown in Figure 77.



*COMPLEMENTARY TRACKING

FIGURE 76. DC Biasing for ± 15 V_{DC} Operation

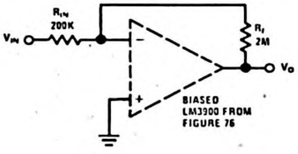


FIGURE 77. A DC Amplifier Operating with ± 15 V_{DC}

This is a standard inverting DC amplifier connection. The (+) input is "effectively" at ground and the biasing shown in Figure 76 is used to take care of DC levels at the inputs.

10.3 Tachometers

Many pulse averaging tachometers can be built using the LM3900. Inputs can be voltage pulses, current pulses or the differentiated transitions of squarewaves. The DC output voltage can be made to increase with increasing input frequency, can be made proportional to twice the input frequency (frequency doubling for reduced output ripple), and can also be made proportional to either the sum or the difference between two input frequencies. Due to the small bias current and the high gain of the LM3900, the transfer function is linear between the saturation states of the amplifier.

10.3.1 A Basic Tachometer

If an RC averaging network is added from the output to the (-) input, the basic tachometer of Figure 78 results Current pulse inputs will provide the desired transfer function shown on the figure. Each input current pulse causes a small change in the output voltage. Neglecting the effects of R we have

$$\Delta V_O \cong \frac{I \Delta t}{C}$$

The inclusion of R gives a discharge path so the output voltage does not continue to integrate, but rather provides the time dependency which is necessary to average the input pulses. If an additional signal source is simply placed in parallel with the one shown, the output becomes proportional to the sum of these input frequencies. If this additional source were applied to the (-) input, the output voltage would be proportional to the difference between these input frequencies. Voltage pulses can be converted to current pulses by using an input resistor. A series isolating diode should be used if

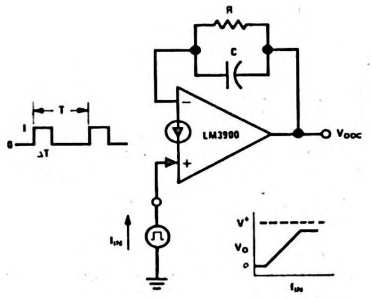


FIGURE 78. A Basic Tachometer

a signal is applied to the (-) input to prevent loading during the low voltage state of this input signal.

10.3.2 Extending V_{OUT} (Minimum) to Ground

The output voltage of the circuit of Figure 78 does not go to ground level but has a minimum value which is equal to the V_{BE} of the (-) input (0.5 V_{DC}). If it is desired that the output voltage go exactly to ground, the circuit of Figure 79 can be used. Now with $V_{IN} = 0\ V_{DC}$, $V_O = 0V_{DC}$ due to the addition of the common-mode biasing resistors (180 kΩ). The diode, CR$_1$, allows the output to go below $V_{CE\ SAT}$ of the output, if desired (a load is required to provide a DC path for the biasing current flow via the R of the averaging network).

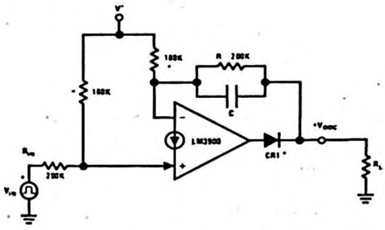


FIGURE 79. Adding Biasing to Provide $V_O = 0\ V_{DC}$

10.3.3 A Frequency Doubling Tachometer

To reduce the ripple on the DC output voltage, the circuit of Figure 80 can be used to effectively double the input frequency. Input pulses are not required, a squarewave is all that is needed. The operation of the circuit is to average the charge and discharge transient currents of the input capacitor, C_{IN}. The resistor, R_{IN}, is used to convert the voltage pulses to current pulses and to limit the surge currents (to approximately 200 μA peak—or less if operating at high temperatures). When the input voltage goes high, the charging current of C_{IN}, I_{CHG} enters the (+) input, is mirrored about ground and is drawn from the RC averaging network into the (-) input terminal. When the input voltage goes back to ground, the discharge current of C_{IN}, $I_{DISCHARGE}$ will also be drawn from the RC averaging network via the now conducting diode, CR$_1$. This full wave action causes two current pulses to be drawn through the RC averaging network for each cycle of the input frequency.

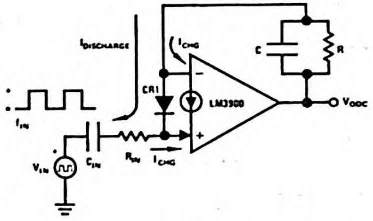


FIGURE 80. A Frequency Doubling Tachometer

10.4 A Squaring Amplifier

A squaring amplifier which incorporates symmetrical hysteresis above and below the zero output state (for noise immunity) is often needed to amplify the low level signals which are provided by variable reluctance transducers. In addition, a high frequency roll-off (low pass characteristic) is desirable both to reduce the natural voltage buildup at high frequencies and to also filter high frequency input noise disturbances. A simple circuit which accomplishes this function is shown in Figure 81. The input voltage is converted to input currents by using the input resistors, R_{IN}. Common-mode biasing is provided by R_{B1} and R_{B2}. Finally positive feedback (hysteresis) is provided by R_f. The large source resistance, R_{IN}, provides a low pass filter due to the "Miller-effect" input capacitance of the amplifier (approximately 0.002 μF). The amount of hysteresis and the symmetry about the zero volt input are controlled by the positive feedback resistor, R_f, and R_{B1} and R_{B2}.

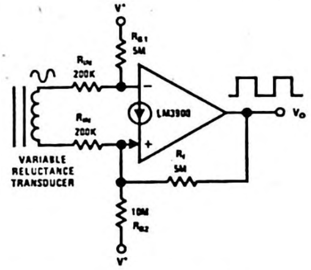


FIGURE 81. A Squaring Amplifier with Hysteresis

With the values shown in Figure 81 the trip voltages are approximately ±150 mV centered about the zero output voltage state of the transducer (at low frequencies where the low pass filter is not attenuating the input signal).

10.5 A Differentiator

An input differentiating capacitor can cause the input of the LM3900 to swing below ground and actuate the input clamp circuit. Again, common-mode biasing can be used to prevent this negative swing at the input terminals of the LM3900. The schematic of a differentiator circuit is shown in Figure 82. Common-mode biasing is provided by R_{B1} and R_{B2}. The feedback resistor, R_f, is one-half the value of R_{IN} so the gain is 1/2. The output voltage will bias at $V^+/2$ which thereby allows both a positive and a negative swing above and below this bias point. The resistor, R_{IN}, keeps the negative swing isolated from the (-) input terminal and therefore both inputs remain biased at $+V_{BE}$ . .

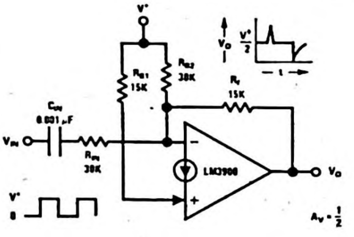


FIGURE 82. A Differentiator Circuit

10.6 A Difference Integrator

A difference integrator is the basis of many of the sweep circuits which can be realized using the LM3900 operating on only a single power supply voltage. This circuit can also be used to provide the time integral of the difference between two input waveforms. The schematic of the difference integrator is shown in Figure 83.

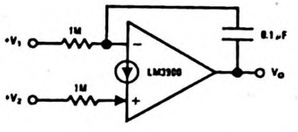


FIGURE 83. A Difference Integrator

This is a useful component for DC feedback loops as both the comparison to a reference and the integration take place in one amplifier.

10.7 A Low Drift Sample and Hold Circuit

In sample and hold applications a very low input biasing current is required. This is usually achieved by using a FET transistor or a special low input current IC op amp. The existance of many matched amplifiers in the same package allows the LM3900 to provide some interesting low "equivalent" input biasing current applications.

10.7.1 Reducing the "Effective" Input Biasing Current

One amplifier can be used to bias one or more additional amplifiers as shown in Figure 84.

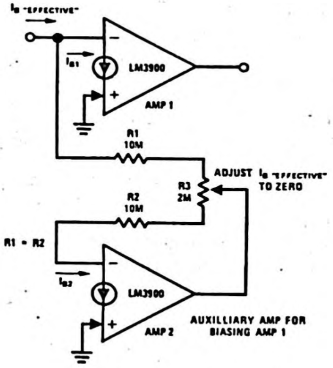


FIGURE 84. Reducing I_B "Effective" to Zero

The input terminal of Amp. 1 will only need to supply the signal current if the DC biasing current, I_{B1}, is accurately supplied via R_1. The adjustment, R_3, allows a zeroing of "I_B effective" but simply omitting R_3 and letting $R_1 = R_2$ (and relying on amplifier symmetry) can cause I_B "effective" to be less than $I_B/10$ (3 nA). This is useful in circuit applications such as sample and hold, where small values of I_B "effective" are desirable.

10.7.2 A Low Drift Ramp and Hold Circuit

The input current reduction technique of the previous section allows a relatively simple ramp and hold circuit to be built which can be ramped up or down or allowed to remain at any desired output DC level in a "hold" mode. This is shown in Figure 85. If both inputs are at 0 V_{DC} the circuit is in a hold mode. Raising either input will cause the DC output voltage to ramp either up or down depending on which one goes positive. The slope is a function of the magnitude of the input voltage and additional inputs can be placed in parallel, if desired, to increase the input control variables.

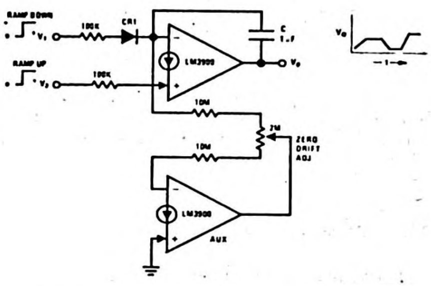


FIGURE 85. A Low-drift Ramp and Hold Circuit

10.7.3 Sample-hold and Compare with New $+V_{IN}$

An example of using the circuit of the previous section is shown in Figure 86 where clamping transistors, Q_1 and Q_2, put the circuit in a hold mode when they are driven ON. When OFF the output voltage of Amp. 1 can ramp either up or down as needed to guarantee that the output voltage of Amp. 1 is equal to the DC input voltage which is applied to Amp. 3. Resistor R_1 provides a fixed "down" ramp current which is balanced or controlled via the comparator, Amp. 3, and the resistor R_4. When Q_1 and Q_2 are OFF a feedback loop guarantees that V_{01} (from Amp. 1) is equal to $+V_{IN}$ (to Amp. 3). Amplifier 2 is used to supply the input biasing current to Amp. 1.

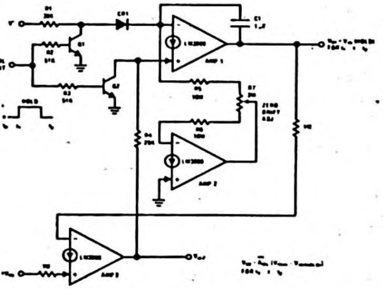


FIGURE 86. Sample-hold and Compare with New $+V_{IN}$

The stored voltage appears at the output, V_{01} of Amp. 1, and as Amp. 3 is active, a continued comparison is made between V_{01} and V_{IN} and the output of Amp. 3 fully switches based on this comparison. A second loop could force V_{IN} to be maintained at the stored value (V_{01}) by making use of V_{02} as an error signal for this second loop. Therefore, a control system could be manually controlled to bring it to a particular operating condition; then, by exercising the hold control, the system would maintain this operating condition due to the analog memory provided by V_{01}.

10.8 Audio Mixer or Channel Selector

The multiple amplifiers of the LM3900 can be used for audio mixing (many amplifiers simultaneously providing signals which are added to generate a composite output signal) or for channel selection (only one channel enabled at a time). Three amplifiers are shown being summed into a fourth amplifier in Figure 87.

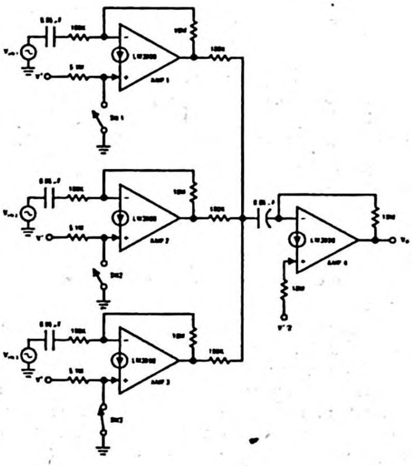


FIGURE 87. Audio Mixing or Selection

If a power amplifier were available, all four amplifiers could feed the single input of the power amplifier. For audio mixing all amplifiers are simulatneously active. Particular amplifiers can be gated OFF by making use of DC control signals which are applied to the (+) inputs to provide a channel select feature. As shown on Figure 87, Amp. 3 is active (as sw 3 is closed) and Amps. 1 and 2 are driven to positive output voltage saturation by the 5.1M which is applied to the (+) inputs. The DC output voltage bias level of the active amplifier is approximately 0.8 V_{DC} and could be raised if larger signal levels were to be accommodated. Frequency shaping networks can be added either to the individual amplifiers or to the common amplifier, as desired. Switching transients may need to be filtered at the DC control points if the output amplifier is active during the switching intervals.

10.9 A Low Frequency Mixer

The diode which exists at the (+) input can be used for non-linear signal processing. An example of this is a mixer which allows two input frequencies to produce a sum and difference frequency (in addition to other high frequency components). Using the amplifier of the LM3900, gain and filtering can also be accomplished with the same circuit in addition to the high input impedance and low output impedance advantages. The schematic of Figure 88 shows a mixer with a gain of 10 and a low pass single pole filter (1M and 150 pF feedback elements) with a corner frequency of 1 kHz. With one signal larger in amplitude, to serve as the local oscillator input (V_1), the transconductance of the input diode is gated at this rate (f_1). A smaller signal (V_2) can now be added at the second input and the difference frequency is filtered from the composite resulting waveform and is made available at the output. Relatively high frequencies can be applied at the inputs as long as the desired difference frequency is within the bandwidth capabilities of the amplifier and the RC low pass filter.

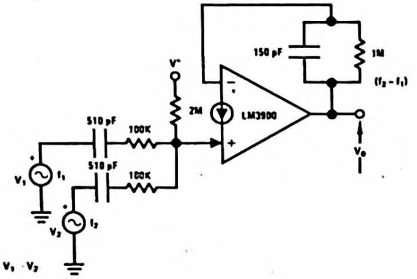


FIGURE 88. A Low Frequency Mixer

10.10 A Peak Detector

A peak detector is often used to rapidly charge a capacitor to the peak value of an input waveform. The voltage drop across the rectifying diode is placed within the feedback loop of an op amp to prevent voltage losses and temperature drifts in the output voltage. The LM3900 can be used as a peak detector as shown in Figure 89. The feedback resistor, R_f, is kept small (1 MΩ) so that the 30 nA base current will cause only a +30 mV error in V_O. This feedback resistor is constantly loading C in addition to the current drawn by the circuitry which samples V_O. These loading effects must be considered when selecting a value for C.

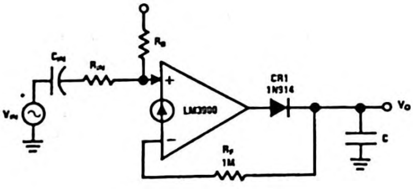


FIGURE 89. A Peak Detector

The biasing resistor, R_B, allows a minimum DC voltage to exist across the capacitor and the input resistor, R_{IN}, can be selected to provide gain to the input signal.

10.11 Power Circuits

The amplifier of the LM3900 will source a maximum current of approximately 10 mA and will sink maximum currents of approximately 80 mA (if overdriven at the (−) input). If the output is driven to a saturated state to reduce device dissipation, some interesting power circuits can be realized. These maximum values of current are typical values for the unit operating at 25°C and therefore have to be de-rated for reliable operation. For fully switched operation, amplifiers can be paralleled to increase current capability.

10.11.1 Lamp and/or Relay Drivers (≤ 30 mA)

Low power lamps and relays (as reed relays) can be directly controlled by making use of the larger value of sink current than source current. A schematic is shown in Figure 90 where the input resistor, R, is selected such that V_{IN} supplies at least 0.1 mA of input current.

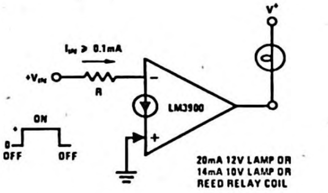


FIGURE 90. Sinking 20 to 30 mA Loads

10.11.2 Lamp and/or Relay Drivers (≤ 300 mA)

To increase the power capability, an external transistor can be added as shown in Figure 91. The resistors R_1 and R_2 hold Q_1 OFF when the output of the LM3900 is high. The resistor, R_2, limits the base drive when Q_1 goes ON. It is required that pin 14 tie to the same power supply as the emitter of Q_1 to guarantee that Q_1 can be held OFF. If an inductive load is used, such as a relay coil, a backswing diode should be added to prevent large inductive voltage kicks during the switching interval, ON to OFF.

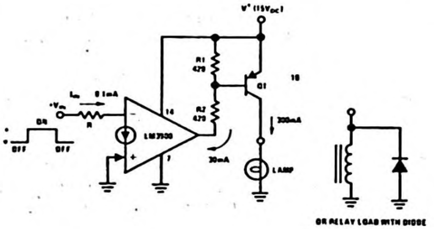

V+ (15VDC)
R1
470
R2
470
Q1
10
Iin
0.1mA
+Vin
R
ON
OFF
OFF
LM3900
14
7
30mA
300mA
LAMP
OR RELAY LOAD WITH DIODE

FIGURE 91. Boosting to 300 mA Loads

10.11.3 Positive Feedback Oscillators

If the LM3900 is biased into the active region and a resonant circuit is connected from the output to the (+) input, a positive feedback oscillator results. A driver for a piezoelectric transducer (a warning type of noise maker) is shown in Figure 92. The resistors R_1 and R_2 bias the output voltage at $V^+/2$ and keep the amplifier active. Large currents can be entered into the (+) input and negative currents (or currents out of this terminal) are provided by the epi-substrate diode of the IC fabrication.

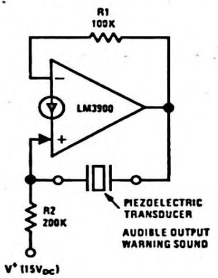

R1
100K
LM3900
R2
200K
V+ (15VDC)
PIEZOELECTRIC TRANSDUCER
AUDIBLE OUTPUT WARNING SOUND

FIGURE 92. Positive Feedback Power Oscillators

When one of the amplifiers is operated in this large negative input current mode, the other amplifiers will be disturbed due to interaction. Multiple sounds may be generated as a result of using two or more transducers in various combinations, but this has not been investigated. Other two-terminal RC, RLC or piezoelectric resonators can be connected in this circuit to produce an oscillator.

10.12 High Voltage Operation

The amplifiers of the LM3900 can drive an external high voltage NPN transistor to provide a larger output voltage swing (as for an electrostatic CRT deflection system) or to operate off of an existing high voltage power supply (as the +98 V_{DC} rectified line). Examples of both type of circuits are presented in this section.

10.12.1 A High Voltage Inverting Amplifier

An inverting amplifier with an output voltage swing from essentially 0 V_{DC} to +300 V_{DC} is shown in Figure 93. The transistor, Q_1, must be a high breakdown device as it will have the full HV supply across it. The biasing resistor R_3 is used to center the transfer characteristic and the gain is the ratio of R_2 to R_1. The load resistor, R_L, can be increased, if desired, to reduce the HV current drain.

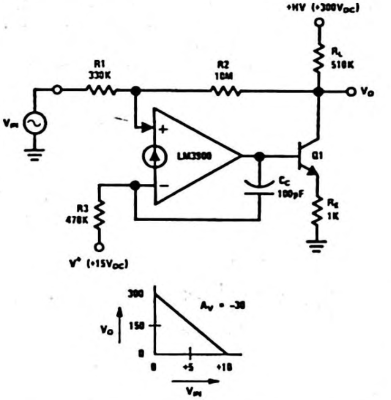

+HV (+300VDC)
RL
510K
R1
330K
R2
10M
Vo
Vin
LM3900
Q1
CC
100pF
RE
1K
R3
470K
V+ (+15VDC)
300
150
0
Vo
AV = -30
0
+5
+10
Vin

FIGURE 93. A High Voltage Inverting Amplifier

10.12.2 A High Voltage Non-inverting Amplifier

A high voltage non-inverting amplifier is shown in Figure 94. Common-mode biasing resistors (R_2) are used to allow V_{IN} to go to 0 V_{DC}. The output voltage, V_O, will not actually go to zero due to R_E, but should go to approximately

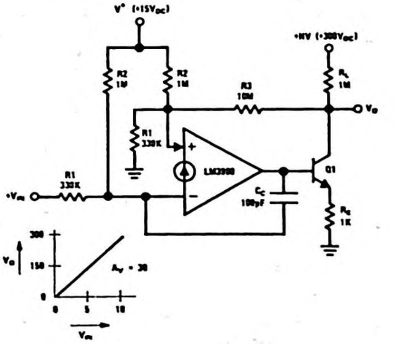

V+ (+15VDC)
+HV (+300VDC)
R2
1M
R2
1M
R3
10M
RL
1M
Vo
R1
330K
LM3900
Q1
R1
330K
+Vin
CC
100pF
RE
1K
300
150
0
Vo
AV = 30
0
5
10
Vin

FIGURE 94. A High Voltage Non-inverting Amplifier

0.3 V_{DC}. Again, the gain is 30 and a range of the input voltage of from 0 to +10 V_{DC} will cause the output voltage to range from approximately 0 to +300 V_{DC}.

10.12.3 A Line Operated Audio Amplifier

An audio amplifier which operates off a +98 V_{DC} power supply (the rectified line voltage) is often used in consumer products. The external high voltage transistor, Q_1 of Figure 95, is biased and controlled by the LM3900. The magnitude of the DC biasing voltage which appears across the emitter resistor of Q_1 is controlled by the resistor which is placed from the (-) input to ground.

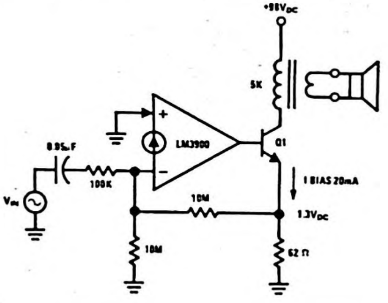


FIGURE 95. A Line Operated Audio Amplifier

10.13 A Dual-channel Class-A Driver for Auto Radios

A germanium power transistor is widely used in automotive class A audio amplifiers. As shown in Figure 96, two amplifiers can be cascaded to bias and to control the 2N176 power transistor. This circuit has many advantages over the standard discrete circuit which is used as:

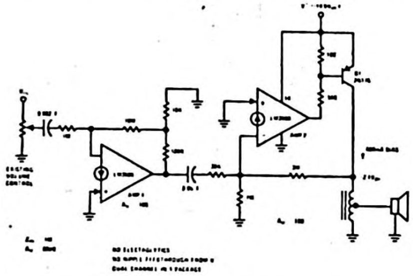


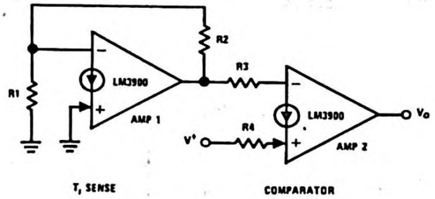
FIGURE 96. A Dual-channel IC Driver for Class A Car Radios

1.) No electrolytic capacitors are used.
2.) The ripple on the power supply line is rejected.
3.) The input impedance is high (1 MΩ).
4.) A large closed loop gain is easily achieved (80 dB).
5.) The slow start-up delay is eliminated.
6.) Two channels are available in one package.

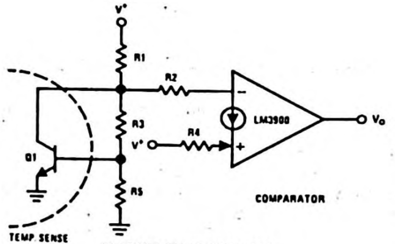
Again, the pin 14 voltage must be at least as high as the power supply used at the emitter of Q_1 to guarantee an OFF control for Q_1.

10.14 Temperature Sensing

The LM3900 can be used to monitor the junction temperature of the monolithic chip as shown in Figure 97(a). Amp. 1 will generate an output voltage which can be designed to undergo a large negative temperature change by design of R_1 and R_2. The second amplifier compares this temperature dependent voltage with the power supply voltage and goes high at a designed maximum T_j of the IC.



(a) IC T_j MONITOR



(b) REMOTE TEMPERATURE SENSE

FIGURE 97. Temperature Sensing

For remote sensing, an NPN transistor, Q_1 of Figure 97(b), is connected as an N V_{BE} generator (with R_3 and R_5) and is biased via R_1 from the power supply voltage, V^+. The LM3900 again compares this temperature dependent voltage with the supply voltage and can be designed to have V_O go high at a maximum temperature of the remote temperature sensor, Q_1.

10.15 A "Programmable Unijunction"

If a diode is added to the Schmitt-trigger, a "programmable unijunction" function can be obtained as shown in Figure 98. For a low input voltage, the output voltage of the LM3900 is high and CRI is OFF. When the input voltage rises to the high trip voltage, the output falls to essentially 0V and CRI goes ON to discharge the input capacitor, C. The low trip voltage must be larger than approximately 1V to guarantee that the forward drop of CRI added to the output voltage of the LM3900 will be less than the low trip voltage. The discharge current can be increased by using smaller values for R_2 to provide pull down currents larger than the 1.3 mA bias current source. The trip voltages of the Schmitt-Trigger are designed as shown in section 9.7.

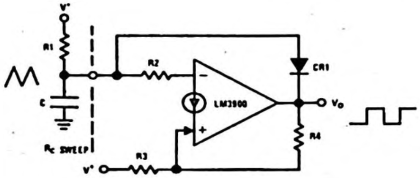


FIGURE 98. A "Programmable Unijunction"

10.16 Adding a Differential Input Stage

A differential amplifier can be added to the input of the LM3900 as shown in Figure 99.

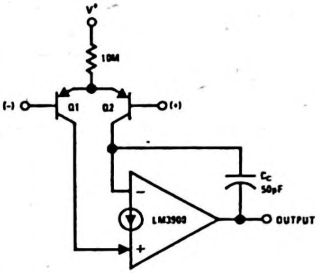


FIGURE 99. Adding a Differential Input Stage

This will increase the gain and reduce the offset voltage. Frequency compensation can be added as shown. The BV_{EBO} limit of the input transistors must not be exceeded during a large differential input condition, or diodes and input limiting resistors should be added to restrict the input voltage which is applied to the bases of Q_1 and Q_2 to $\pm V_D$.

The input common-mode voltage range does not go exactly to ground as a few tenths of a volt are needed to guarantee that Q_1 or Q_2 will not saturate and cause a phase change (and a resulting latch-up). The input currents will be small, but could be reduced further, if desired, by using FETS for Q_1 and Q_2. This circuit can also be operated off of $\pm 15\ V_{DC}$ supplies.

LM139/LM239/LM339 — A Quad of Independently Functioning Comparators

National Semiconductor
Application Note 74
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INTRODUCTION

The LM139/LM239/LM339 family of devices is a monolithic quad of independently functioning comparators designed to meet the needs for a medium speed, TTL compatible comparator for industrial applications. Since no antisaturation clamps are used on the output such as a Baker clamp or other active circuitry, the output leakage current in the OFF state is typically 0.5 nA. This makes the device ideal for system applications where it is desired to switch a node to ground while leaving it totally unaffected in the OFF state.

Other features include single supply, low voltage operation with an input common mode range from ground up to approximately one volt below V_{CC}. The output is an uncommitted collector so it may be used with a pull-up resistor and a separate output supply to give switching levels from any voltage up to 36V down to a $V_{CE\,SAT}$ above ground (approx. 100 mV), sinking currents up to 15 mA. In addition it may be used as a single pole switch to ground, leaving the switched node unaffected while in the OFF state. Power dissipation with all four comparators in the OFF state is typically 4 mW from a single 5V supply (1 mW/comparator).

CIRCUIT DESCRIPTION

Figure 1 shows the basic input stage of one of the four comparators of the LM139. Transistors Q_1 through Q_4 make up a PNP Darlington differential input stage with Q_5 and Q_6 serving to give single-ended output from differential input with no loss in gain. Any differential input at Q_1 and Q_4 will be amplified causing Q_6 to switch OFF or ON depending on input signal polarity. It can easily be seen that operation with an input common mode voltage of ground is possible. With both inputs at ground potential, the emitters of Q_1 and Q_4 will be at one V_{BE} above ground and the emitters of Q_2 and Q_3 at 2 V_{BE}. For switching action the base of Q_5 and Q_6 need only go to one V_{BE} above ground and since Q_2 and Q_3 can operate with zero volts collector to base, enough voltage is present at a zero volt common mode input to insure comparator action. The bases should not be taken more than several hundred millivolts below ground, however, to prevent forward biasing a substrate diode which would stop all comparator action and possibly damage the device. If very large input currents were provided.

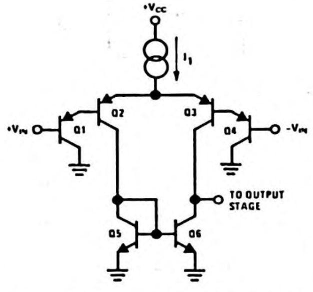


FIGURE 1. Basic LM139 Input Stage

Figure 2 shows the comparator with the output stage added. Additional voltage gain is taken through Q_7 and Q_8 with the collector of Q_8 left open to offer a wide variety of possible applications. The addition of a large pull-up resistor from the collector of Q_8 to either $+V_{CC}$ or any other supply up to 36V both increases the LM139 gain and makes possible output switching levels to match practically any application. Several outputs may be tied together to provide an ORing function or the pull-up resistor may be omitted entirely with the comparator then serving as a SPST switch to ground.

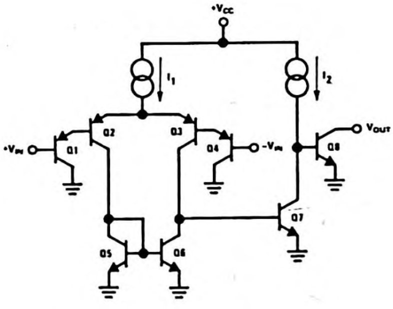


FIGURE 2. Basic LM139 Comparator

Output transistor Q_8 will sink up to 15 mA before the output ON voltage rises above several hundred millivolts. The output current sink capability may be boosted by the addition of a discrete transistor at the output.

The complete circuit for one comparator of the LM139 is shown in Figure 3. Current sources I_3 and I_4 are added to help charge any parasitic capacitance at the emitters of Q_1 and Q_4 to improve the slew rate of the input stage. Diodes D_1 and D_2 are added to speed up the voltage swing at the emitters of Q_1 and Q_2 for large input voltage swings.

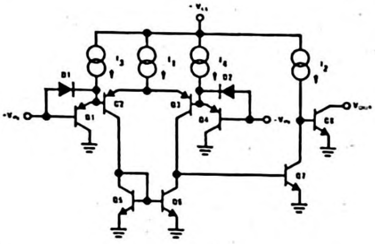


FIGURE 3. Complete LM139 Comparator Circuit

Biasing for current sources I_1 through I_4 is shown in Figure 4. When power is first applied to the circuit, current flows through the JFET Q_{13} to bias up diode D_5. This biases transistor Q_{12} which turns ON transistors Q_9 and Q_{10} by allowing a path to ground for their base and collector currents.

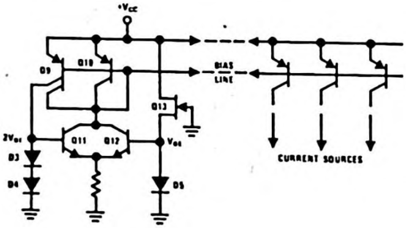


FIGURE 4. Current Source Biasing Circuit

Current from the left hand collector of Q_9 flows through diodes D_3 and D_4 bringing up the base of Q_{11} to 2 V_{BE} above ground and the emitters of Q_{11} and Q_{12} to one V_{BE}. Q_{12} will then turn OFF because its base emitter voltage goes to zero. This is the desired action because Q_9 and Q_{10} are biased ON through Q_{11}, D_3 and D_4 so Q_{12} is no longer needed. The "bias line" is now sitting at a V_{BE} below $+V_{CC}$ which is the voltage needed to bias the remaining current sources in the LM139 which will have a constant bias regardless of $+V_{CC}$ fluctuations. The upper input common mode voltage is V_{CC} minus the saturation voltage of the current sources (approximately 100 mV) minus the 2 V_{BE} of the input devices Q_1 and Q_2 (or Q_3 and Q_4).

COMPARATOR CIRCUITS

Figure 5 shows a basic comparator circuit for converting low level analog signals to a high level digital output. The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. Resistors R_1 and R_2 are used to set the input threshold trip voltage (V_{REF}) at any value desired within the input common mode range of the comparator.

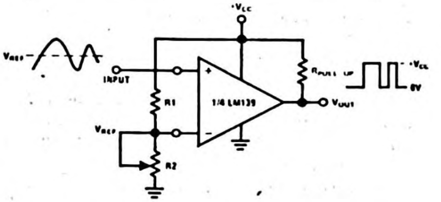


FIGURE 5. Basic Comparator Circuit

Comparators with Hysteresis

The circuit shown in Figure 5 suffers from one basic drawback in that if the input signal is a slowly varying low level signal, the comparator may be forced to stay within its linear region between the output high and low states for an undesireable length of time. If this happens, it runs the risk of oscillating since it is basically an uncompensated, high gain op amp. To prevent this, a small amount of positive feedback or hysteresis is added around the comparator. Figure 6 shows a comparator with a small amount of positive feedback. In order to insure proper comparator action, the components should be chosen as follows:

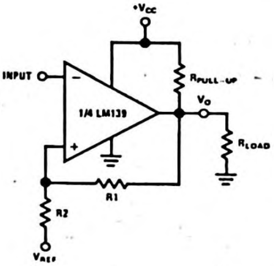


FIGURE 6. Comparator with Positive Feedback to Improve Switching Time

$$R_{PULL\text{-}UP} < R_{LOAD} \text{ and}$$

$$R_1 > R_{PULL\text{-}UP}$$

This will insure that the comparator will always switch fully up to $+V_{CC}$ and not be pulled down by the load or feedback. The amount of feedback is chosen arbitrarily to insure proper switching with the particular type of input signal used. If the output swing is 5V, for example, and it is desired to feedback 1% or 50 mV, then $R_1 \approx 100\ R_2$. To describe circuit operation, assume that the inverting input goes above the reference input ($V_{IN} > V_{REF}$). This will drive the output, V_O, towards ground which in turn pulls V_{REF} down through R_1. Since V_{REF} is actually the non-inverting input to the comparator, it too will drive the output towards ground insuring the fastest possible switching time regardless of how slow the input moves. If the input then travels down to V_{REF}, the same procedure will occur only in the opposite direction insuring that the output will be driven hard towards $+V_{CC}$.

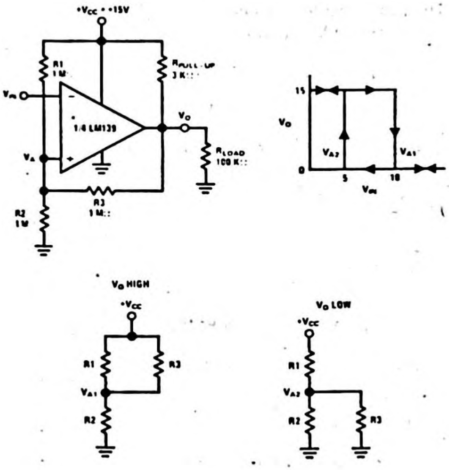


FIGURE 7. Inverting Comparator with Hysteresis

Putting hysteresis in the feedback loop of the comparator has far more use, however, than simply as an oscillation suppressor. It can be made to function as a Schmitt trigger with presettable trigger points. A typical circuit is shown in Figure 7. Again, the hysteresis is achieved by shifting the reference voltage at the positive input when the output voltage V_O changes state. This network requires only three resistors and is referenced to the positive supply $+V_{CC}$ of the comparator. This can be modeled as a resistive divider, R_1 and R_2, between $+V_{CC}$ and ground with the third resistor, R_3, alternately connected to $+V_{CC}$ or ground, paralleling either R_1 or R_2. To analyze this circuit, assume that the input voltage, V_{IN}, at the inverting input is less than V_A. With $V_{IN} \leq V_A$ the output will be high ($V_O = +V_{CC}$). The upper input trip voltage, V_{A1}, is defined by:

$$V_{A1} = \frac{+V_{CC}\ R_2}{(R_1 \| R_3) + R_2}$$

or

$$V_{A1} = \frac{+V_{CC}\ R_2\ (R_1 + R_3)}{R_1\ R_2 + R_1\ R_3 + R_2\ R_3} \qquad (1)$$

When the input voltage V_{IN}, rises above the reference voltage ($V_{IN} > V_{A1}$), voltage, V_O, will go low (V_O = GND). The lower input trip voltage, V_{A2}, is now defined by:

$$V_{A2} = \frac{+V_{CC}\ R_2 \| R_3}{R_1 + R_2 \| R_3}$$

or

$$V_{A2} = \frac{+V_{CC}\ R_2\ R_3}{R_1\ R_2 + R_1\ R_3 + R_2\ R_3} \qquad (2)$$

When the input voltage, V_{IN}, decreases to V_{A2} or lower, the output will again switch high. The total hysteresis, ΔV_A, provided by this network is defined by:

$$\Delta V_A = V_{A1} - V_{A2}$$

or, subtracting equation 2 from equation 1

$$\Delta V_A = \frac{+V_{CC}\ R_1\ R_2}{R_1\ R_2 + R_1\ R_3 + R_2\ R_3} \qquad (3)$$

To insure that V_O will swing between $+V_{CC}$ and ground, choose:

$$R_{PULL\text{-}UP} < R_{LOAD} \text{ and} \qquad (4)$$

$$R_3 > R_{PULL\text{-}UP} \qquad (5)$$

Heavier loading on $R_{PULL\text{-}UP}$ (i.e. smaller values of R_3 or R_{LOAD}) simply reduces the value of the maximum output voltage thereby reducing the amount of hysteresis by lowering the value of V_{A1}. For simplicity, we have assumed in the above equations that V_O high switches all the way up to $+V_{CC}$.

To find the resistor values needed for a given set of trip points, we first divide equation (3) by equation (2). This gives us the ratio:

$$\frac{\Delta V_A}{V_{A2}} = \frac{1 + \dfrac{R_1}{R_3} + \dfrac{R_1}{R_2}}{1 + \dfrac{R_3}{R_2} + \dfrac{R_3}{R_1}} \qquad (6)$$

If we let $R_1 = n\ R_3$, equation (6) becomes:

$$\frac{\Delta V_A}{V_{A2}} = n \qquad (7)$$

We can then obtain an expression for R_2 from equation (1) which gives

$$R_2 = \frac{R_1 \| R_3}{\dfrac{+V_{CC}}{V_{A1}} - 1} \qquad (8)$$

The following design example is offered:

Given: $V^+ = +15V$
$R_{LOAD} = 100\ k\Omega$
$V_{A1} = +10V$
$V_{A2} = +5V$

To find: R_1, R_2, R_3, $R_{PULL\text{-}UP}$

Solution:

From equation (4) $R_{PULL\text{-}UP} < R_{LOAD}$
$R_{PULL\text{-}UP} < 100\ k\Omega$
so let $R_{PULL\text{-}UP} = 3\ k\Omega$

From equation (5) $R_3 > R_{LOAD}$
$R_3 > 100 k\Omega$
so let $R_3 = 1\ M\Omega$

From equation (7) $n = \frac{\Delta V_A}{V_{A2}} = \frac{10-5}{5} = 1$

and since $R_1 = nR_3$
this gives $R_1 = 1R_3 = 1\ M\Omega$

From equation (8) $R_2 = \frac{500\ k\Omega}{\frac{15}{10} - 1} = 1\ M\Omega$

These are the values shown in Figure 7.

The circuit shown in Figure 8 is a non-inverting comparator with hysteresis which is obtained with only two resistors, R_1 and R_2. In contrast to the first method, however, this circuit requires a separate reference voltage at the negative input. The trip voltage, V_A, at the positive input is shifted about V_{REF} as V_O changes between $+V_{CC}$ and ground.

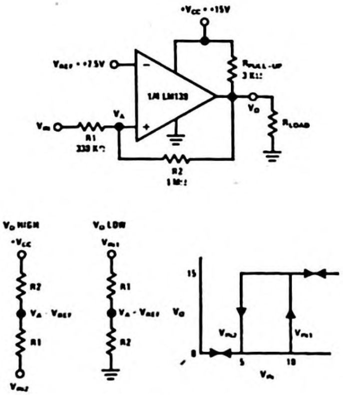


FIGURE 8. Non-Inverting Comparator with Hysteresis

Again for analysis, assume that the input voltage, V_{IN}, is low so that the output, V_O, is also low (V_O = GND). For the output to switch, V_{IN} must rise up to $V_{IN\ 1}$ where $V_{IN\ 1}$ is given by:

$$V_{IN\ 1} = \frac{V_{REF}\ (R_1 + R_2)}{R_2} \qquad (9)$$

As soon as V_O switches to $+V_{CC}$, V_A will step to a value greater than V_{REF} which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN\ 1})R_1}{R_1 + R_2} \qquad (10)$$

To make the comparator switch back to its low state (V_O = GND) V_{IN} must go below V_{REF} before V_A will again equal V_{REF}. This lower trip point is now given by:

$$V_{IN\ 2} = \frac{V_{REF}\ (R_1 + R_2) - V_{CC}\ R_1}{R_2} \qquad (11)$$

The hysteresis for this circuit, ΔV_{IN}, is the difference between $V_{IN\ 1}$ and $V_{IN\ 2}$ and is given by:

$$\Delta V_{IN} = V_{IN\ 1} - V_{IN\ 2} =$$

$$\frac{V_{REF}\ (R_1 + R_2)}{R_2} - \frac{V_{REF}\ (R_1 + R_2) - V_{CC}\ R_1}{R_2}$$

or

$$\Delta V_{IN} = \frac{V_{CC}\ R_1}{R_2} \qquad (12)$$

As a design example consider the following:

Given: $R_{LOAD} = 100\ k\Omega$
$V_{IN\ 1} = 10V$
$V_{IN\ 2} = 5V$
$+V_{CC} = 15V$

To find: V_{REF}, R_1, R_2 and R_3

Solution:

Again choose $R_{PULL\text{-}UP} < R_{LOAD}$ to minimize loading, so let

$$R_{PULL\text{-}UP} = 3\ k\Omega$$

From equation (12) $\frac{R_1}{R_2} = \frac{\Delta V_{IN}}{V_{CC}}$

$$\frac{R_1}{R_2} = \frac{10-5}{15} = \frac{1}{3}$$

$$R_1 = \frac{R_2}{3}$$

From equation (9) $V_{REF} = \frac{10}{1 + \frac{R_1}{R_2}}$

$$V_{REF} = \frac{V_{IN}}{1 + \frac{1}{3}} = 7.5V$$

To minimize output loading choose

$$R_2 > R_{PULL\text{-}UP}$$

or $$R_2 > 3\ k\Omega$$

so let $$R_2 = 1\ M\Omega$$

The value of R_1 is now obtained from equation (12)

$$R_1 = \frac{R_2}{3}$$

$$R_1 = \frac{1\ M\Omega}{3} \cong 330\ k\Omega$$

These are the values shown in Figure 8.

Limit Comparator with Lamp Driver

The limit comparator shown in Figure 9 provides a range of input voltages between which the output devices of both LM139 comparators will be OFF.

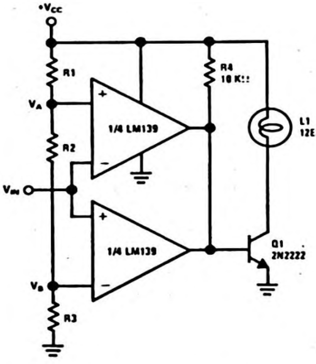


FIGURE 9. Limit Comparator with Lamp Driver

This will allow base current for Q_1 to flow through pull-up resistor R_4, turning ON Q_1 which lights the lamp. If the input voltage, V_{IN}, changes to a value greater than V_A or less than V_B, one of the comparators will switch ON, shorting the base of Q_1 to ground, causing the lamp to go OFF. If a PNP transistor is substituted for Q_1 (with emitter tied to $+V_{CC}$) the lamp will light when the input is above V_A or below V_B. V_A and V_B are arbitrarily set by varying resistors R_1, R_2 and R_3.

Zero Crossing Detector

The LM139 can be used to symmetrically square up a sine wave centered around zero volts by incorporating a small amount of positive feedback to improve switching times and centering the input threshold at ground (see Figure 10). Voltage divider R_4 and R_5 establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$. The positive feedback resistor, R_6, is made very large with respect to R_5 ($R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10\ mV$) but it is sufficient to insure rapid output voltage transitions. Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

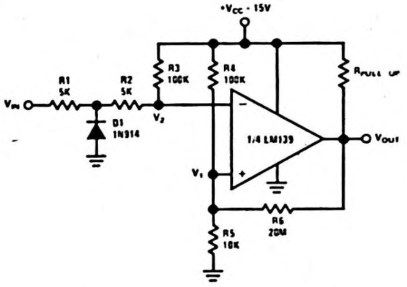


FIGURE 10. Zero Crossing Detector

Comparing the Magnitude of Voltages of Opposite Polarity

The comparator circuit shown in Figure 11 compares the magnitude of two voltages, $V_{IN\ 1}$ and $V_{IN\ 2}$ which have opposite polarities. The resultant input voltage at the minus input terminal to the comparator, V_A, is a function of the voltage divider from $V_{IN\ 1}$ and $V_{IN\ 2}$ and the values of R_1 and R_2. Diode connected transistor Q_1 provides protection for the minus input terminal by clamping it at several hundred millivolts below ground. A 2N2222 was chosen over a 1N914 diode because of its lower diode voltage. If desired, a small amount of hysteresis may be added using the techniques described previously. Correct magnitude comparison can be seen as follows: Let $V_{IN\ 1}$ be the input for the positive polarity input voltage and $V_{IN\ 2}$ the input for the negative polarity. If the magnitude of $V_{IN\ 1}$ is greater than that

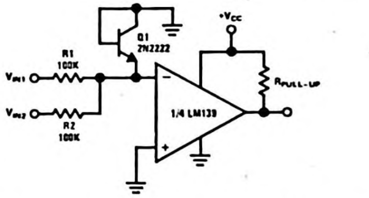


FIGURE 11. Comparing the Magnitude of Voltages of Opposite Polarity

of $V_{IN\,2}$ the output will go low (V_{OUT} = GND). If the magnitude of $V_{IN\,1}$ is less than that of $V_{IN\,2}$, however, the output will go high ($V_{OUT} = V_{CC}$).

Magnetic Transducer Amplifier

A circuit that will detect the zero crossings in the output of a magnetic transducer is shown in Figure 12. Resistor divider, R_1 and R_2, biases the positive input at $+V_{CC}/2$, which is well within the common mode operating range. The minus input is biased through the magnetic transducer. This allows large signal swings to be handled without exceeding the input voltage limits. A symmetrical square wave output is insured through the positive feedback resistor R_3. Resistors R_1 and R_2 can be used to set the DC bias voltage at the positive input at any desired voltage within the input common mode voltage range of the comparator.

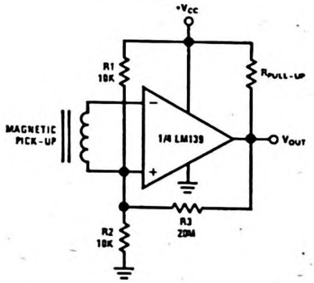


FIGURE 12. Magnetic Transducer Amplifier

OSCILLATORS USING THE LM139

The LM139 lends itself well to oscillator applications for frequencies below several megacycles. Figure 13 shows a symmetrical square wave generator using a minimum of components. The output frequency is set by the RC time constant of R_4 and C_1 and the total hysteresis of the loop is set by R_1, R_2 and R_3. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output which would degrade the output slew rate.

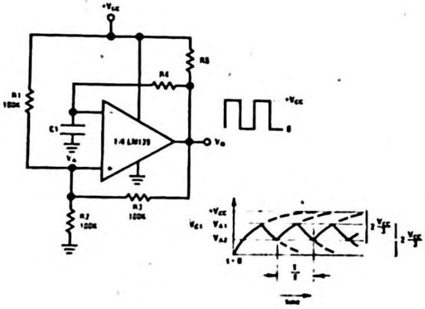


FIGURE 13. Square Wave Generator

To analyze this circuit assume that the output is initially high. For this to be true, the voltage at the negative input must be less than the voltage at the positive input. Therefore, capacitor C_1 is discharged. the voltage at the positive input, V_{A1}, will then be given by:

$$V_{A1} = \frac{+V_{CC}\,R_2}{R_2 + (R_1 \| R_3)} \tag{13}$$

where if $R_1 = R_2 = R_3$

then $$V_{A1} = \frac{2\,V_{CC}}{3} \tag{14}$$

Capacitor C_1 will charge up through R_4 so that when it has charged up to a value equal to V_{A1}, the comparator output will switch. With the output V_O = GND, the value of V_A is reduced by the hysteresis network to a value given by:

$$V_{A2} = \frac{+V_{CC}}{3} \tag{15}$$

using the same resistor values as before. Capacitor C_1 must now discharge through R_4 towards ground. The output will return to its high state ($V_O = +V_{CC}$) when the voltage across the capacitor has discharged to a value equal to V_{A2}. For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The period can be calculated from:

$$V_1 = V_{MAX}\, e^{-t_1/RC} \tag{16}$$

where

$$V_{MAX} = \frac{2\,V_{CC}}{3} \tag{17}$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \tag{18}$$

One period will be given by:

$$\frac{1}{\text{freq.}} = 2t_1 \tag{19}$$

or calculating the expenential gives

$$\frac{1}{\text{freq.}} = 2\,(0.694)\,R_4C_1 \tag{20}$$

Resistors R_3 and R_4 must be at least 10 times larger than R_5 to insure that V_O will go all the way up to $+V_{CC}$ in the high state. The frequency stability of this circuit should strictly be a function of the external components.

Pulse Generator with Variable Duty Cycle

The basic square wave generator of Figure 13 can be modified to obtain an adjustable duty cycle pulse generator, as shown in Figure 14, by providing a separate charge and discharge path for capacitor C_1. One path, through R_4 and D_1 will charge the capacitor and set the pulse width (t_1). The other path, R_5 and D_2, will discharge the capacitor and set the time between pulses (t_2). By varying resistor R_5, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying R_4, the pulse width will be altered without affecting the time between pulses. Both controls will change the freqeuncy of the generator, however. With the values given in Figure 14, the pulse width and time between pulses can be found from:

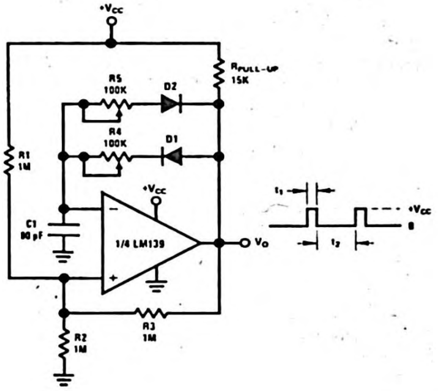


FIGURE 14. Pulse Generator with Variable Duty Cycle

$$V_1 = V_{MAX}\,(1 - e^{-t_1/R_4C_1}) \text{ risetime} \tag{21a}$$

$$V_1 = V_{MAX}\,e^{-t_2/R_5C_1} \text{ falltime} \tag{21b}$$

where

$$V_{MAX} = \frac{2\,V_{CC}}{3} \tag{22}$$

and

$$V_1 = \frac{V_{MAX}}{2} = \frac{V_{CC}}{3} \tag{23}$$

which gives

$$\frac{1}{2} = e^{-t_1/R_4C_1} \tag{24}$$

t_2 is then given by:

$$\frac{1}{2} = e^{-t_2/R_5C_1} \tag{25}$$

These terms will have a slight error due to the fact that V_{MAX} is not exactly equal to 2/3 V_{CC} but is actually reduced by the diode drop to:

$$V_{MAX} = \frac{2}{3}\,(V_{CC} - V_{BE}) \tag{26}$$

therefore

$$\frac{1}{2(1 - V_{BE})} = e^{-t_1/R_4C_1} \tag{27}$$

and

$$\frac{1}{2(1 - V_{BE})} = e^{-t_2/R_5C_1} \tag{28}$$

Crystal Controlled Oscillator

A simple yet very stable oscillator can be obtained by using a quartz crystal resonator as the feedback element. Figure 15 gives a typical circuit diagram of this. This value of R_1 and R_2 are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC time constant of R_3 and C_1 is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

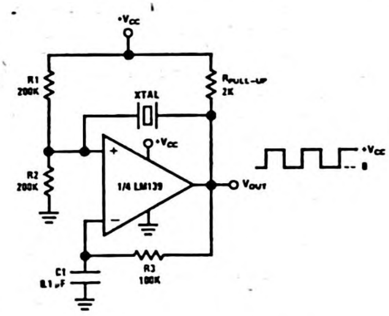


FIGURE 15. Crystal Controlled Oscillator

When specifying the crystal, be sure to order series resonant along with the desired temperature coefficient and load capacitance to be used.

MOS Clock Driver

The LM139 can be used to provide the oscillator and clock delay timing for a two phase MOS clock driver (see Figure 16). The oscillator is a standard comparator square wave generator similar to the one shown in Figure 13. Two other comparators of the LM139 are used to establish the desired phasing between the two outputs to the clock driver. A more detailed explanation of the delay circuit is given in the section under "Digital and Switching Circuits."

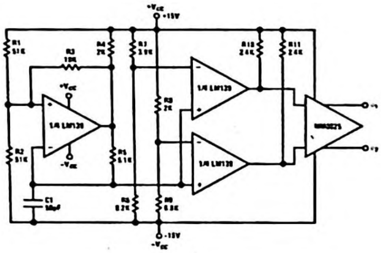

+Vcc
+15V
R1
51K
R3
10K
R4
2K
R7
3.9K
R10
2.4K
R11
2.4K
+Vcc
1/4 LM139
R8
2K
1/4 LM139
R2
51K
-Vcc
R5
5.1K
1/4 LM139
C1
50pF
R6
8.2K
R9
6.8K
-15V
-Vcc

FIGURE 16. MOS Clock Driver

Wide Range VCO

A simple yet very stable voltage controlled oscillator using a minimum of external components can be realized using three comparators of the LM139. The schematic is shown in Figure 17a. Comparator 1 is used closed loop as an integrator (for further discussion of closed loop operation see section on Operational Amplifiers) with comparator 2 used as a triangle to square wave converter and comparator 3 as the switch driving the integrator. To analyze the circuit, assume that comparator 2 is its high state ($V_{SQ} = +V_{CC}$) which drives comparator 3 to its high state also. The output device of comparator 3 will be OFF which prevents any current from flowing through R_2 to ground. With a control voltage, V_C, at the input to comparator 1, a current I_1 will flow through R_1 and begin discharging capacitor C_1, at a linear rate. This discharge current is given by.

$$I_1 = \frac{V_C}{2 R_1} \tag{29}$$

and the discharge time is given by:

$$I_1 = C_1 \frac{\Delta V}{\Delta t} \cdot \tag{30}$$

ΔV will be the maximum peak change in the voltage across capacitor C_1 which will be set by the switch points of comparator 2. These trip points can be changed by simply altering the ratio of R_F to R_S, thereby increasing or decreasing the amount of hysteresis around comparator 2. With $R_F = 100\ k\Omega$ and $R_S = 5\ k\Omega$, the amount of hysteresis is approximately ±5% which will give switch points of $+V_{CC}/2 \pm 750$ mV from a 30V supply. (See "Comparators with Hysteresis").

As capacitor C_1 discharges, the output voltage of comparator 1 will decrease until it reaches the lower trip point of comparator 2, which will then force the output of comparator 2 to go to its low state (V_{SQ} = GND).

This in turn causes comparator 3 to go to its low state where its output device will be in saturation. A current I_2 can now flow through resistor R_2 to

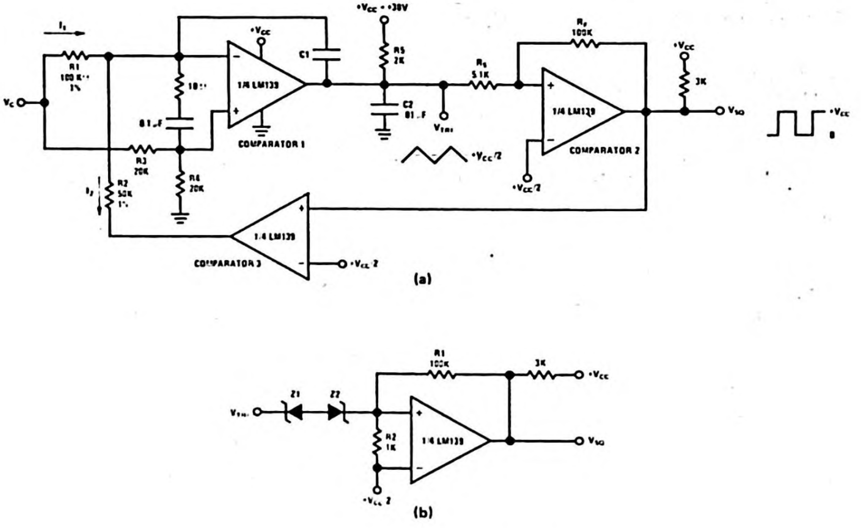

I1
R1
100 K
1%
Vc
10K
.01µF
R3
20K
R2
50K
1%
I2
R6
20K
+Vcc
1/4 LM139
COMPARATOR 1
C1
+Vcc = +30V
R5
2K
C2
.01µF
VTRI
+Vcc/2
RF
100K
RS
5.1K
1/4 LM139
COMPARATOR 2
+Vcc/2
+Vcc
3K
VSQ
+Vcc
0
1/4 LM139
COMPARATOR 3
+Vcc/2
(a)
R1
100K
3K
+Vcc
VTRI
Z1
Z2
R2
1K
1/4 LM139
VSQ
+Vcc/2
(b)

FIGURE 17. Voltage Controlled Oscillator

ground. If the value of R_2 is chosen as $R_1/2$ a current equal to the capacitor discharge current can be made to flow out of C_1 charging it at the same rate as it was discharged. By making $R_2 = R_1/2$, current I_2 will equal twice I_1. This is the control circuitry which guarantees a constant 50% duty cycle oscillation independent of frequency or temperature. As capacitor C_1 charges, the output of comparator 1 will ramp up until it trips comparator 2 to its high state ($V_{SQ} = +V_{CC}$) and the cycle will repeat.

The circuit shown in Figure 17a uses a +30V supply and gives a triangle wave of 1.5V peak-to-peak. With a timing capacitor, C_1 equal to 500 pF, a frequency range from approximately 115 kHz down to approximately 670 Hz was obtained with a control voltage ranging from 50V down to 250 mV. By reducing the hysteresis around comparator 2 down to ±150 mV ($R_F = 100\ k\Omega$, $R_S = 1\ k\Omega$) and reducing the compensating capacitor C_2 down to .001 μF, frequencies up to 1 MHz may be obtained. For lower frequencies ($f_o \leq 1$ Hz) the timing capacitor, C_1, should be increased up to approximately 1 μF to insure that the charging currents, I_1 and I_2, are much larger than the input bias currents of comparator 1.

Figure 17b shows another interesting approach to provide the hysteresis for comparator 2. Two identical Zener diodes, Z_1 and Z_2, are used to set the trip points of comparator 2. When the triangle wave is less than the value required to Zener one of the diodes, the resistive network, R_1 and R_2, provides enough feedback to keep the comparator in its proper state, (the input would otherwise be floating). The advantage of this circuit is that the trip points of comparator 2 will be completely independent of supply voltage fluctuations. The disadvantage is that Zeners with less than one volt breakdown voltage are not obtainable. This limits the maximum upper frequency obtainable because of the larger amplitude of the triangle wave. If a regulated supply is available, Figure 17a is preferable simply because of less parts count and lower cost.

Both circuits provide good control over at least two decades in frequency with a temperature coefficient largely dependent on the TC of the external timing resistors and capacitors. Remember that good circuit layout is essential along with the .01μF compensation capacitor at the output of comparator 1 and the series 10Ω, resistor and 0.1μF capacitor between its inputs, for proper operation. Comparator 1 is a high gain amplifier used closed loop as an integrater so long leads and loose layout should be avoided.

DIGITAL AND SWITCHING CIRCUITS

The LM139 lends itself well to low speed (<1 MHz) high level logic circuits. They have the advantage of operating with high signal levels, giving high noise immunity, which is highly desirable for industrial applications. The output signal level can be selected by setting the V_{CC} to which the pull-up resistor is connected to any desired level.

AND/NAND Gates

A three input AND gate is shown in Figure 18. Operation of this gate is as follows: resistor divider R_1 and R_2 establishes a reference voltage at the inverting input to the comparator. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers comprised of R_3, R_4, R_5 and R_6. The output will go high only when all three inputs are high, causing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a "0" equal to ground and a "1" equal +15V. The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are the "1" state. This circuit with increased fan-in is shown in Figure 19.

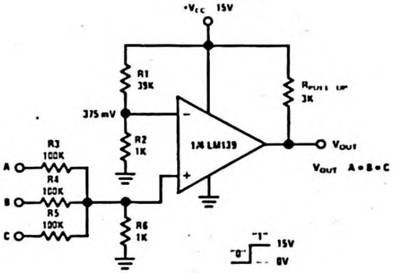


FIGURE 18. Three Input AND Gate

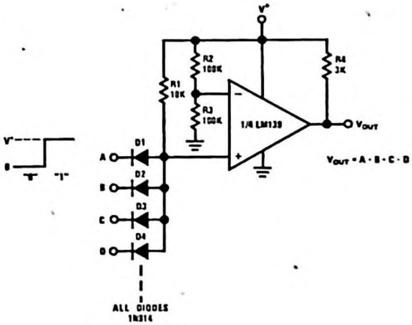


FIGURE 19. AND Gate with Large Fan-In

To convert these AND gates to NAND gates simply interchange the inverting and non-inverting inputs to the comparator. Hysteresis can be added to speed up output transitions if low speed input signals are used.

OR/NOR Gates

The three input OR gate (positive logic) shown in Figure 20 is achieved from the basic AND gate simply by increasing R_1 thereby reducing the reference voltage. A logic "1" at any of the inputs will produce a logic "1" at the output. Again a NOR gate may be implemented by simply reversing the comparator inputs. Resistor R_6 may be added for the OR or NOR function at the expense of noise immunity if so desired.

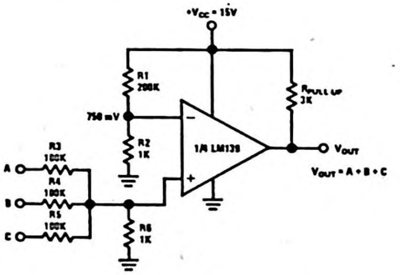

+VCC = 15V
R1
200K
RPULL UP
3K
750 mV
R2
1K
1/4 LM139
VOUT
VOUT = A + B + C
R3
100K
A
R4
100K
B
R5
100K
C
R6
1K

FIGURE 20. Three Input OR Gate

Output Strobing

The output of the LM139 may be disabled by adding a clamp transistor as shown in Figure 21. A strobe control voltage at the base of Q_1 will clamp the comparator output to ground, making it immune to any input changes.

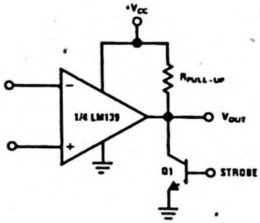

+VCC
RPULL-UP
1/4 LM139
VOUT
Q1
STROBE

FIGURE 21. Output Strobing Using a Discrete Transistor

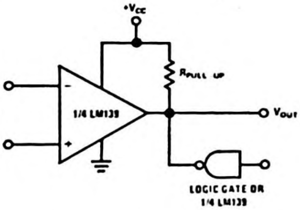

+VCC
RPULL UP
1/4 LM139
VOUT
LOGIC GATE OR
1/4 LM139

FIGURE 22. Output Strobing with TTL Gate

If the LM139 is being used in a digital system the output may be strobed using any other type of gate having an uncommitted collector output (such as National's DM5401/DM7401). In addition another comparator of the LM139 could also be used for output strobing, replacing Q_1 in Figure 21, if desired. (See Figure 22.)

One Shot Multivibrators

A simple one shot multivibrator can be realized using one comparator of the LM139 as shown in Figure 23. The output pulse width is set by the values of C_2 and R_4 (with $R_4 > 10\ R_3$ to avoid loading the output). The magnitude of the input trigger pulse required is determined by the resistive divider R_1 and R_2. Temperature stability can be achieved by balancing the temperature coefficients of R_4 and C_2 or by using components with very low TC. In addition, the TC of resistors R_1 and R_2 should be matched so as to maintain a fixed reference voltage of $+V_{CC}/2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset the one shot at the end of its pulse. It also prevents the non-inverting input from being driven below ground. The output pulse width is relatively independent of the magnitude of the supply voltage and will change less than 2% for a five volt change in $+V_{CC}$.

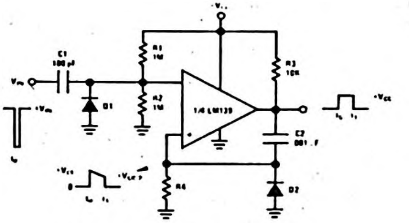

+VCC
C1
100 pF
VIN
R1
1M
R2
1M
D1
R3
10K
1/4 LM139
C2
.001 μF
+VCC
R4
D2
0

FIGURE 23. One Shot Multivibrator

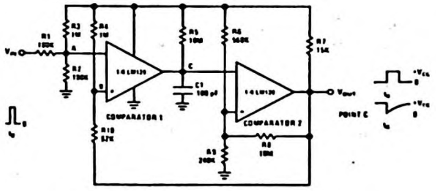

R1
100K
VIN
R3
1M
R4
1M
R2
100K
A
B
1/4 LM139
COMPARATOR 1
R10
C
C1
100 pF
R5
10M
R6
R7
15K
1/4 LM139
COMPARATOR 2
R8
10M
R9
240K
VOUT
POINT C
+VCC
0

FIGURE 24. Multivibrator with Input Lock-Out

The one shot multivibrator shown in Figure 24 has several characteristics which make it superior to that shown in Figure 23. First, the pulse width is independent of the magnitude of the power supply voltage because the charging voltage and the intercept voltage are a fixed percentage of $+V_{CC}$. In addition this one-shot is capable of 99% duty cycle and exhibits input trigger lock-out to insure that the circuit will not re-trigger before the output pulse has been completed. The trigger level is the voltage required at the input to raise the voltage at point A higher than the voltage at point B, and is set by the resistive divider R_4 and R_{10} and the network R_1, R_2 and R_3. When the multivibrator has been triggered, the output of comparator 2 is high causing the reference voltage at the non-inverting input of comparator 1 to go to $+V_{CC}$. This prevents any additional input pulses from disturbing the circuit until the output pulse has been completed.

The value of the timing capacitor, C_1, must be kept small enough to allow comparator 1 to completely discharge C_1 before the feedback signal from comparator 2 (through R_{10}) switches comparator 1 OFF and allows C_1 to start an exponential charge. Proper circuit action depends on rapidly discharging C_1 to a value set by R_6 and R_9 at which time comparator 2 latches comparator 1 OFF. Prior to the establishment of this OFF state, C_1 will have been completely discharged by comparator 1 in the ON state. The time delay, which sets the output pulse width, results from C_1 recharging to the reference voltage set by R_6 and R_9. When the voltage across C_1 charges beyond this reference, the output pulse returns to ground and the input is again reset to accept a trigger.

Bistable Multivibrator

Figure 25 is the circuit of one comparator of the LM139 used as a bistable multivibrator. A reference voltage is provided at the inverting input by a voltage divider comprised of R_2 and R_3. A pulse applied to the SET terminal will switch the output high. Resistor divider network R_1, R_4, and R_5 now clamps the non-inverting input to a voltage greater than the reference voltage. A pulse now applied to the RESET input will pull the output low. If both Q and $\overline{Q}$ outputs are needed, another comparator can be added as shown dashed in Figure 25.

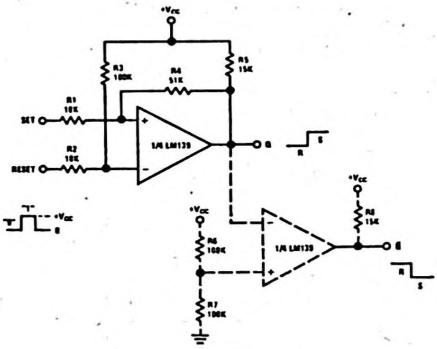


FIGURE 25. Bistable Multivibrator

Figure 26 shows the output saturation voltage of the LM139 comparator verses the amount of current being passed to ground. The end point of 1 mV at zero current along with an R_{SAT} of 60Ω shows why the LM139 so easily adapts itself to oscillator and digital switching circuits by allowing the DC output voltage to go practically to ground while in the ON state.

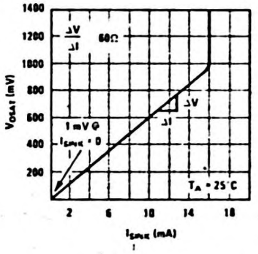


FIGURE 26. Typical Output Saturation Characteristics

Time Delay Generator

The final circuit to be presented under "Digital and Switching Circuits" is a time delay generator (or sequence generator) as shown in Figure 27.

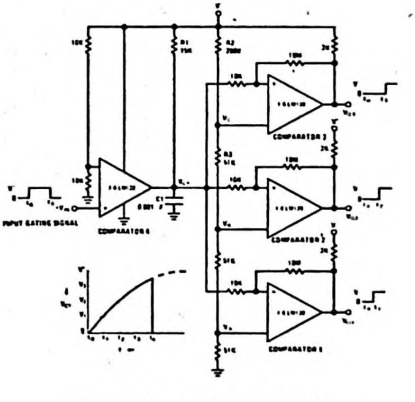


FIGURE 27. Time Delay Generator

This timer will provide output signals at prescribed time intervals from a time reference t_O and will automatically reset when the input signal returns to ground. For circuit evaluation, first consider the quiescent state ($V_{IN} = 0$) where the output of comparator 4 is ON which keeps the voltage across C_1 at zero volts. This keeps the outputs of comparators 1, 2 and 3 in their ON state (V_{OUT} = GND). When an input signal is applied, comparator 4 turns OFF allowing C_1 to charge at an exponential rate through R_1. As this voltage rises past the preset trip points V_A, V_B and V_C of comparators 1, 2 and 3 respectively, the output voltage of each of these comparators will switch to the high state ($V_{OUT} = +V_{CC}$). A small amount of hysteresis has been provided to insure fast switching for the case where the R_C time constant has been chosen large to give long delay times. It is not necessary that all comparator outputs be low in the quiescent state. Several or all may be reversed as desired simply be reversing the inverting and non-inverting input connections. Hysteresis again is optional.

LOW FREQUENCY OPERATIONAL AMPLIFIERS

The LM139 comparator can be used as an operational amplifier in DC and very low frequency AC applications (≤100 Hz). An interesting combination is to use one of the comparators as an op amp to provide a DC reference voltage for the other three comparators in the same package.

Another useful application of an LM139 has the interesting feature that the input common mode voltage range includes ground even though the amplifier is biased from a single supply and ground. These op amps are also low power drain devices and will not drive large load currents unless current boosted with an external NPN transistor. The largest application limitation comes from a relatively slow slew rate which restricts the power bandwidth and the output voltage response time.

The LM139, like other comparators, is not internally frequency compensated and does not have internal provisions for compensation by external components. Therefore, compensation must be applied at either the inputs or output of the device. Figure 28 shows an output compensation scheme which utilizes the output collector pull-up resistor working with a single compensation capacitor to form a dominant pole. The feedback network, R_1 and R_2 sets the closed loop gain at $1 + R_1/R_2$ or 101 (40 dB). Figure 29 shows the output swing limitations versus frequency. The output current capability of this amplifier is limited by the relatively large pull-up resistor (15 kΩ) so the output is shown boosted with an external NPN transistor in Figure 30. The frequency response is greatly extended by the use of the new compensation scheme also shown in Figure 30. The DC level shift due to the V_{BE} of Q_1 allows the output voltage to swing from ground to approximately one volt less than $+V_{CC}$. A voltage offset adjustment can be added as shown in Figure 31.

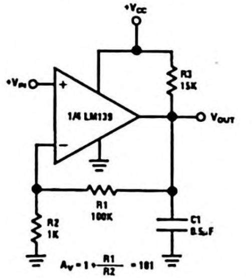


FIGURE 28. Non-Inverting Amplifier

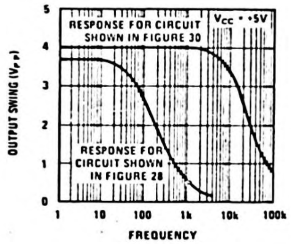


FIGURE 29. Large Signal Frequency Response

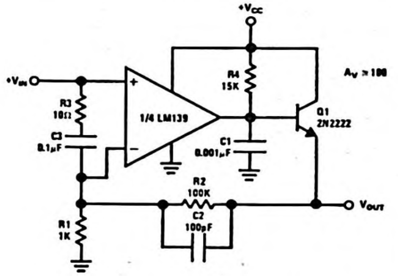


FIGURE 30. Improved Operational Amplifier

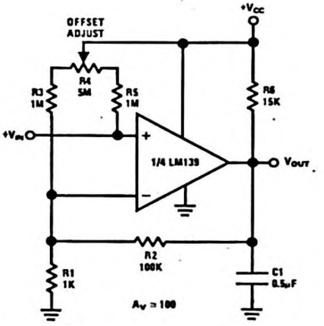


FIGURE 31. Input Offset Null Adjustment

Dual Supply Operation

The applications presented here have been shown biased typically between $+V_{CC}$ and ground for simplicity. The LM139, however, works equally well from dual (plus and minus) supplies commonly used with most industry standard op amps and comparators, with some applications actually requiring fewer parts than the single supply equivalent.

The zero crossing detector shown in Figure 10 can be implemented with fewer parts as shown in Figure 32. Hysteresis has been added to insure fast transitions if used with slowly moving input signals. It may be omitted if not needed, bringing the total parts count down to one pull-up resistor.

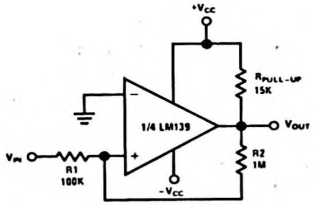


FIGURE 32. Zero Crossing Detector Using Dual Supplies

The MOS clock driver shown in Figure 16 uses dual supplies to properly drive the MM0025 clock driver.

The square wave generator shown in Figure 13 can be used with dual supplies giving an output that swings symmetrically above and below ground (see Figure 33). Operation is identical to the single supply oscillator with the only change being in the lower trip point.

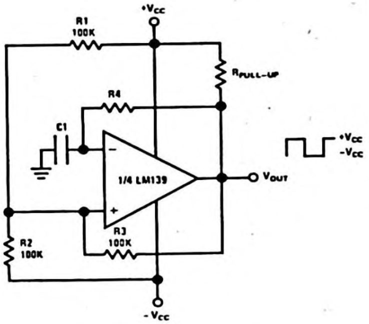


FIGURE 33. Squarewave Generator Using Dual Supplies

Figure 34 shows an LM139 connected as an op amp using dual supplies. Biasing is actually simpler if full output swing at low gain settings is required by biasing the inverting input from ground rather than from a resistive divider to some voltage between $+V_{CC}$ and ground.

All the applications shown will work equally well biased with dual supplies. If the total voltage across the device is increased from that shown, the output pull-up resistor should be increased to prevent the output transistor from being pulled out of saturation by drawing excessive current, thereby preventing the output low state from going all the way to $-V_{CC}$.

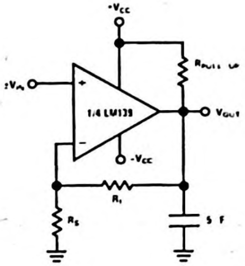


FIGURE 34. Non-Inverting Amplifier Using Dual Supplies

MISCELLANEOUS APPLICATIONS

The following is a collection of various applications intended primarily to further show the wide versatility that the LM139 quad comparator has to offer. No new modes of operation are presented here so all of the previous formulas and circuit descriptions will hold true. It is hoped that all of the circuits presented in this application note will suggest to the user a few of the many areas in which the LM139 can be utilized.

Remote Temperature Sensor/Alarm

The circuit shown in Figure 35 shows a temperature over-range limit sensor. The 2N930 is a National process 07 silicon NPN transistor connected to produce a voltage reference equal to a multiple of its base emitter voltage along with a temperature coefficient equal to a multiple of 2.2 mV/°C. That multiple is determined by the ratio of R_1 to R_2. The theory of operation is as follows: with transistor Q_1 biased up, its base to emitter voltage will appear across resistor R_1. Assuming a reasonably high beta ($\beta \geq 100$) the base current can be neglected so that the current that flows through resistor R_1 must also be flowing through R_2. The voltage drop across resistor R_2 will be given by:

$$I_{R1} = I_{R2}$$

and

$$V_{R1} = V_{be} = I_{R1} R_1$$

so

$$V_{R2} = I_{R2} R_2 = I_{R1} R_2 = V_{be} \frac{R_2}{R_1} \tag{31}$$

As stated previously this base-emitter voltage is strongly temperature dependent, minus 2.2 mV/°C for a silicon transistor. This temperature coefficient is also multiplied by the resistor ratio R_1/R_2.

This provides a highly linear, variable temperature coefficient reference which is ideal for use as a temperature sensor over a temperature range from approximately −65°C to +150°C. When this temperature sensor is connected as shown in Figure 35 it can be used to indicate an alarm condition of either too high or too low a temperature excursion. Resistors R_3 and R_4 set the trip point reference voltage, V_B, with switching occuring when $V_A = V_B$. Resistor R_5 is used to bias up Q_1 at some low value of current simply to keep quiescent power dissipation to a minimum. An I_Q near 10μA is acceptable.

Using one LM139, four separate sense points are available. The outputs of the four comparators can be used to indicate four separate alarm conditions or the outputs can be OR'ed together to indicate an alarm condition at any one of the sensors. For the circuit shown the output will go HIGH when the temperature of the sensor goes above the preset level. This could easily be inverted by simply reversing the input leads. For operation over a narrow temperature range, the resistor ratio R_2/R_1 should be large to make the alarm more sensitive to temperature variations. To vary the trip points a potentiometer can be substituted for R_3 and R_4. By the addition of a single feedback resistor to the non-inverting input to provide a slight amount of hysteresis, the sensor could function as a thermostat. For driving loads greater than 15 mA, an output current booster transistor could be used.

Four Independently Variable, Temperature Compensated, Reference Supplies

The circuit shown in Figure 36 provides four independently variable voltages that could be used for low current supplies for powering additional equipment or for generating the reference voltages needed in some of the previous comparator applications. If the proper Zener diode is chosen, these four voltages will have a near zero temperature coefficient. For industry standard Zeners, this will be somewhere between 5.0 and 5.4V at a Zener current of approximately 10 mA. An alternative solution is offered to reduce this 50 mW quiescent

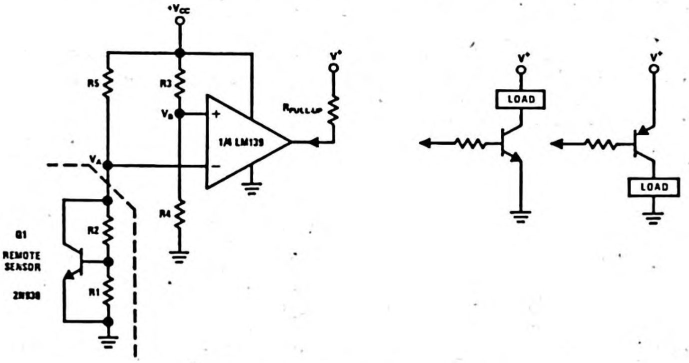


FIGURE 35. Temperature Alarm

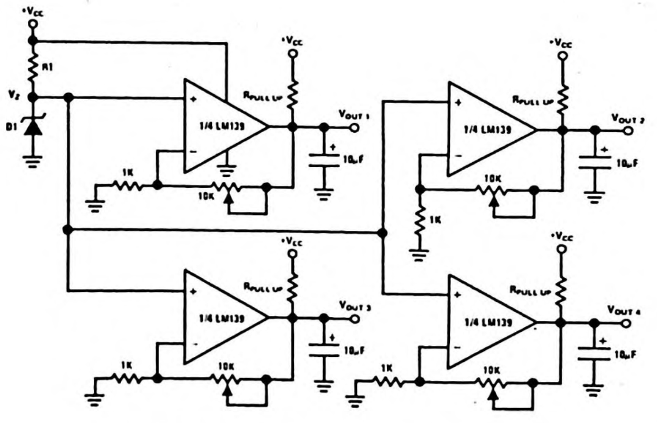


FIGURE 36. Four Variable Reference Supplies

power drain. Experimental data has shown that any of National's process 21 transistors which have been selected for low reverse beta ($\beta_R < .25$) can be used quite satisfactorily as a zero T.C. Zener. When connected as shown in Figure 37, the T.C. of the base-emitter Zener voltage is exactly cancelled by the T.C. of the forward biased base-collector junction if biased at 1.5 mA. The diode can be properly biased from any supply by adjusting R_5 to set I_q equal to 1.5 mA. The outputs of any of the reference supplies can be current boosted by using the circuit shown in Figure 30.

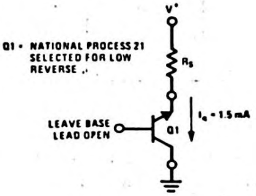

V+
Q1 • NATIONAL PROCESS 21 SELECTED FOR LOW REVERSE β
R5
LEAVE BASE LEAD OPEN
Q1
Iq = 1.5 mA

FIGURE 37. Zero T.C. Zener

Digital Tape Reader

Two circuits are presented here — a tape reader for both magnetic tape and punched paper tape. The circuit shown in Figure 38, the magnetic tape reader, is the same as Figure 12 with a few resistor values changed. With a 5V supply, to make the output TTL compatible, and a 1MΩ feedback resistor, ±5 mV of hysteresis is provided to insure fast switching and higher noise immunity. Using one LM139, four tape channels can be read simultaneously.

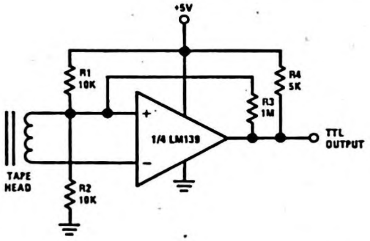

+5V
R1 10K
R4 5K
R3 1M
1/4 LM139
TTL OUTPUT
TAPE HEAD
R2 10K

FIGURE 38. Magnetic Tape Reader with TTL Output

The paper tape reader shown in Figure 39 is essentially the same circuit as Figure 38 with the only change being in the type of transducer used. A photo-diode is now used to sense the presence or absence of light passing through holes in the tape. Again a 1MΩ feedback resistor gives ±5 mV of hysteresis to insure rapid switching and noise immunity.

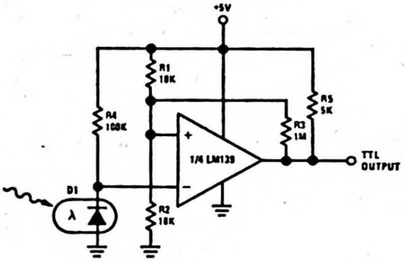

+5V
R1 10K
R4 100K
R5 5K
R3 1M
1/4 LM139
TTL OUTPUT
D1
λ
R2 10K

FIGURE 39. Paper Tape Reader With TTL Output

Pulse Width Modulator

Figure 40 shows the circuit for a simple pulse width modulator circuit. It is essentially the same as that shown in Figure 13 with the addition of an input control voltage. With the input control voltage equal to $+V_{CC}/2$, operation is basically the same as that described previously. If the input control voltage is moved above or below $+V_{CC}/2$, however, the duty cycle of the output square wave will be altered. This is because the addition of the control voltage at the input has now altered the trip points. These trip points can be found if the circuit is simplified as in Figure 41. Equations 13 through 20 are still applicable if the effect of R_C is added, with equations 17 through 20 being altered for the condition where $V_C \neq +V_{CC}/2$.

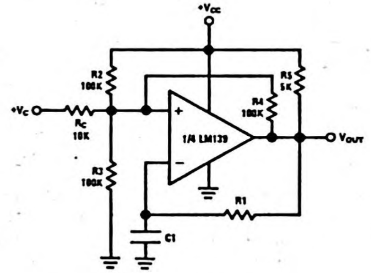

+VCC
R2 100K
R5 5K
R4 100K
+VC
RC 10K
1/4 LM139
VOUT
R3 100K
R1
C1

FIGURE 40. Pulse Width Modulator

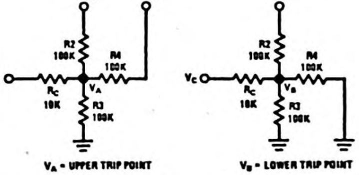

+VCC
+VCC
R2 100K
R4 100K
RC 10K
VA
R3 100K
VA = UPPER TRIP POINT
+VCC
R2 100K
R4 100K
VC
RC 10K
VB
R3 100K
VB = LOWER TRIP POINT

FIGURE 41. Simplified Circuit For Calculating Trip Points of Figure 40.

Pulse width sensitivity to input voltage variations will be increased by reducing the value of R_C from 10 kΩ and alternately, sensitivity will be reduced by increasing the value of R_C. The values of R_1 and C_1 can be varied to produce any desired center frequency from less than one hertz to the maximum frequency of the LM139 which will be limited by $+V_{CC}$ and the output slew rate.

Positive and Negative Peak Detectors

Figures 42 and 43 show the schematics for simple positive or negative peak detectors. Basically the LM139 is operated closed loop as a unity gain follower with a large holding capacitor from the output to ground. For the positive peak detector a low impedance current source is needed so an additional transistor is added to the output. When the output of the comparator goes high, current is passed through Q_1 to charge up C_1. The only discharge path will be the 1MΩ resistor shunting C_1 and any load that is connected to V_{OUT}. The decay time can be altered simply by changing the 1MΩ resistor higher or lower as desired. The output should be used through a high impedance follower to avoid loading the output of the peak detector.

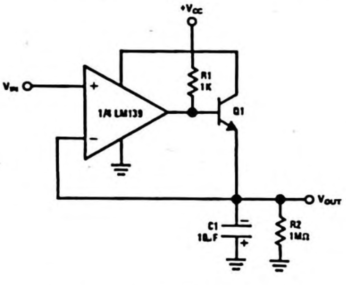


FIGURE 42. Positive Peak Detector

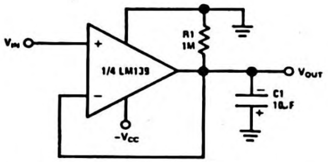


FIGURE 43. Negative Peak Detector

For the negative peak detector, a low impedance current sink is required and the output transistor of the LM139 works quite well for this. Again the only discharge path will be the 1MΩ resistor and any load impedance used. Decay time is changed by varying the 1MΩ resistor.

Conclusion

The LM139 is an extremely versatile comparator package offering reasonably high speed while operating at power levels in the low mW region. By offering four independent comparators in one package, many logic and other functions can now be performed at substantial savings in circuit complexity, parts count, overall physical dimensions, and power consumption.

For limited temperature range applications, the LM239 or LM339 may be used in place of the LM139.

It is hoped that this application note will provide the user with a guide for using the LM139 and also offer some new application ideas.

Applications for a High Speed FET Input Op Amp

National Semiconductor
Application Note 75
Barry Siegel
December 1972

INTRODUCTION

The principal limitations in speed and bandwidth in IC FET input op amps have been reduced by over an order of magnitude with the introduction of the LH0062/LH0062C. Internal compensation assures unity gain stability with bandwidths in excess of 15 MHz. Voltage follower slew rate is typically 75V/µs and is guaranteed in excess of 50V/µs. Furthermore, external components may be used to extend the slew rate to 120V/µs and settling times under 1µs. The LH0062H (TO-5) is pin compatible with LM101, LM741 and LH0022. A summary of the LH0062's performance characteristics is given in Table 1.

PARAMETER (T_A = 25°C)	MIN	TYP	MAX	UNITS
Input Offset Voltage		2.0	5.0	mV
Input Bias Current			20	pA
Voltage Gain	50	100		V/mV
Slew Rate	50	75		V/µs
Bandwidth		15		MHz

TABLE 1. Summary of LH0062 Characteristics

CIRCUIT DESCRIPTION

The LH0062 is basically a two stage amplifier (Figure 1) consisting of a N channel junction FET input stage (Q_1 and Q_2) and a PNP output stage (Q_4 and Q_5). Q_1 and Q_2 are a well matched interdigitated monolithic pair that provide high common mode rejection and input offset voltage tracking usually associated only with bipolar designs. The current mirror (Q_6 and Q_7) converts to single ended operation in addition to providing active high impedance load for Q_4 and Q_5 thus providing high gain. Q_3 and D_1 provides a temperature compensated current source for the input stage and Q_8, Q_9, D_2 and D_3 form a class AB output buffer. Detailed schematic is illustrated in Figure 2. Note that the FET inputs are protected by 5V zener diodes and input current under transient conditions should be limited by inserting a 1k ohm or larger resistor in series with one of the inputs.

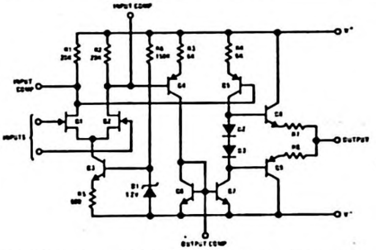


FIGURE 1. Simplified LH0062 Circuit Schematic

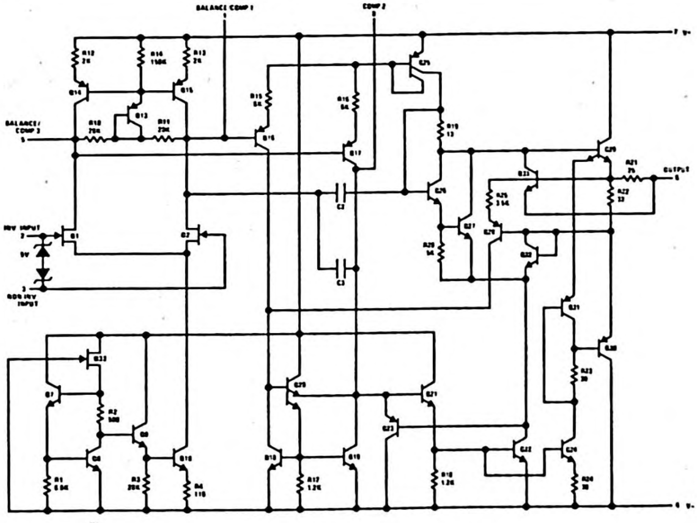


FIGURE 2. Complete LH0062 Schematic

COMPENSATION CONSIDERATIONS

As noted earlier, the LH0062 is internally compensated for unity gain stability. However, a few precautions are advised. Like most wide band amplifiers, the LH0062 is sensitive to power supply inductance, and decoupling the supplies with 0.1μF ceramic disc capacitors within an inch or two of the device will prevent spurious oscillations and save a fair amount of grief. The device is capable of driving 50 to 100 pF loads; for larger loads, an isolation resistor, R_3 as shown in Figure 3 is recommended. Alternatively, a current buffer such as the LH0002 or LH0033 may be used for loads in excess of 500 pF with no degradation in slew rate as shown in Figure 4.

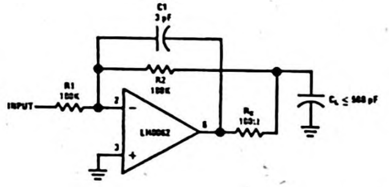

C1
3 pF
R2
100K
R1
100K
INPUT
2
3
LH0062
6
R0
100Ω
C_L ≤ 500 pF

FIGURE 3. Isolating a Capacitive Load up to 500 pF

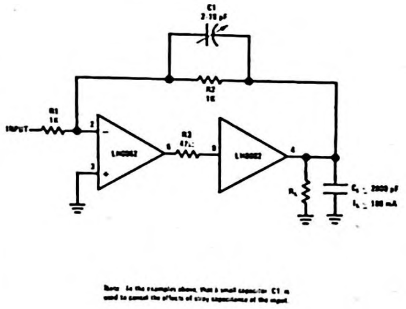

C1
2-10 pF
R2
1K
R1
1K
INPUT
2
3
LH0062
6
R3
47Ω
5
LH0002
4
R_L
C_L ≤ 2000 pF
I_L ≤ 100 mA

FIGURE 4. Driving Capacitances in Excess of 500 pF and Loads

The LH0062 may be feed-forward compensated in inverting mode applications as shown in Figure 5. This boosts slew rate to over 120V/μs and bandwidth to over 30 MHz. When full bandwidth is not required, the device may be over-compensated as shown in Figure 6 to reduce bandwidth to 5 MHz. This technique improves phase margin and reduces susceptibility to spurious oscillations in applications where speed is less critical.

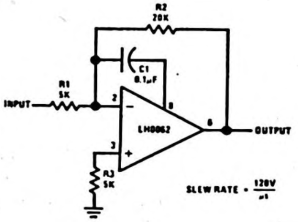

R2
20K
C1
0.1μF
R1
5K
INPUT
2
8
LH0062
6
OUTPUT
3
R3
5K
SLEW RATE = 120V/μs

FIGURE 5. Feed Forward Compensation

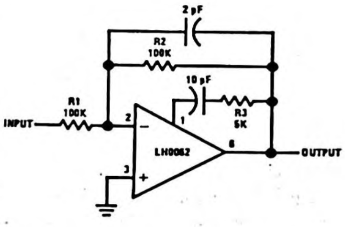

2 pF
R2
100K
10 pF
R1
100K
R3
5K
INPUT
2
1
LH0062
6
OUTPUT
3

FIGURE 6. Overcompensation

Minimum settling time of less than 1μs to 0.1% for a 20V input step is obtained as illustrated in Figure 7. A small tweak capacitor, C_1 is recommended to cancel stray board layout capacitance, C_S. Once best value of trimmer capacitor C_1 is determined for a particular layout, it may be replaced with a fixed value.

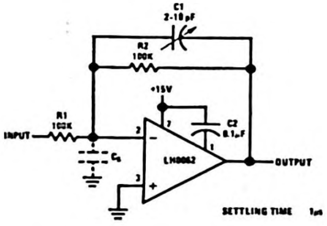

C1
2-10 pF
R2
100K
+15V
R1
100K
INPUT
2
7
C2
0.1μF
1
C_S
LH0062
OUTPUT
3
SETTLING TIME 1μs

FIGURE 7. Compensation for Minimum Settling Time

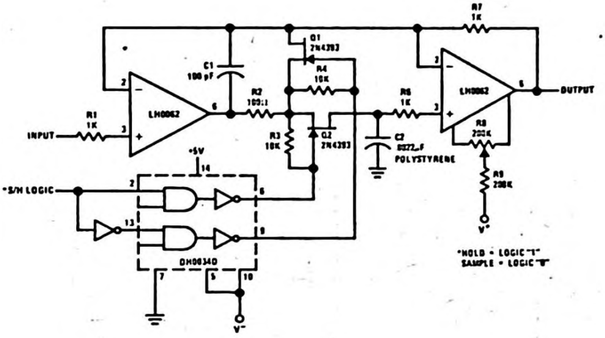

R7
1K
Q1
2N4393
C1
100 pF
R4
10K
LH0062
R2
100:1
R6
1K
LH0062
OUTPUT
R1
1K
INPUT
R3
10K
Q2
2N4393
C2
.0022μF
POLYSTYRENE
R8
200K
R9
200K
V+
+5V
14
*S/H LOGIC
2
6
13
9
DH0034D
7
5
10
V⁻
*HOLD = LOGIC "1"
SAMPLE = LOGIC "0"

FIGURE 8. High Speed Sample & Hold

APPLICATIONS

The circuit of Figure 8 is a high speed sample and hold with sample acquisition time of 10μs for 0.1% accuracy and aperture time of approximately 25 ns. Resistor, R_6, is used to limit input current during power on and off transients. Although the inputs of the LH0062 are protected by back-to-back diodes excessive input current could damage the device. Resistor R_9 and the pot, R_8, allow null of the output offset with negligible effect on offset drift.

The peak detector of Figure 9 will acquire a +10V peak signal in under 4μs with droop rates under 20 mV/sec. Reversing the polarity of diodes D_1 and D_2 will allow peak detecting negative signals. Any ultra-low leakage diode may be substituted for the 2N930 collector-base junction.

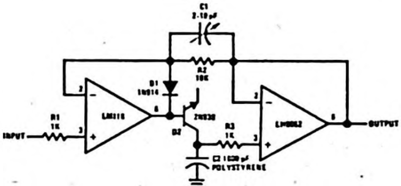

C1
2-10pF
R2
10K
D1
1N914
LM318
2N930
D2
R1
1K
INPUT
R3
1K
LH0062
OUTPUT
C2 1000 pF
POLYSTYRENE

FIGURE 9. High Speed Peak Detector

The circuit of Figure 10 is a programmable integrator with a range in period from 1μs to 1 ms. For best results C_1 through C_4 should be low leakage construction such as polycarbonate or polystyrene. A simple method of implementing the offset adjustment is to momentarily insert a 100k ohm resistor between pins 2 and 6 of the LH0062. With the switches of the AH5009 off, the output may be set to zero with R_2.

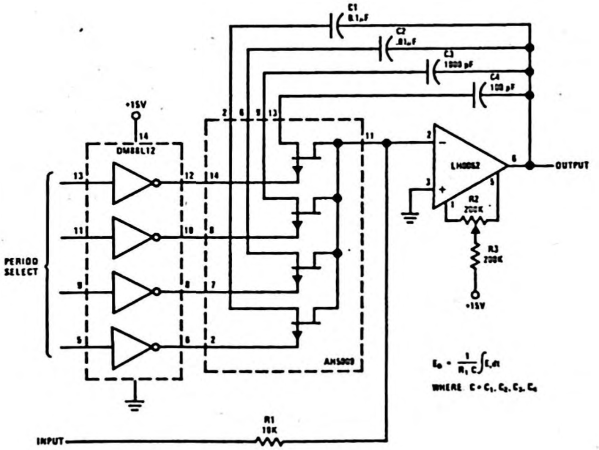

C1
0.1μF
C2
.01μF
C3
1000 pF
C4
100 pF
+15V
14
DM88L12
2 6 9 13
11
LH0062
OUTPUT
PERIOD SELECT
13
12
14
11
10
8
9
8
7
5
6
2
AH5009
R2
200K
R3
200K
+15V
R1
10K
INPUT
$E_o = -\frac{1}{R_1 C}\int E_i dt$
WHERE C = C₁, C₂, C₃, C₄

FIGURE 10. Programmable Integrator

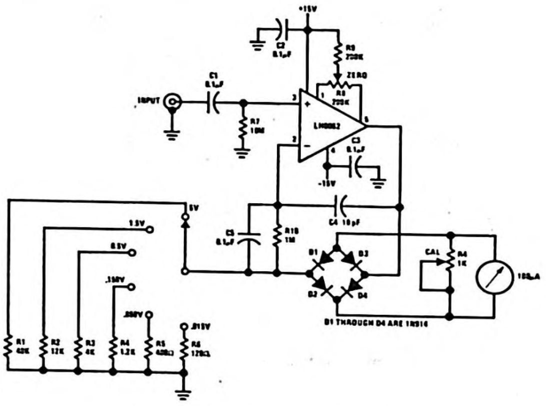

+15V
C2
0.1µF
R9
200K
ZERO
R8
200K
C1
0.1µF
INPUT
R7
10M
3
+
1
LH0062
6
2
−
C3
0.1µF
4
−15V
5V
1.5V
0.5V
.150V
.050V
.015V
C5
0.1µF
R10
1M
C4 10pF
D1
D2
D3
D4
CAL
R4
1K
100µA
D1 THROUGH D4 ARE 1N914
R1
40K
R2
12K
R3
4K
R4
1.2K
R5
400Ω
R6
120Ω

FIGURE 11. Wide Band AC Voltmeter

The circuit of Figure 11 is a wide band AC voltmeter capable of measuring AC signals as low as 15 mV at frequencies from 100 Hz to 500 kHz. Full scale sensitivity may be changed by altering the values R_1 through R_6 ($R \cong V_{IN}/100\mu A$).

HEAT SINKING, GUARDING, AND BOOTSTRAPPING

The LH0062 is specified for operation without an external heat sink. However, standby power is typically 240 mW causing a junction rise of approximately 60°C. A clip-on heat sink can reduce internal heating hence reduce input bias current from 20 pA at 25°C ambient to 2 or 3 pA.

Guarding input leads is recommended in stringent applications. An excellent discussion on guarding is given in AN-63 and the techniques discussed are directly applicable to the LH0062. Another benefit of guarding is reduced input capacitance. By bootstrapping the inputs, as shown in Figure 12, the apparent input capacitance is reduced to fractions of a pico-farad.

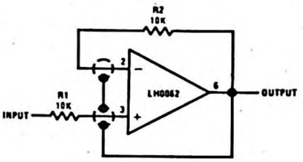

R2
10K
2
−
LH0062
6
OUTPUT
R1
10K
INPUT
3
+

FIGURE 12. Guard/Bootstrap for Unity Gain

Furthermore, the case of the LH0062 is electrically isolated, and the output may be tied to case in order to eliminate stray capacitance introduced by the header.

REFERENCES

1. R. K. Underwood, *"New Design Techniques for FET Op Amps,"* National Semiconductor AN-63, March 1972.
2. R. C. Dobkin, *"LM118 Op Amp Slews 70V/µs,"* National Semiconductor LB-17, September 1971.

IC Preamplifier Challenges Choppers on Drift

National Semiconductor
Application Note 79
Robert C. Dobkin
February 1973

Since the introduction of monolithic IC amplifiers there has been a continual improvement in DC accuracy. Bias currents have been decreased by 5 orders of magnitude over the past 5 years. Low offset voltage drift is also necessary in a high accuracy circuits. This is evidenced by the popularity of low drift amplifier types as well as the requests for selected low-drift op amps. However, until now the chopper stabilized amplifier offered the lowest drift. A new monolithic IC preamplifier designed for use with general purpose op amps improves DC accuracy to where the drift is lower than many chopper stabilized amplifiers.

INTRODUCTION

Chopper amplifiers have long been known to offer the lowest possible DC drift. They are not without problems, however. Most chopper amps can be used only as inverting amplifiers, limiting their applications. Chopping can introduce noise and spikes into the signal. Mechanical choppers need replacement as well as being shock sensitive. Further, chopper amplifiers are designed to operate over a limited power supply, limited temperature range.

Previous low-drift op amps do not provide optimum performance either. Selected devices may only meet their specified voltage drift under restrictive conditions. For example, if a 741 device is selected without offset nulling, the addition of a offset null pot can drastically change the drift. Low drift op amps designed for offset balancing have another problem. The resistor network used in the null circuit is designed to null the drift when the offset voltage is nulled. The mechanism to achieve nulled drift depends on the difference in temperature coefficient between the internal resistors and the external null pot. Since the internal resistors have a non-linear temperature coefficient and may vary device to device as well as between manufacturers, it can only approximately null offset drift. The problem gets worse if the external null pot has a TC other than zero.

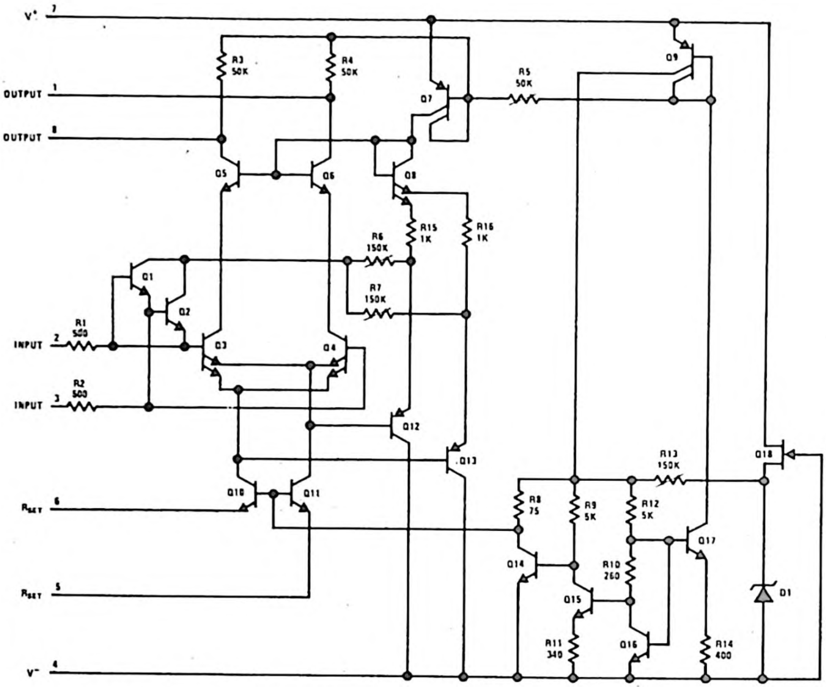
A new IC preamplifier is now available which can give drifts as low as $0.2\mu V/^\circ C$. It is used with conventional op amps and eliminates the problems associated with older devices. As well as improving the DC input characteristics of the op amp, loop-gain is increased when an LM121 is used. This further improves overall accuracy since DC gain error is decreased.

The LM121 preamp is designed to give zero drift when the offset voltage is nulled to zero. The operating current of the LM121 is programmable by the value of the null network resistors. The drift is independent of the value of the nulling network so it can be used over a wide range of operating currents while retaining low drift. The operating current can be chosen to optimize bias current, gain, speed, or noise while still retaining the low drift. Further, since the drift is independent of the match between external and internal resistors when the offset is nulled, lower and more predictable drifts can be expected in actual use. The input is fully differential, overcoming many of the problems with single ended chopper-amps. The device also has enough common mode rejection ratio to allow the low drift to be fully utilized.

CIRCUIT DESCRIPTION

The LM121 is a well matched differential amplifier utilizing super-gain transistors as the input devices. A schematic is shown in Figure 1. The input signal is applied to the bases of Q_3 and Q_4 through protection resistors R_1 and R_2. Q_3 and Q_4 have two emitters to allow offset balancing which will be explained later. The operating current for the differential amplifier is supplied by current sources Q_{10} and Q_{11}. The operating current is externally programmed by resistors connected from the emitters of Q_{10} and Q_{11} to the negative supply. Input transistors Q_3 and Q_4 are cascoded by transistors Q_5 and Q_6 to keep the collector base voltage on the input stage equal to zero. This eliminates leakage at high operating temperatures and keeps the common mode input voltage from appearing across the low breakdown super-gain input transistors. Additionally, the cascode improves the common mode rejection of the differential amplifier. Q_1 and Q_2 protect the input against large differential voltages.

The output signal is developed across resistive loads R_3 and R_4. The total collector current of the input is then applied to the base of a fixed gain PNP, Q_7. The collector current of Q_7 sets the operating current of Q_8, Q_{12}, and Q_{13}. These transistors are used to set the operating voltage of the cascode, Q_5 and Q_6. By operating the cascode biasing transistors at the same operating current as the input stage, it is possible to keep collector base voltage at zero; and therefore, collector-base leakage remains low over a wide current range. Further, this minimizes the effects of V_{BE} variations and finite transistor current gain. At high operating currents the collector base voltage of the input stage is increased by about 100 mV due to the drop across R_{15} and R_{16}. This prevents the input transistors from saturating under worst case conditions of high current and high operating temperature.


V+ 7
OUTPUT 1
OUTPUT 8
INPUT 2
INPUT 3
RSET 6
RSET 5
V- 4
R1 500
R2 500
R3 50K
R4 50K
R5 50K
R6 150K
R7 150K
R8 75
R9 5K
R10 260
R11 340
R12 5K
R13 150K
R14 400
R15 1K
R16 1K
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
D1

*PIN CONNECTIONS SHOWN ON DIAGRAM AND TYPICAL APPLICATIONS ARE FOR TO-5 PACKAGE.

FIGURE 1. Schematic Diagram of the LM121

The rest of the devices comprise the turn-on and regulator circuitry. Transistors Q_{14}, Q_{15}, and Q_{16} form a 1.2V regulator for the bases of the input stage current source. By fixing the bases of the current sources at 1.2V, their output current changes proportional to absolute temperature. This compensates for the temperature sensitivity of the input stage transconductance. Temperature compensating the transconductance makes the preamp more useful in some applications such as an instrumentation amplifier and minimizes bandwidth variations with temperature. The regulator is started by Q_{18} and its operating current is supplied by Q_{17} and Q_9, Figure 2 shows the LM121 chip.

Offset Balancing

The LM121 was designed to operate with an offset balancing network connected to the current source transistors. The method of balancing the offset also minimizes the drift of the preamp. Unlike earlier devices such as the LM725, the LM121 depends only upon the highly predictable emitter base voltages of transistors to achieve low drift. Devices like the LM725 depend on the match between internal resistor temperature coefficient and the external null pot as well as the input stage transistors characteristics for drift compensation.

The input stage of the LM121 is actually two differential amplifiers connected in parallel, each having a fixed offset. The offset is due to different

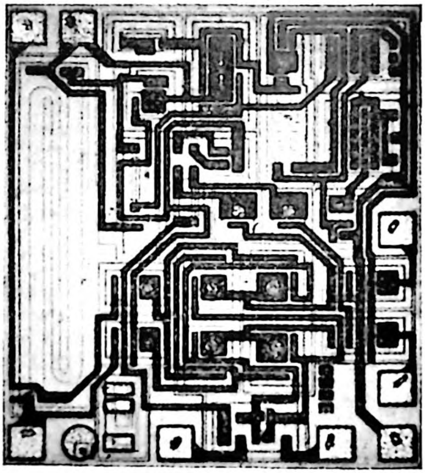


FIGURE 2. LM121 Chip

areas for the transistor emitters. The offset for each pair is given by:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{A_1}{A_2}$$

where k is Boltzmann's constant T is absolute temperature, q is the charge on an electron, and A_1 and A_2 are emitter areas. Because of the offset, each pair has a fixed drift. When the pairs are connected in parallel, if they match, the offsets and drift cancel. However, since matching is not perfect, the emitters of the pairs are not connected in parallel, but connected to independent current sources to allow offset balancing. The offset and drift effect of each pair is proportional to its operating current, so varying the ratio of the current from current sources will vary both the offset and drift. When the offset is nulled to zero, the drift is nulled to below 1μV/°C.

The offset balancing method used in the LM121 has several advantages over conventional balancing schemes. Firstly, as mentioned earlier, it theoretically zeros the drift and offset simultaneously. Secondly, since the maximum balancing range is fixed by transistor areas, the effect of null network variations on offset voltage is minimized. Resistor shifts of one percent only cause a 30μV shift in offset voltage on the LM121, while a one percent shift in collector resistors on a standard diff amp causes a 300μV offset change. Finally, it allows the value of the null network to set the operating current.

Achieving Low Drift

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted. In many cases, the low drift of the op amp is completely swamped by external effects while the amplifier is blamed for the high drift.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Whenever dissimilar metals are joined, a thermocouple results. The voltage generated by the thermocouple is proportional to the temperature difference between the junction and the measurement end of the metal. This voltage can range between essentially zero and hundred of microvolts per degree, depending on the metals used. In any system using integrated circuits a minimum of three metals are found: copper, solder, and kovar (lead material of the IC).

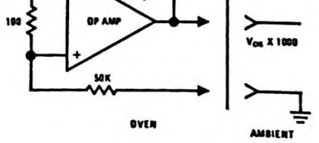
Nominally, most parts of a circuit are at the same temperature. However, a small temperature gradient can exist across even a few inches — and this is a big problem with low level signals. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally are the package-to printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

For example, a very low drift amplifier was constructed and the output monitored over a 1 minute period. During the 1 minute it appeared to have input referred offset variations of ±5μV. Shielding the circuit from air currents reduced this to ±0.5μV. The 10μV error was due to thermal gradients across the circuit from air currents.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or managanin are best since they only generate about 2μV/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50μV error. Most precision resistors use different material for different ranges of resistor values. It is not unexpected that resistors differing by a factor of 1000, do not track perfectly with temperature. For best results insure that the gain fixing resistors are of the same material or have tracking temperature coefficients.

Testing low drift amplifiers is also difficult. Standard drift testing techniques such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method — do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signals through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The circuit in Figure 3 will yield good results if well constructed.



*OP AMP SHOWN IN FIGURE 9.

FIGURE 3. Drift Measurement Circuit

Performance

It is somewhat difficult to specify the performance of the LM121 since it is programmable over a wide range of operating currents. Changing the operating current varies gain, bias current, and offset current — three critical parameters in a high accuracy system. However, offset voltage and drift are virtually independent of the operating current.

Typical performance at an operating current of 20µA is shown in Table I. Figures 4 and 5 show how the bias current, offset current, and gain change as a function of programming current. Drift is guaranteed at 1µV/°C independent of the operating current.

TABLE I. Typical Performance at an Operating Current of 10µA Per Side

Offset Voltage	Nulled
Bias Current	7 nA
Offset Current	0.5 nA
Offset Voltage Drift	0.3µV/°C
Common Mode Rejection Ratio	125 dB
Supply Voltage Rejection Ratio	125 dB
Common Mode Range	±13V
Gain	20V/V
Supply Current	0.5 mA

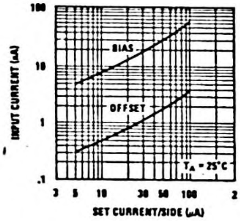


FIGURE 4. Bias and Offset Current vs Set Current

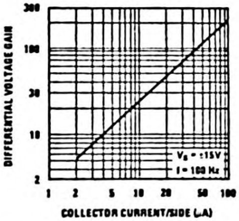


FIGURE 5. Gain vs Set Current

Over a temperature range of −55°C to +125°C the LM121 has less than 1µV/°C offset voltage drift when nulled. It is important that the offset voltage is accurately nulled to achieve this low drift. The drift is directly related to the offset voltage with 3.8µV/°C drift resulting from every millivolt of offset. For example, if the offset is nulled to 100µV, about 0.4µV/°C will result — or twice the typically expected drift. This drift is quite predictable and could even be used to cancel the drift elsewhere in a system. Figure 6 shows drift as a function of offset voltage. For critical applications selected devices can achieve 0.2µV/°C.

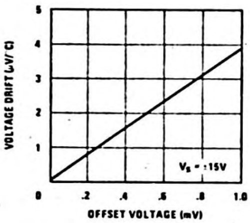


FIGURE 6. Drift vs Offset Voltage

Figures 7 and 8 show the bias current, offset current, and gain variation over a −55°C to +125°C temperature range. These performance characteristics do not tell the whole story. Since the LM121 is used with an operational amplifier, the op amp characteristics must be considered for over-all amplifier performance.

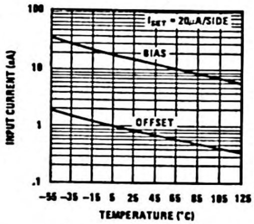


FIGURE 7. Bias and Offset Current vs Temperature

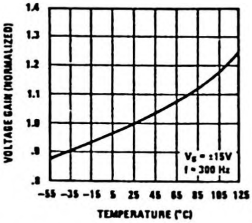


FIGURE 8. Gain vs Temperature for the LM121

Op Amp Effects

The LM121 is nominally used with a standard type of operational amplifier. The op amp functions as the second and ensuing stages of the amplifying system. When the LM121 is connected to an op amp, the two devices may be treated (and used) just as a single op amp. The inputs of the combination are the inputs of the LM121 and the output is from the op amp. Feedback, as with any op amp, is applied back to the inputs. Figure 9 shows the general configuration of an amplifier using the LM121.

The offset voltage and drift of the op amp used have an effect on overall performance and must be considered. (The bias and offset currents of today's op amp are low enough to be ignored.) Although the exact effects of the op amp stage are difficult and tedious to calculate, a few approximations will show the sources of drift.

Op amp drift is perhaps the most important source of error. Drift of the op amp is directly reduced by the gain of the LM121. The drift referred to the input is given by:

$$\text{input drift} = \frac{\text{op amp drift}}{\text{LM121 gain}} + \text{LM121 drift.}$$

If the op amp has a drift of 10μV/°C and the LM121 is operated at a gain of $A_V = 50$, there will be a 0.2μV/°C component of the total drift due to the op amp. It is therefore important that the LM121 be operated at relatively high gain to minimize the effects of op amp drift. Lower gains for the LM121 will give proportionately less reduction in op amp drift. Of course, a moderately low drift op amp such as the LM108A eases the problem.

Op amp offset voltage also has an effect on total drift. For purpose of analysis assume the LM121 to be perfect with no offset or drift of its own. Then any offset seen when the LM121 is connected to an op amp is due to the op amp alone. The offset is equal to:

$$\text{offset voltage} = \frac{\text{op amp offset}}{\text{LM121 gain}}$$

or the offset is reduced by the gain of the LM121. For example, with a gain of 50 for the LM121, 2 mV of offset on the op amp appears as 40μV of offset at the LM121 input. Unlike offset due to a mismatch in the LM121, this 40μV of offset does not cause any drift. However, when the system is nulled so the offset at the input of the LM121 is zero, 40μV of imbalance has been inserted into the LM121. The imbalance caused by nulling the offset induced by the op amp will cause a drift of about 0.14μV/°C. With the system nulled the drift due to op amp will cause a drift of about 0.15μV/°C. With the system nulled the drift due to op amp offset can be expressed as:

$$\text{drift } (\mu\text{V/°C}) = \frac{\text{op amp offset (mV)}}{\text{LM121 gain}} \; (3.6\mu\text{V/°C}).$$

In actual operation, drift due to op amp offsets will usually be better than predicted. This is because offset voltage and drift are not independent. With the LM121 there is a strong, predictable, correlation between offset and drift. Also, there is a correlation with op amps, but it is not as strong. The drift of the op amp tends to cancel the drift induced in the LM121 when the system is nulled.

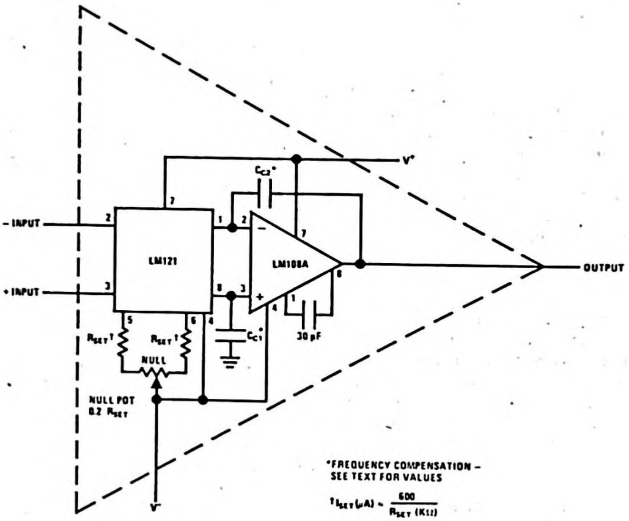
In the previous example the drift due to the op amp offset was 0.15μV/°C. If the op amp has a drift of 3.6μV/°C per millivolt of offset (like the LM121) it will have a drift of 7.2μV/°C. This drift is reduced by the gain of the LM121 ($A_V = 50$) to 0.14μV/°C. This 0.14μV/°C will cancel the 0.14μV/°C drift due to balancing the LM121. Since op amps do not always have a strong correlation between offset and drift, the cancellation of drifts is not total. Once again, high gain for the LM121 and a low offset op amp helps achieve low drifts.

Frequency Compensation

The additional gain of the LM121 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. This is because the additional gain introduced by the LM121 must be rolled-off before the phase shift through the LM121 and op amp reaches 180°. The additional compensation depends on the gain of the LM121 as well as the closed loop gain of the system. Two frequency compensation techniques are shown here that will operate with any op amp that is unity gain stable.

When the closed loop gain of the op amp with the LM121 is less than the gain of the LM121 alone, more compensation is needed. The worst case situation is when there is 100% feedback — such as a voltage follower or integrator — and the gain of the LM121 is high. When high closed loop gains are used — for example $A_V = 1000$ — and only an additional gain of 100 is inserted by the LM121, the frequency compensation of the op amp will usually suffice.

The basic circuit of the LM121 in Figure 9 shows two compensation capacitors connected to the op amp (disregarding the 30 pF frequency compensation for the op amp alone). The capacitor from pin



*FREQUENCY COMPENSATION – SEE TEXT FOR VALUES

†$I_{SET}(\mu A) = \frac{600}{R_{SET}\,(K\Omega)}$

FIGURE 9. General Purpose Amplifier Using the LM121

6 to pin 2 around the op amp acts as an integrating capacitor to roll off the gain. Since the output of the LM121 is differential, a second capacitor is needed to roll off pin 3 of the op amp. These capacitors are C_{C1} and C_{C2} in Figure 9.

With capacitors equal, the circuit retains good AC power supply rejection. The approximate value of the compensation capacitors is given by:

$$C_C = \frac{8}{10^6\,A_{CL}\,R_{SET}} \text{ farads}$$

where R_{SET} is the current set resistor from each current source and where A_{CL} is closed loop gain. Table II shows typical capacitor values.

An alternate compensation scheme was developed for applications requiring more predictable and smoother roll off. This is useful where the amplifier's gain is changed over a wide range. In this case C_{C1} is made large and connected to V^+ rather than ground. The output of the LM121 is rendered single ended by a 0.01μF bypass capacitor to V^+. Overall frequency compensation then is achieved by an integrating capacitor around the op amp:

$$\text{Bandwidth at unity gain} \cong \frac{12}{2\pi\,R_{SET}\,C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6\,R_{SET}}$$

TABLE II. Typical compensation capacitors for various operating currents and closed loop gains. Values given apply to LM101A, LM108, and LM741 type amplifiers.

CLOSED LOOP GAIN	CURRENT SET RESISTOR				
	120 kΩ	60 kΩ	30 kΩ	12 kΩ	6 kΩ
$A_V = 1$	68 pF	130 pF	270 pF	680 pF	1300 pF
$A_V = 5$	15 pF	27 pF	50 pF	130 pF	270 pF
$A_V = 10$	10 pF	15 pF	27 pF	68 pF	130 pF
$A_V = 50$	1 pF	3 pF	5 pF	15 pF	27 pF
$A_V = 100$		1 pF	3 pF	5 pF	10 pF
$A_V = 500$			1 pF	1 pF	3 pF
$A_V = 1000$					

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz. If closed loop gain is greater than unity "C" may be decreased to:

$$C = \frac{4}{10^6\, A_{CL}\, R_{SET}}$$

Applications

No attempt will be made to include precision op amp applications as they are well covered in other literature. The previous sections detail frequency compensation and drift problems encountered in using very low drift op amps. The circuit shown in Figure 9 will yield good results in almost any op amp application. However, it is important to choose the operating current properly. From the curves given it is relatively easy to see the effects of current changes. High currents increase gain and reduce op amp effects on drift. Bias and offset current also increase at high current. When the operating source resistance is relatively high, errors due to high bias and offset current can swamp offset voltage drift errors. Therefore, with high source impedances it may be advantageous to operate at lower currents.

Another important consideration is output common mode voltage. This is the voltage between the outputs of the LM121 and the positive power supply. Firstly, the output common mode voltage must be within the operating common mode range of the output op amp. At currents above 10μA there is no problems with the LM108, LM101, and LM741 type devices. Higher currents are needed for devices with more limited common mode range, such as the LM118. As the operating current is increased, the positive common mode limit for the LM121 is decreased. This is because there is more voltage drop across the internal 50k load resistors. The output common mode voltage and positive common mode limits are about equal and given by:

$$\begin{matrix}\text{Output common mode voltage} \\ \text{positive common mode limit}\end{matrix} \approx V^+ - 0.6V^+ \frac{0.65 \times 50\text{k}\Omega}{R_{SET}}$$

If it is necessary to increase the common mode output voltage (or limit), external resistors can be connected in parallel with the internal 50kΩ resistors. This should only be done at high operating currents (80μA) since it reduces gain and diverts part of the input stage current from the internal biasing circuitry. A reasonable value for external resistors is 50kΩ.

The external resistors should be of high quality and low drift, such as wirewound resistors, since they will affect drift if they do not track well with temperature. A 20ppm/°C difference in external resistor temperature coefficient will introduce an additional 0.3μV/°C drift.

An unusually simple gain of 1000 instrumentation amplifier can be made using the LM121. The amplifier has a floating, full differential, high impedance input. Linearity is better than 1%, depending upon input signal level with maximum error at maximum input. Gain stability, as shown in Figure 10, is about ±2% over a −55°C to +125°C temperature range. Finally, the amplifier has very low drift and high CMRR.

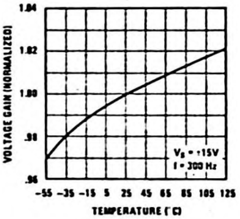
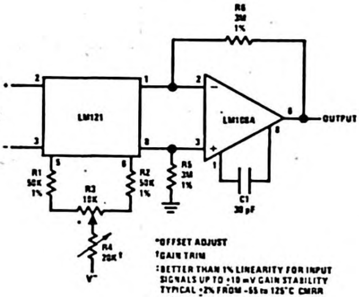


FIGURE 10. Instrumentation Amplifier Gain vs Temperature

Figure 11 shows a schematic of the instrumentation amplifier. The LM121 is used as the input stage and operated open-loop. It converts an input voltage to a differential output current at pins 1 and 8 to drive an op amp. The op amp acts as a current to voltage converter and has a single-ended output.



*OFFSET ADJUST

†GAIN TRIM

‡BETTER THAN 1% LINEARITY FOR INPUT SIGNALS UP TO ±10 mV GAIN STABILITY TYPICAL ±2% FROM −55 to 125°C CMRR 110 dB.

FIGURE 11. Gain of 1000 Instrumentation Amplifier

Resistors R_1 and R_2 with null pot R_3 set the operating current of the LM121 and provide offset adjustment. R_4 is a fine trim to set the gain at 1000. There is very little interaction between the gain and null pots.

This instrumentation amplifier is limited to a maximum input signal of ±10 mV for good linearity. At high signal levels the transfer characteristic of the LM121 become rapidly non-linear, as with any differential amplifier. Therefore, it is most useful as a high gain amplifier.

Since feedback is not applied around the LM121, CMRR is not dependent on resistor matching. This eliminates the need for precisely matched resistor as with conventional instrumentation amplifiers. Although the linearity and gain stability are not as good as conventional schemes, this amplifier will find wide application where low drift and high CMRR are necessary.

A precision reference using a standard cell is shown in Figure 12. The low drift and low input current of the LM121A allow the reference amplifier to buffer the standard cell with high accuracy. Typical long term drift for the LM121 operating at constant temperature is less than 2μV per 1000 hours.

To minimize temperature gradient errors, this circuit should be shielded from air currents. Good single-point wiring should also be used. When power is not applied, it is necessary to disconnect the standard cell from the input of the LM121 or it will discharge through the internal protection diodes.

CONCLUSIONS

A new preamplifier for operational amplifiers has been described. It can achieve voltage drifts as low as many chopper amplifiers without the problems associated with chopping. Operating current is programmable over a wide range so the input characteristics can be optimized for the particular application. Further, using a preamp and a conventional op amp allows more flexibility than a single low-drift op amp.

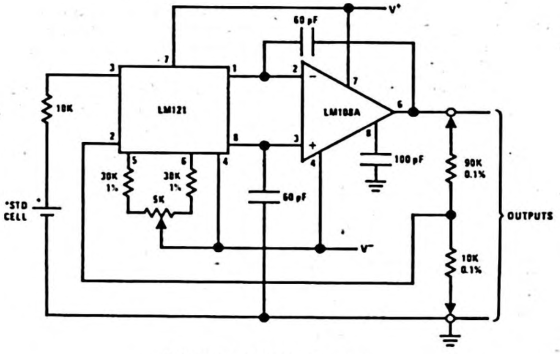


FIGURE 12. 10V Reference

LM1800
(LM1310, LM1310E*)
Phase Locked Loop FM Stereo Demodulator

National Semiconductor
Application Note 81
T. D. Isbell
D. S. Mishler
June 1973

INTRODUCTION

The LM1800 is a phase locked loop FM stereo demodulator built on a single monolithic die. In addition to separating left (L) and right (R) signal information from the detected IF output, the LM1800 features automatic stereo/monaural switching, 45 dB power supply rejection, and a 100 mA stereo indicator lamp driver. Particularly attractive is the low external part count and total elimination of coils. A single inexpensive potentiometer performs all tuning. The resulting FM stereo system delivers high fidelity sound while still meeting the cost requirements of inexpensive stereo receivers.

Figures 1 and 2 outline the role played by the LM1800 in the FM stereo receiver. The frequency domain plot shows that the composite input waveform contains L+R information in the audio band and L-R information suppressed carrier modulated on 38 kHz. A 19 kHz pilot tone, locked to the 38 kHz subcarrier at the transmitter, is also included. SCA information occupies a higher band but is of no importance in the consumer FM receiver.

The block diagram of the LM1800 shows the composite input signal applied to the audio frequency amplifier, which acts as a unity gain buffer to the decoder section. A second amplified signal is capacitively coupled to two phase detectors — one in the phase locked loop and the other in the stereo switching circuitry. In the phase locked loop, the output of the 76 kHz voltage controlled oscillator (VCO) is frequency divided twice (to 38 then 19 kHz), forming the other input to the loop phase detector. The output of the loop phase detector adjusts the VCO to precisely 76 kHz. The 38 kHz output of the first frequency divider becomes the regenerated subcarrier which demodulates L-R information in the decoder section. The amplified composite and an "in phase" 19 kHz signal, generated in the phase locked loop, drive the "in phase" phase detector. When the loop is locked, the DC output voltage of this phase detector measures pilot amplitude. For pilot signals sufficiently strong to enable good stereo reception the trigger latches, applying regenerated subcarrier to the decoder and powering the stereo indicator lamp. Hysteresis, built into the trigger, protects against erratic stereo/monaural switching and the attendant lamp flicker.

In the monaural mode (electronic switch open) the decoder outputs duplicate the composite input signal except that the de-emphasis capacitors (from pins 3 and 6 to ground) roll off with the load resistors at 2 kHz. In the stereo mode (electronic switch closed), the decoder demodulates the L-R information, matrixes it with the L+R information, then delivers buffered separated L and R signals to output pins 4 and 5 respectively.

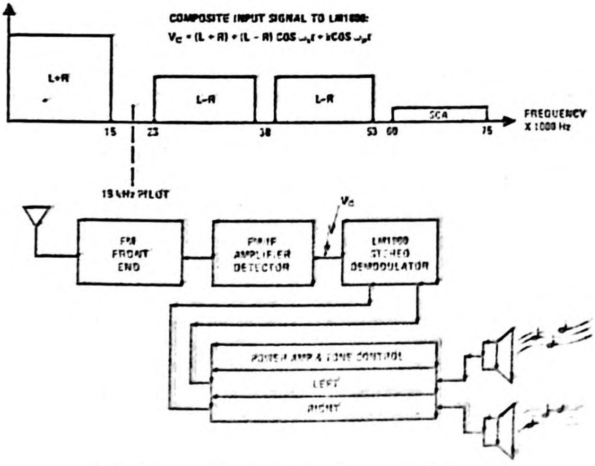


FIGURE 1. FM Receiver Block Diagram and Frequency Spectrum of LM1800 Input Signal

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*The information contained in this application note also generally applies to LM1310, LM1310E.

CIRCUIT DESCRIPTION

The complex circuit schematic of Figure 13 is more easily understood by reducing it to four subsections:

- Regulator and Audio Amplifier
- Phase Locked Loop
- Stereo/Monaural Switching Circuitry
- Decoder and Output Section

Regulator and Audio Amplifier

Transmission of power supply ripple and noise has plagued users of integrated FM stereo demodulators in the past. The introduction of a voltage regulator on the chip, along with improvements in the decoder output circuitry, provides excellent supply rejection, eliminating the need for costly supply filtering. Figure 3 shows an equivalent schematic of the 5.8V regulator. Z_2 holds the voltage across

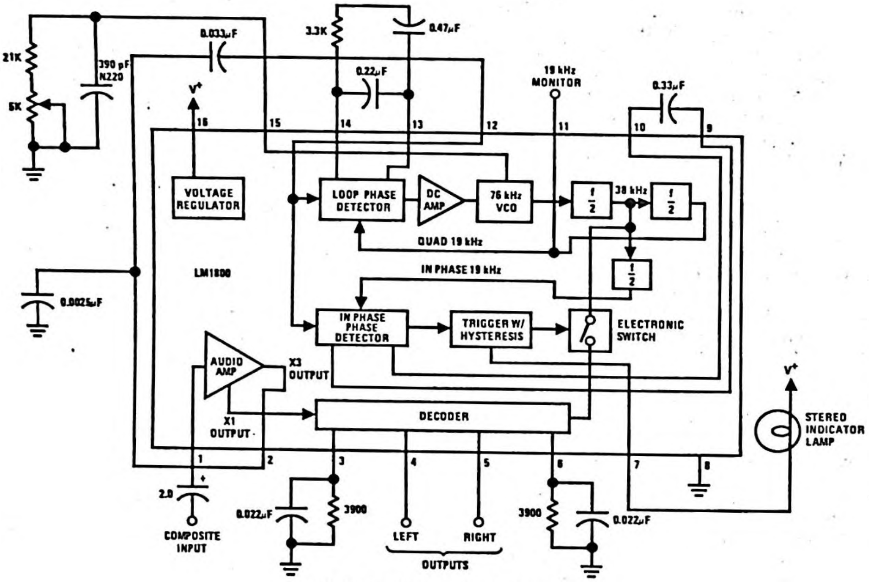

21K
5K
390 pF N220
0.033μF
3.3K
0.47μF
0.22μF
19 kHz MONITOR
0.33μF
V+
16
15
14
13
12
11
10
9
VOLTAGE REGULATOR
LOOP PHASE DETECTOR
DC AMP
76 kHz VCO
f/2
38 kHz
f/2
QUAD 19 kHz
IN PHASE 19 kHz
f/2
LM1800
0.0025μF
IN PHASE PHASE DETECTOR
TRIGGER W/ HYSTERESIS
ELECTRONIC SWITCH
AUDIO AMP
X3 OUTPUT
X1 OUTPUT
DECODER
V+
STEREO INDICATOR LAMP
1
2
3
4
5
6
7
8
2.0
COMPOSITE INPUT
0.022μF
3900
LEFT
RIGHT
OUTPUTS
3900
0.022μF

FIGURE 2. LM1800 Block Diagram

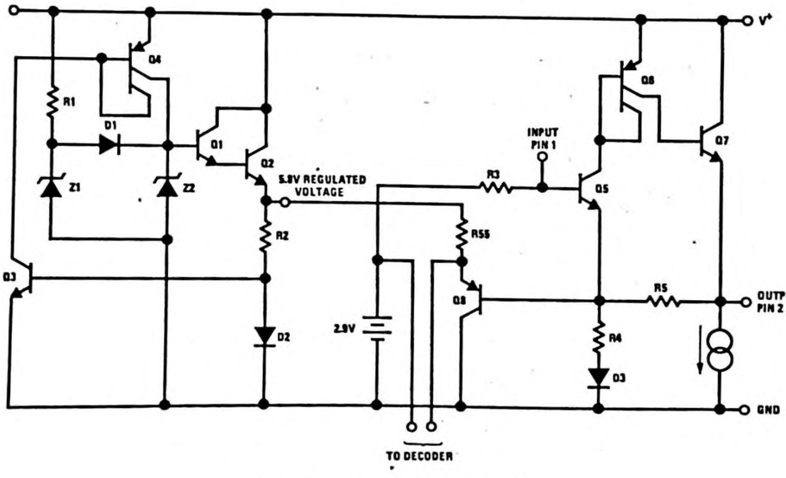

V+
Q4
R1
D1
Q1
Q2
Z1
Z2
5.8V REGULATED VOLTAGE
R2
Q3
D2
Q6
Q7
INPUT PIN 1
R3
Q5
R55
Q8
2.9V
R5
OUTPUT PIN 2
R4
D3
GND
TO DECODER

FIGURE 3. Regulator and Audio Amplifier

R_2 constant, thereby establishing a constant current through D_2, Q_3 and Q_4. The current through Z_2 then depends on the voltage drop across Z_2 and not on the supply line. R_1, Z_1 and D_1 assure startup after which the voltage across D_1 drops to zero, disconnecting R_1 from the remainder of the regulator circuitry.

The audio amp is biased internally by 2.9V through R_3 to the base of Q_5. Since the emitter current of Q_5 is much less than that of Q_7 and the base current of Q_8 is also negligible, current through R_4 approximately equals that through R_5. The DC quiescent voltage at the output pin becomes:

$$V_{P2} = V_{E5} + (V_{E5} - 0.7)\ R_5/R_4 = 5.4 \text{ volts}$$

and gain to a dynamic input is:

$$A_{\text{pin 1 - pin 2}} = 1 + R_5/R_4 = 3.0$$

A second signal path of unity gain exists through Q_5 and Q_8. The potential at Q_8's emitter is also approximately 2.9V, providing conveniently biased drive to the decoder section. R_3 sets the input resistance at typically 45 kΩ.

Phase Locked Loop

A phase locked loop is a feedback system comprised of a phase detector, a low pass filter, and an error amplifier in the forward transmission path while a voltage controlled oscillator provides the feedback element. Figure 4 illustrates a simplified loop. Without an input signal the error voltage drops to zero. The VCO then oscillates at some free running frequency, f_O. As an input signal is introduced, the phase detector compares the phase (and frequency, since frequency is the time derivative of phase) of the input signal with that of the VCO, generating an error voltage related to the frequency difference. The error signal is filtered and amplified before it is applied to the control input of the VCO. The control voltage forces the VCO frequency to move in the direction that reduces the frequency difference between the input signal and f_O. For free running frequencies sufficiently close to the incoming signal, the nature of loop feedback causes the VCO to synchronize to exactly the incoming frequency. Some finite phase difference exists between the two signals. This phase difference is necessary to generate the corrective error voltage for the VCO.

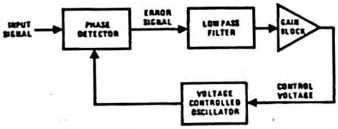


FIGURE 4. Basic Phase Locked Loop Block Diagram

The LM1800 operates on precisely this principle except that the VCO free runs at approximately four times the frequency of the incoming pilot. Two frequency dividers provide a signal at the phase detector input sufficiently close in frequency to the 19 kHz pilot tone to accomplish lock. The loop provides sufficient gain to keep the phase error small, and the frequency dividers generate accurate 50% duty cycle waveforms, both necessary requirements for good stereo demodulation.

VCO

Consider the voltage controlled oscillator scheme outlined in Figure 5. At turn-on the non-inverting input rises rapidly to 1.2V as set by the resistor divider (R_{13}/R_{15}), while the external capacitor holds the inverting input low. The output quickly rises to 5.8V and begins charging the capacitor through R_{11}. The output simultaneously lifts the non-inverting input rapidly to 4.7V. When the voltage across the capacitor also reaches 4.7V, the output drops low, reverse biasing the diodes while the capacitor begins discharging through the potentiometer. With the output low, the non-inverting input is again resistively set at 1.2V until the capacitor discharges and the cycle repeats. The capacitor voltage decays about twenty times slower than it charges, resulting in a repetition rate dominated by the external RC time constant.

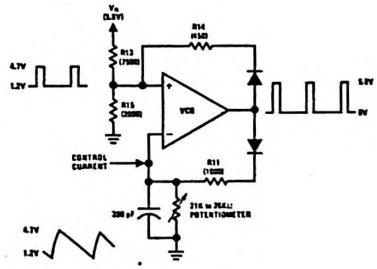


FIGURE 5. Equivalent Circuit of VCO

When the VCO is in its high state, the output is clamped at the regulated voltage. This causes the temperature coefficient of the trip points to be dependent on only the regulated voltage, resulting in an oscillation frequency quite independent of temperature.

Figure 6 details the frequency dividers used to transform the short duty cycle 76 kHz waveform into precisely 50% duty cycle 38 and 19 kHz waveforms. To understand their operation, first consider Q_{24}/Q_{25} saturated while Q_{23}/Q_{26} are in cutoff. As the trigger goes low the collector voltage for Q_{25}/Q_{26} collapses and conduction in them ceases. Since Q_{23}/Q_{24} are bistable by themselves, Q_{24} remains saturated and Q_{23} cutoff. With the trigger in this low state, the base of Q_{24} sits at one base-emitter voltage (0.7V) while the base of Q_{23} is at the saturation voltage of Q_{24}

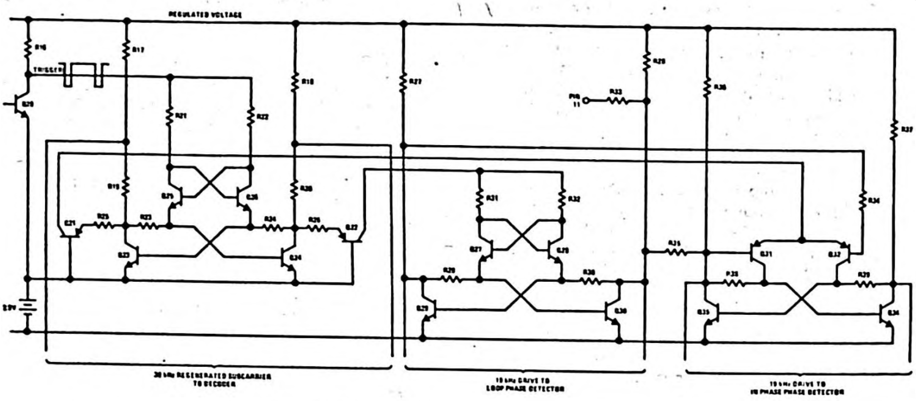

REGULATED VOLTAGE
TRIGGER
R16
R17
R18
R27
R28
R30
R33
PIN 11
R37
R21
R22
R19
R20
R31
R32
R34
Q20
Q25
Q26
Q21
Q22
Q23
Q24
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
R25
R23
R24
R26
R35
2.2V
38 kHz REGENERATED SUBCARRIER TO DECODER
19 kHz DRIVE TO LOOP PHASE DETECTOR
19 kHz DRIVE TO IN PHASE PHASE DETECTOR

FIGURE 6. Frequency Dividers

(0.2V). On the rising edge of the trigger pulse, Q_{26} conducts before Q_{25} because of the different voltages on their emitters. Q_{26} saturates and drives enough current through R_{24} to saturate Q_{23} while Q_{24} goes to cutoff. Thus Q_{23}/Q_{24} change state on every rising edge of a trigger pulse, dividing the repetition rate of the trigger signal by two. The other two frequency dividers function similarly except that the third one is slaved in quadrature with the second. Figure 7 shows the waveforms throughout the divider string.

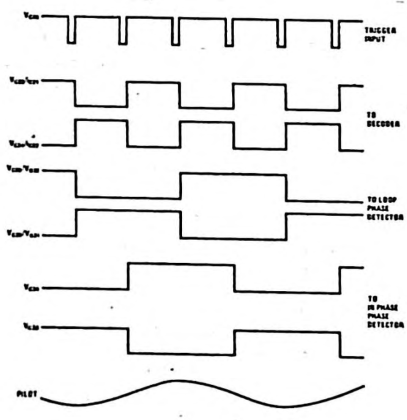

TRIGGER INPUT
TO DECODER
TO LOOP PHASE DETECTOR
TO IN PHASE PHASE DETECTOR
PILOT

FIGURE 7. Frequency Divider Waveforms

Loop Phase Detector

The loop phase detector is shown equivalently in Figure 8. Consider the loop phase detector where the toggle is driven in quadrature with the pilot. The waveforms show that zero volts DC appears across the capacitor. Any deviation from this quadrature relationship produces a voltage, which is a function of phase difference, across the capacitor. A second condition results when the toggle is driven in phase with the pilot. In this case the DC voltage across the capacitor measures pilot tone amplitude and is used to drive the stereo-monaural switching circuitry.

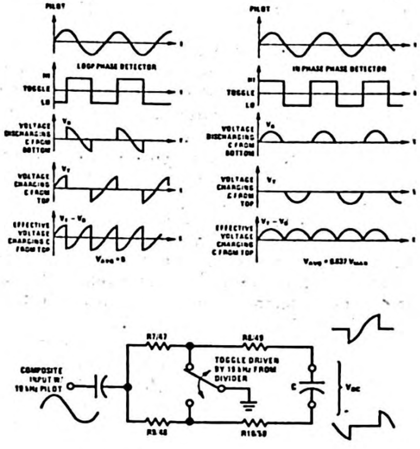

PILOT
LOOP PHASE DETECTOR
IN PHASE PHASE DETECTOR
HI
TOGGLE
LO
VOLTAGE DISCHARGING C FROM BOTTOM
VOLTAGE CHARGING C FROM TOP
EFFECTIVE VOLTAGE CHARGING C FROM TOP
V_avg = 0
V_avg = 0.637 V_max
R7/47
R8/49
R9/48
R10/50
COMPOSITE INPUT W/ 19 kHz PILOT
TOGGLE DRIVEN BY 19 kHz FROM DIVIDER
C
V_DC

FIGURE 8. Phase Detector Performance

The DC amplifier in the phase locked loop is standard differential with push-pull output, maintaining excellent temperature stability in the loop.

Stereo/Monaural Switching Circuitry

Composite inputs sufficiently large for good quality stereo switch the LM1800 into the stereo mode via the circuitry of Figure 9. The differential pair Q_{47}/Q_{48} is driven by the DC output of the "in phase" phase detector. When the phase locked loop is locked, this differential input voltage to Q_{47}/Q_{48} is proportional to pilot amplitude (as explained in previous section and Figure 8). The emitter area of Q_{47} is five times larger than that of Q_{48}, building in 40 mV offset voltage. Until the base of Q_{48} is 40 mV higher than the base of Q_{47}, collector current in Q_{47} is larger than collector current in Q_{48}. Transistor design of Q_{49} constrains its beta to unity. So long as I_{C47} is larger than I_{C48}, Q_{49} remains in saturation (holding Q_{50} in cutoff). When the 40 mV offset voltage is overcome in Q_{47}/Q_{48}, Q_{49} comes out of saturation and Q_{50} enters conduction. Q_{50}, Q_{51}, D_5, and R_{51} form a positive feedback loop which regenerates when Q_{50} is allowed to conduct. R_{51} is chosen to halt the regeneration process at $I_{C51} = 30\mu A$. The latched loop current drives the lamp driver Darlington (Q_{54}/Q_{55}) as well as Q_{57} (via Q_{52} and Q_{53}). The signal to the decoder switches from common to differential mode 38 kHz and stereo demodulation begins. Should the input composite waveform decrease by 6 dB, the differential voltage back at Q_{47}/Q_{48} reduces to 20 mV. Under this condition the current flowing from Q_{49} into Q_{51} (as Q_{49} returns toward saturation) is sufficient to unlatch the loop, prohibiting drive to both Q_{57} and Q_{54}/Q_{55}. The signal driving the decoder returns to common mode 38 kHz and monaural reception resumes. R_{52} and Q_{56} limit cold lamp surge currents to about 250 mA.

Decoder and Output Section

The basic decoder section shown in Figure 10 has been used previously in the LM1304, LM1305, LM1307, LM1307E series, and is well described in reference 2. In an effort to transform the rigor into intuition, consider first Q_{43}, Q_{44}, and the emitter matrix resistors (R_{44}, R_{45}, R_{46}). Under small signal conditions the emitter of Q_{43} remains at a constant voltage while the emitter of Q_{44} tracks the composite input waveform applied to its base. Analysis of the simplified circuit shown in Figure 11 produces the current waveforms through R_{44} and R_{45}. These currents are not equal and opposite as in a standard multiplier because R_{46} in no way approximates a current source. Rather, the currents through R_{44} and R_{45} can be shown to be related by a constant:

$$K = I_{R44}/I_{R45} = R_{46}/(R_{45} + R_{46})$$

For NPN transistors operating in their active regions, collector current approximately equals emitter current, then:

$$I_{C43} = KI_{C44}$$

Since the upper quad transistors (Q_{39}, Q_{40}, Q_{41}, Q_{42}) operate as antiphase switches, the base current resulting through Q_{38} becomes the sum of I_{C44} gated by Q_{42} and I_{C43} gated by Q_{40}. These upper quad transistors alternately pass or block the currents flowing in Q_{43} and Q_{44}. This gating

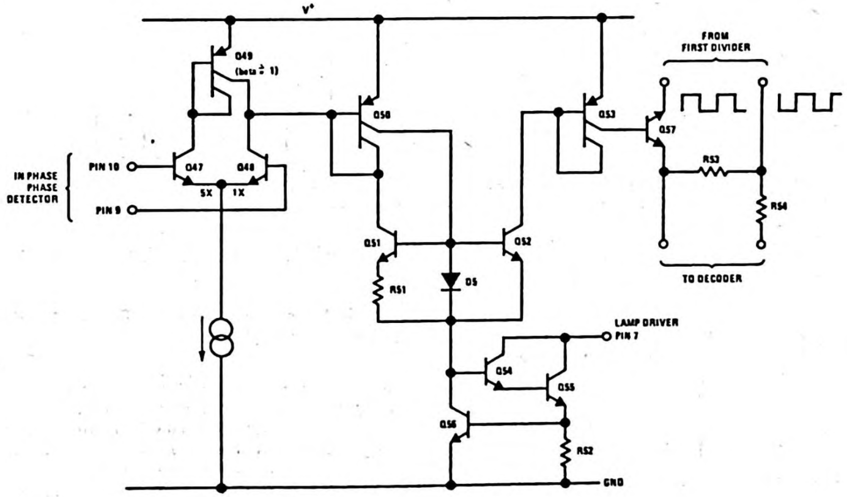


FIGURE 9. Stereo/Monaural Switch

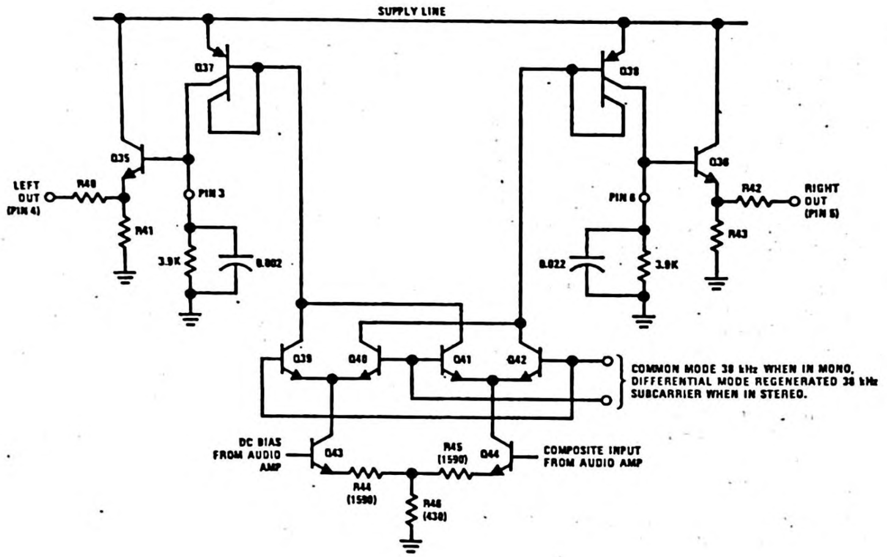

SUPPLY LINE
Q37
Q38
Q35
Q36
LEFT OUT (PIN 4)
R40
R41
PIN 3
3.9K
0.022
PIN 6
0.022
3.9K
R42
R43
RIGHT OUT (PIN 5)
Q39
Q40
Q41
Q42
COMMON MODE 38 kHz WHEN IN MONO, DIFFERENTIAL MODE REGENERATED 38 kHz SUBCARRIER WHEN IN STEREO.
DC BIAS FROM AUDIO AMP
Q43
R45 (1590)
Q44
COMPOSITE INPUT FROM AUDIO AMP
R44 (1590)
R46 (430)

FIGURE 10. Decoder and Output Section

action is represented mathematically in Figure 12. Applying the gating function to the currents in Q_{43} and Q_{44}:

$$I_{B38} = V_C \left[\frac{1}{2} - \frac{2}{\pi} \cos \omega_s t\right] - K V_C \left[\frac{1}{2} + \frac{1}{\pi} \cos \omega_s t\right]$$

where V_C = composite input signal

and ω_s = subcarrier (38 kHz)

Substituting the expression for V_C (given in Figure 1), carrying out the algebra, and retaining only the low frequency terms gives:

$$I_{B38} = L\left[0.5 - 0.5K - \frac{K+1}{\pi}\right] + R\left[0.5 - 0.5K + \frac{K+1}{\pi}\right]$$

Equating the coefficient of the left (L) term to zero, yields a value for K of 0.22. Thus designing the matrix resistors R_{44}, R_{45}, R_{46} to give this

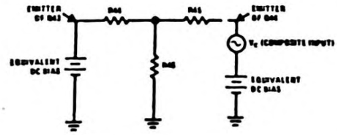
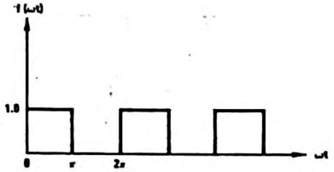

EMITTER OF Q43
R44
R45
EMITTER OF Q44
V_c (COMPOSITE INPUT)
EQUIVALENT DC BIAS
R46
EQUIVALENT DC BIAS

FIGURE 11. Equivalent Circuit for Decoder Matrix

value for K cancels all left information from the Q_{38} current. The base current of Q_{38} then is proportional to the right (R) separated signal.



$$f(\omega t) = \frac{1}{2} + \frac{2}{\pi}\Sigma\frac{1}{n}\cos n\omega t$$

$$= \frac{1}{2} + \frac{2}{\pi}\cos\omega t + \ldots$$

FIGURE 12. Fourier Analysis of Decoder Switching Waveform

Similar analysis can be performed to show that the base current of Q_{37} contains only left (L) separated signal. Amplification and level shifting of these base currents occurs in fixed beta transistors Q_{37} and Q_{38}, and the resultant currents drive external grounded loads at pins 3 and 6. Since the collector currents of Q_{37} and Q_{38} depend only on their respective base currents, supply ripple and noise are rejected from the output pins. Q_{35} and Q_{36} serve as output buffers with R_{40} and R_{42} setting the output resistance at typically 1300Ω.

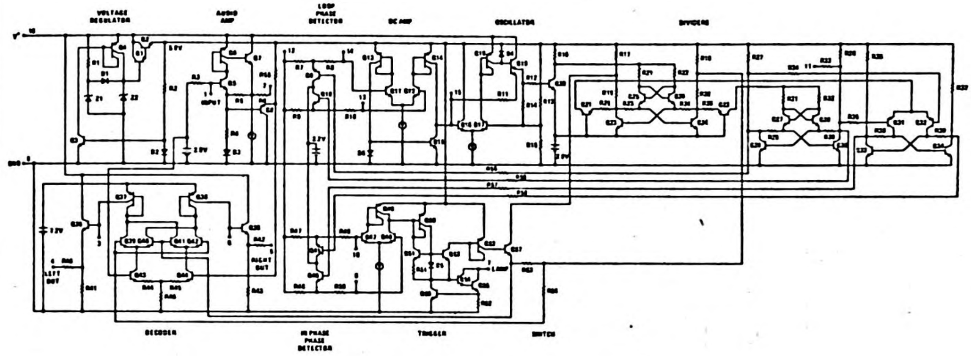


FIGURE 13. LM1800 Equivalent Schematic

In the monaural mode the upper quad transistors are driven by a common mode signal which causes all four transistors to conduct equally. This passes the composite input directly to the outputs where the de-emphasis capacitors serve to roll off the higher frequency unwanted information. Further, the LM1800 offers improved distortion over earlier integrated demodulators. As the signal driving the base of Q_{44} increases in amplitude, the AC currents through Q_{43} and Q_{44} become a significant percentage of the DC bias currents. In this manner the transconductance of Q_{43} and Q_{44} is modulated by the incoming signal resulting in second harmonic distortion. To reduce this effect, the base bias potentials of Q_{43} and Q_{44} and the matrix resistor values have been raised above the levels used in earlier demodulators. The loss in gain that this implies is recovered in the PNP level shifting transistors.

CIRCUIT PERFORMANCE

The circuit in Figure 14 illustrates the simplicity of designing an FM stereo demodulation system using the LM1800. R_3 and C_3 establish an adequate loop capture range and a low frequency well damped natural loop resonance. C_8 has the effect of shunting phase jitter, a dominant cause of high frequency channel separation problems. Recall that the 38 kHz subcarrier regenerates by phase locking the output of a 19 kHz divider to the pilot tone. Time delays through the divider result in the 38 kHz waveform leading the transmitted subcarrier. Addition of capacitor C_9 ($0.0025\mu F$) at pin 9 introduces a lag at the input to the phase lock loop, compensating for these frequency divider delays. The output resistance of the audio amplifier is designed at 500Ω to facilitate this connection.

Table I and Figures 15 through 27 detail typical performance resulting from this basic hookup. The excellent supply rejection characteristics shown, coupled with the fact that supply current drain is nearly independent of supply voltage, somewhat simplifies receiver power supply requirements. The low drain current, even for a 24V supply, results in cooler circuit operation and increased reliability. Figure 22 shows that increasing the size of input coupling capacitor C_6 improves low frequency channel separation by reducing the phase shift of the lower frequency components in the composite waveform.

Figure 27 illustrates an interesting characteristic of the LM1800: channel separation increases as the VCO is detuned in either direction. The separation peaks change in size for different signal frequencies and change in position (% detuning) for changing composite amplitudes. If the VCO free running frequency is set at precisely 19 kHz, separation remains constant over a wide range of composite amplitude levels, signal frequencies, temperature changes, and component drifts. The 19 kHz monitor available to the customer at pin 11 can be fed into a frequency counter for accurate adjustment of the VCO free running frequency. If a frequency counter is not available, the VCO can be adjusted by utilizing the fact that capture range is symmetrical about the incoming pilot:

(a) rotate frequency adjust pot full CCW
(b) insert weak composite input signal
(c) rotate pot. CW until stereo lamp comes on, note position of pot (R_x)
(d) remove composite and rotate pot full CW
(e) reinsert weak composite input signal
(f) rotate pot CCW until stereo lamp comes on again, note position of pot (R_y)
(g) set pot midway between R_x and R_y.

Figure 28 is included for the user who is willing to sacrifice some performance, particularily channel separation at high input levels and low frequencies to eliminate two external capacitors and reduce the electrolytic input coupling cap size.

On either circuit, some improvement in channel separation can be attained by altering the VCO

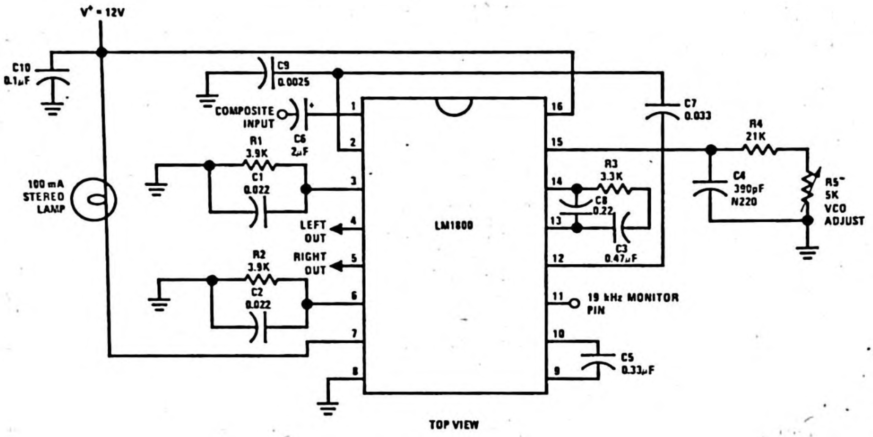

V⁺ = 12V
C10
0.1µF
C9
0.0025
COMPOSITE
INPUT
C6
2µF
R1
3.9K
C1
0.022
100 mA
STEREO
LAMP
LEFT
OUT
RIGHT
OUT
R2
3.9K
C2
0.022
LM1800
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
C7
0.033
R4
21K
R3
3.3K
C8
0.22
C3
0.47µF
C4
390pF
N220
R5
5K
VCO
ADJUST
19 kHz MONITOR
PIN
C5
0.33µF
TOP VIEW

FIGURE 14. Typical Application Circuit

TABLE 1.

PARAMETERS	CONDITIONS	TYP	UNITS
Supply Current	Lamp "OFF"	21	mA
Lamp Driver Saturation Voltage	100 mA Lamp Current	1.3	V
Lamp Driver Leakage Current		1	nA
Pilot Level for Lamp "ON"	Pin 11 Adjusted for 19 kHz ±10 Hz	16	mV
Pilot Level for Lamp "OFF"	Pin 11 Adjusted for 19 kHz ±10 Hz	8	mV
Stereo Lamp Hysteresis		6	dB
Stereo Channel Separation	100 Hz (Note 1)	40	dB
	1000 Hz (Note 1)	45	dB
	10000 Hz (Note 1)	45	dB
Monaural Channel Unbalance	200 mVrms, 1000 Hz Input	0.3	dB
Recovered Audio	200 mVrms, 400 Hz Input	190	mVrms
Total Harmonic Distortion	500 mVrms, 1000 Hz Monaural Input	0.5	%
Capture Range	25 mV of 19 kHz pilot	±4	% of f_0
Supply Ripple Rejection	600 mVrms, 200 Hz Ripple	45	dB
Dynamic Input Resistance		45	kΩ
Dynamic Output Resistance		1300	Ω
SCA Rejection	200 mVrms Composite at 67 kHz	50	dB
Ultrasonic Frequency Rejection	Combined 19 and 38 kHz	33	dB

Note 1: The stereo input signal is made by summing 123 mVrms left or right modulated signal with 25 mVrms of 19 kHz pilot tone, measuring all voltages with an average responding meter calibrated in rms, the resulting waveform is about 800 mVp-p. VCO adjusted to 19kHz ±10Hz.

FIGURE 15. Supply Drain

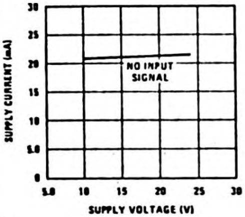


FIGURE 16. Total Harmonic Distortion

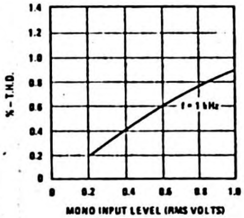


FIGURE 17. Supply Ripple Rejection

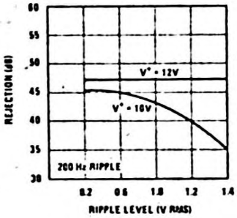


FIGURE 18. Supply Ripple Rejection

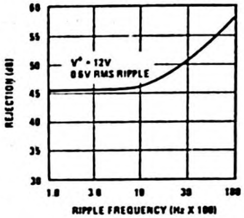


FIGURE 19. VCO Temperature Stability

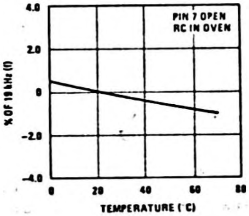


FIGURE 20. VCO Supply Sensitivity

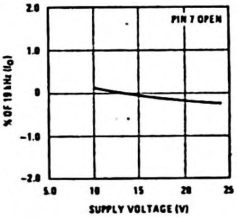


FIGURE 21. Pilot Level For Lamp On

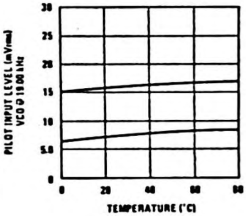


FIGURE 22. Channel Separation

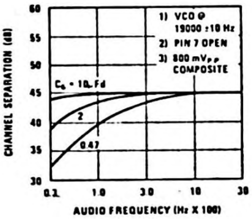


FIGURE 23. Channel Separation

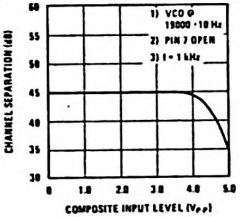


FIGURE 24. Output Frequency Spectrum

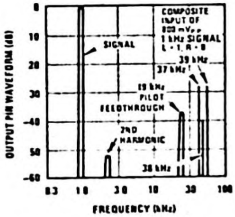


FIGURE 25. Capture Range

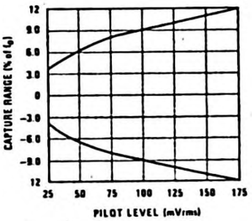


FIGURE 26. Lamp Driver Characteristics

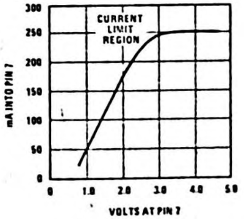
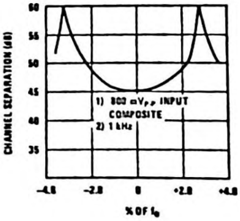


FIGURE 27. Channel Separation and VCO Tuning



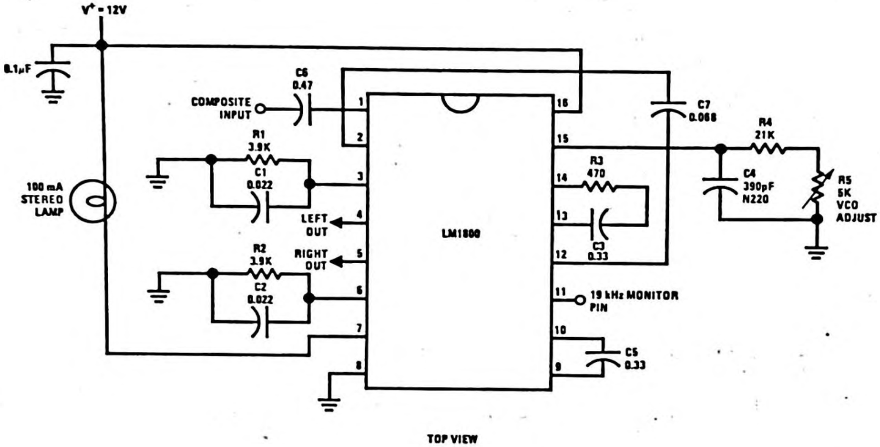

V⁺ = 12V
0.1µF
100 mA STEREO LAMP
COMPOSITE INPUT
C6 0.47
R1 3.9K
C1 0.022
LEFT OUT
R2 3.9K
C2 0.022
RIGHT OUT
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
LM1800
C7 0.068
R4 21K
R3 470
C4 390pF N220
R5 5K VCO ADJUST
C3 0.33
19 kHz MONITOR PIN
C5 0.33
TOP VIEW

FIGURE 28. Minimum Parts Count Application Circuit

slightly. The loop gain can be shown to decrease for a decrease in VCO resistance (R_4 + R_5 in Figure 14). Maintaining a constant RC product, while increasing the capacity from 390 pF to 510 pF narrows the capture range by about 25%. Although the resulting system has slightly improved channel separation, it is more sensitive to VCO tuning.

When the circuits so far described are connected in an actual FM receiver, channel separation often suffers due to imperfect frequency response of the IF stage. The input lead network of Figure 29 can be used to compensate for roll off in the IF and will restore high quality stereo sound. Should a receiver designer prefer a stereo/monaural switching point different than those programmed into the LM1800 (pilot: 16 mVrms on, 8.0 mVrms off typical), the circuit of Figure 30 provides the desired flexibility.

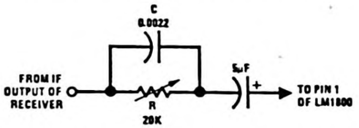

C
0.0022
FROM IF OUTPUT OF RECEIVER
R
20K
5µF
+
TO PIN 1 OF LM1800

FIGURE 29. Compensation for Receiver IF Rolloff

The user who wants slightly increased voltage gain through the demodulator can increase the size of the load resistors (R_1 and R_2 of Figure 14 or 28), being sure to correspondingly change the de-emphasis capacitors (C_1 and C_2). Loads as high as 5600Ω may be used (gain of 1.4). Performance of the LM1800 is virtually independent of the supply voltage used (from 10 to 24V) due to the on chip regulator.

Although the circuit diagrams show a 100 mA indicator lamp, the user may desire an LED. This presents no problem for the LM1800 so long as a resistor is connected in series to limit current to a safe value for the LED. The lamp or LED can be powered from any source (up to 24V), and need not necessarily be driven from the same supply as the LM1800.

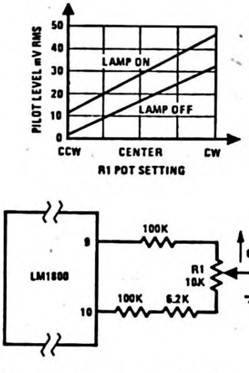


FIGURE 30. Stereo/Monaural Switch Point Adjustment

Utilization of the phase locked loop principle enables the LM1800 to demodulate FM stereo signals without the use of troublesome and expensive coils. The numerous features available on the demodulator make it extremely attractive in a variety of home and automotive receivers. Indeed the LM1800 represents a new generation in integrated stereo FM demodulators.

REFERENCES

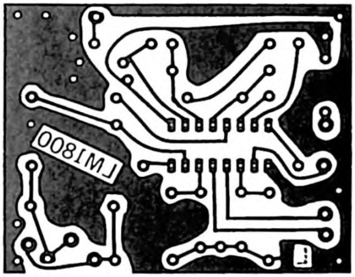
1. Blaser, L. and Cocke, W., *"The μA758, A Phase Locked Loop FM Stereo Multiplex Decoder."* Fairchild Application Note 319, June 1972.

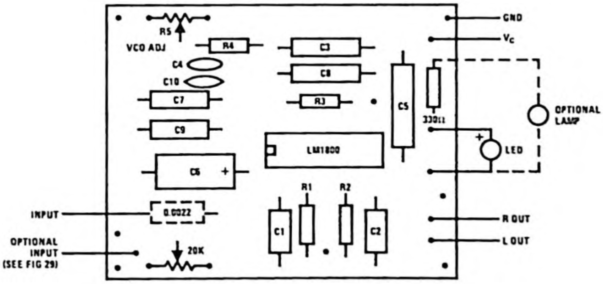
2. Hector Gasquet, *"A Monolithic Integrated FM Stereo Decoder System."* Motorola Application Note AN-432A.

3. Michael J. Gay, *"A Monolithic Phase-Lock-Loop Stereo Decoder."* IEEE Transactions on Broadcast and TV Receivers, Vol. BTR-17, No. 3, August 1971.

4. Thomas B. Mills, *"The Phase Locked Loop IC as a Communication System Building Block."* National Semiconductor Application Note AN-46, June 1971.

5. *"Phase Locked Loops Applications Book,"* Signetics Corporation, 1972.




R5
VCO ADJ
R4
C3
C4
C10
C8
C7
R3
C5
330Ω
OPTIONAL LAMP
C9
LM1800
LED
+
C6
+
R1
R2
INPUT
0.0022
C1
C2
OPTIONAL INPUT (SEE FIG 29)
20K
GND
V_c
R OUT
L OUT

Printed Circuit Board Layout for Circuit of Figure 14.

LM125, LM126, LM127 Precision Dual Tracking Regulators

National Semiconductor
Application Note 82
Todd Smathers
Nello Sevastopoulos
May 1974

INTRODUCTION

The LM125, LM126, and LM127 family of devices are precision, dual, tracking, monolithic voltage regulators. Each provides separate positive and negative regulated outputs, thus simplifying dual power supply designs. Operation requires few or no external components depending on the application. Internal settings provide fixed output voltages: the LM125 at ±15V, the LM126 at ±12V, and the LM127 at +5.0V and −12V for use in MOS applications.

Each regulator is protected from excessive internal power dissipation by a thermal shutdown circuit which turns off the regulator whenever the chip reaches a preset maximum temperature. Other features include both internal and external current limit sensing for device protection while operating with or without external current boost. For applications requiring more current than the internal current limit will allow, boosted operation is possible with the addition of a one NPN pass transistor per regulator. External resistors sense load current for controlling the limiting circuitry. Internal frequency compensation is provided on both positive and negative regulators. The internal voltage reference pin is brought out to facilitate noise filtering when desired.

CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the basic dual tracking regulator. A voltage reference establishes a fixed dc level, independent of supply or temperature variations, at the non-inverting input to the negative regulator Error Amplifier. The Error Amplifier drives the Output Control Circuit which includes the high current output transistors, current limiting, and thermal shutdown circuitry.

The negative regulator output voltage is established by comparing the Voltage Reference against a fraction of the output as set by R_A and R_B. To achieve the desired tracking action of the positive regulator, a voltage established between the positive and negative regulator outputs by resistors R_C and R_D is compared to ground by the positive regulator Error Amplifier. This insures that the positive regulator output voltage will always equal the negative regulator output voltage multiplied by the ratio of R_C to R_D. This ratio is unity for the LM125 (V_O = ±15V), and LM126 (V_O = ±12V), and equals 5/12 for the LM127. The positive regulator Output Control Circuit is essentially the same as that in the negative regulator.

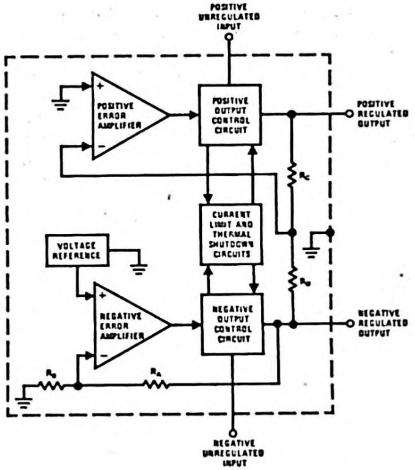

POSITIVE UNREGULATED INPUT
+
−
POSITIVE ERROR AMPLIFIER
POSITIVE OUTPUT CONTROL CIRCUIT
POSITIVE REGULATED OUTPUT
R_C
CURRENT LIMIT AND THERMAL SHUTDOWN CIRCUITS
VOLTAGE REFERENCE
R_D
+
−
NEGATIVE ERROR AMPLIFIER
NEGATIVE OUTPUT CONTROL CIRCUIT
NEGATIVE REGULATED OUTPUT
R_B
R_A
NEGATIVE UNREGULATED INPUT

FIGURE 1. Block Diagram for the Basic Dual Tracking Regulator

The current limit and thermal shutdown circuitry sense the output load current and die temperature respectively and switch off all output drive capability upon reaching their predetermined limits.

Figure 2 gives a more detailed picture of the negative regulator circuitry. The temperature compensated reference voltage appears at the non-inverting input of the differential amplifier, Q19 and Q20, while an error signal proportional to any change in output voltage is applied to the other input. This error signal is amplified by the differential amplifier, Q19 and Q20, and by the triple Darlington Q21, Q22, Q23 to produce a current change through R13 and R17 which brings the output voltage back to its original value. Loop gain is high, typically 88 dB at low output currents, so a 30 pF compensating capacitor is used to guarantee stability. Since $-V_{OUT}$ is the output of a high gain feedback amplifier, high supply rejection is ensured.

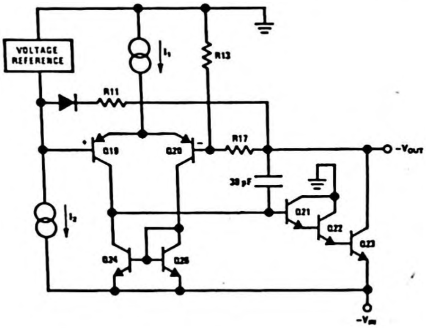


FIGURE 2. Simplified Negative Regulator

Figure 3 shows the basic positive regulator. This is actually an inverting operational amplifier. The negative regulated voltage ($-V_{OUT}$) is applied to the current summing input through R14 while the output ($+V_{OUT}$) is fed-back via R9. Then $+V_{OUT}$ is simply $-$ (R9/R14) ($-V_{OUT}$). Any change in the positive regulator output will create an error signal at the base of Q10 which will be amplified and sent to the voltage follower, Q4 and Q5, forcing the output voltage to track the input voltage. Here the loop gain is on the order of 66 dB so a compensating capacitor of approximately 20 pF is used to ensure amplifier stability.

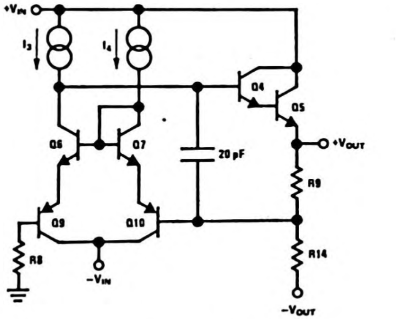


FIGURE 3. Simplified Positive Regulator

The circuitry used for regulator start up, biasing, temperature sensing, and thermal shutdown is shown in Figure 4. The field effect transistor Q28, is initially ON allowing the negative input voltage to force current through zener diode Q34. When enough current flows to fully establish the zener voltage, transistor Q29, Q30 and Q31 turn on and bias up all current sources. The zener voltage also decreases the gate to source voltage of the FET, pinching it off to a lower current value to reduce quiescent power dissipation.

The thermal sensing and shutdown circuitry is comprised of Q34, Q29, Q35, Q32, Q37, Q38, R27, R29, R30, R31, and R33. The voltage divider made up of R29 and R30 provides a relatively fixed bias voltage V_1 at the bases of Q35 and Q36, holding them in the OFF state. When the chip temperature increases to a maximum permissible level, the base to emitter voltage of Q35 and/or Q36 will have decreased sufficiently so that V_1 is now high enough to turn them ON. This causes a voltage drop across R27 sufficient to turn on Q32 which switches Q37 and Q38 to a conducting state shunting all output drive current to $-V_{IN}$. The regulator output voltages are then clamped to zero. Transistors Q35 and Q36 are located on the chip near the regulator output devices so they will see the maximum temperatures reached on the chip, ensuring that neither regulator will ever see more than this preset maximum temperature. The collectors of Q35 and Q36 are tied together so that if either regulator reaches the thermal shutdown temperature, both regulators will shutdown. This ensures that the device can never be destroyed because of excessive internal power dissipation in either regulator.

Figure 5 shows the current limiting circuitry used in the positive regulator; the negative regulator current limiter is identical. The internal current limiter is comprised of Q8 and R5; the external current limiter is comprised of Q11 and an external resistor R_{CL}. Both operate in a similar manner. As the output current through Q5 increases, the voltage drop across resistor R5 eventually turns ON Q8 and shunts all base drive away from the output devices, Q4 and Q5. The maximum load current available with this circuit is approximately 250 mA at $T_J = 25°C$ (see Figure 9).

The external current limiting circuit works in a similar manner. Here the output current is sensed across the external resistor R_{CL}. When the voltage

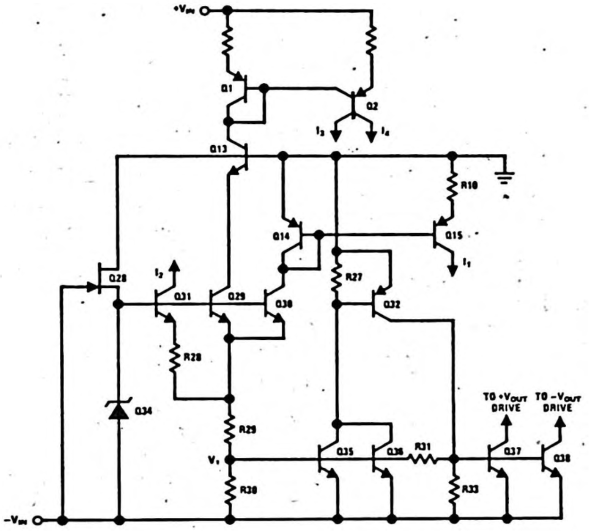

+V_IN
Q1
Q2
I3
I4
Q13
R10
Q14
Q15
I1
Q28
I2
Q31
Q29
Q30
R27
Q32
R28
Q34
R29
V1
R30
Q35
Q36
R31
R33
TO +V_OUT DRIVE
TO −V_OUT DRIVE
Q37
Q38
−V_IN

FIGURE 4. Start-up, Biasing and Thermal Shutdown Circuitry

drop across R_{CL} is sufficient to turn ON transistor Q11, the output drive current is switched away from the output devices Q4 and Q5. This externally set current limit is particularly valuable when used with an external current boosting pass transistor where the current limit could be set to protect that transistor from excessive power dissipation.

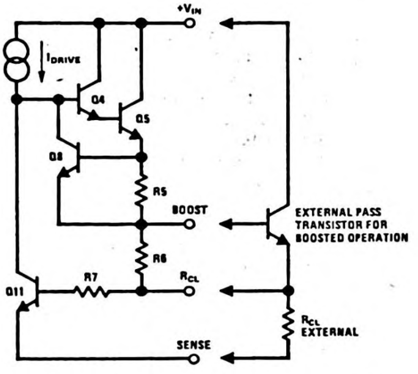

+V_IN
I_DRIVE
Q4
Q5
Q8
R5
BOOST
EXTERNAL PASS TRANSISTOR FOR BOOSTED OPERATION
R6
Q11
R7
R_CL
R_CL EXTERNAL
SENSE

FIGURE 5. Positive Regulator Current Limiting Circuitry

The constant voltage reference circuit is shown in Figure 6. Zener diode Z_1 has a positive temperature coefficient of known value. V_{BE} of Q18 (negative temperature coefficient) is multiplied by the ratio of R18 and R19 and added to the positive TC of Z_1 to produce a near zero TC voltage reference. Current source I_2 is used only during start-up.

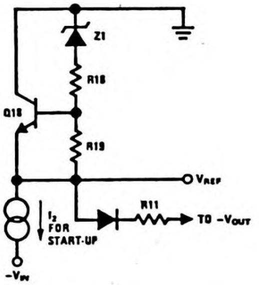
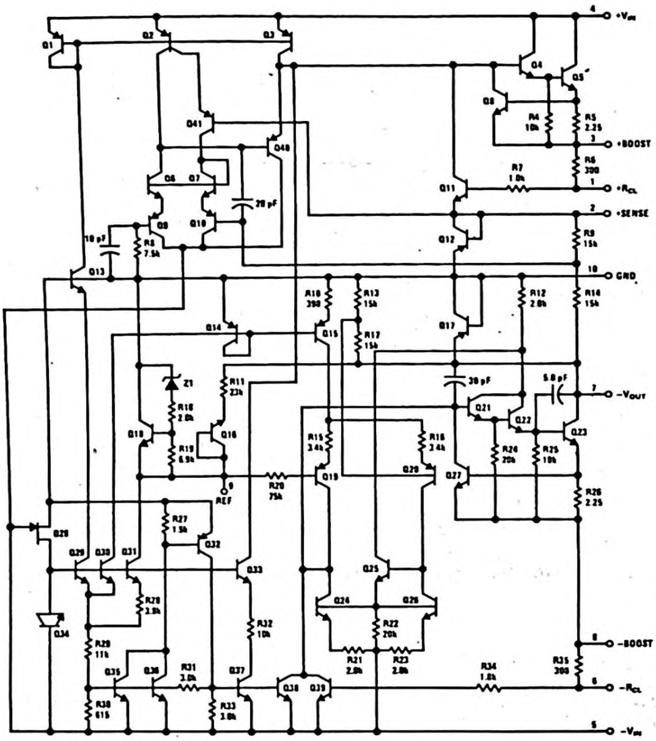

Z1
R18
Q18
R19
V_REF
I2 FOR START-UP
R11
TO −V_OUT
−V_IN

FIGURE 6. Voltage Reference Circuitry

Figure 7 shows the complete schematic of the LM125, LM126, LM127 family of dual regulators. Diodes Q12 and Q17 protect the output transistors, plus any external pass devices used, from breakdown in the event the positive and negative regulated outputs become shorted. Transistors Q6 and Q7 offer full differential voltage gain with the convenience of single ended output. Transistors Q13 and Q33 insure that operation with ±30V input is possible. Q24 and Q26 in the negative regulator amplifier provide single ended output from a differential input with no loss in gain.



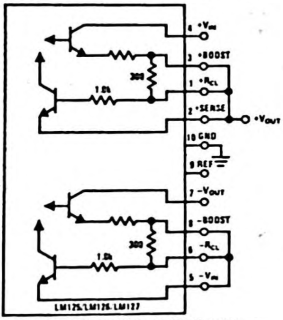
4 +VIN
3 +BOOST
1 +RCL
2 +SENSE
10 GND
7 −VOUT
8 −BOOST
6 −RCL
5 −VIN
9 REF
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Z1
R4 10k
R5 2.25
R6 300
R7 1.0k
R8 7.5k
R9 15k
R10 390
R11 23k
R12 2.0k
R13 15k
R14 15k
R15 3.4k
R16 3.4k
R17 15k
R18 2.0k
R19 6.9k
R20 75k
R21 2.8k
R22 20k
R23 2.8k
R24 20k
R25 10k
R26 2.25
R27 1.5k
R28 3.9k
R29 11k
R30 615
R31 3.0k
R32 10k
R33 3.0k
R34 1.0k
R35 300
20 pF
10 pF
30 pF
5.0 pF

NOTE: PIN NUMBERS APPLY TO METAL CAN PACKAGE ONLY.

FIGURE 7. LM125/LM126/LM127

APPLICATIONS

The basic dual regulator is shown connected in Figure 8. The only connections required other than plus and minus inputs, outputs, and ground are to complete the output current paths from $+R_{CL}$ to $+V_{OUT}$ and from $-R_{CL}$ to $-V_{IN}$. These may be a direct shorts if the internal preset current limit is desired, or resistors may be used to set the maximum current at some level less than the internal current limit. The internal 300Ω resistors from pins 3 to 1 and pins 8 to 6 should be shorted as shown when no external pass transistors are used. To improve line ripple rejection and transient response, filter capacitors may be added to the inputs, outputs, or both, depending on the unregulated input available. If a very low noise output voltage is desired, a capacitor may be connected from the reference voltage pin to ground. Thus shunting noise generated by the reference zener. Figure 9 shows the internal current limiting characteristics for the basic regulator circuit of Figure 8.



4 +VIN
3 +BOOST
1 +RCL
2 +SENSE
+VOUT
10 GND
9 REF
7 −VOUT
8 −BOOST
6 −RCL
5 −VIN
300
1.0k
300
1.0k
LM125/LM126/LM127

NOTE: PIN NUMBERS FOR METAL CAN PACKAGE ONLY.

FIGURE 8. Basic Dual Regulator

HIGH CURRENT REGULATOR

For applications requiring more supply current than can be delivered by the basic regulator, an external NPN pass transistor may be added to each regulator. This will increase the maximum output current by a factor of the external transistor beta. The circuit for current boosted operation is shown in Figure 10.

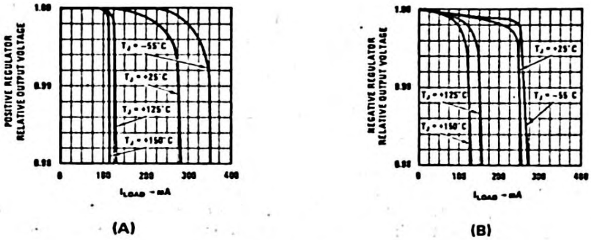


FIGURE 9. Internal Current Limiting Characteristics

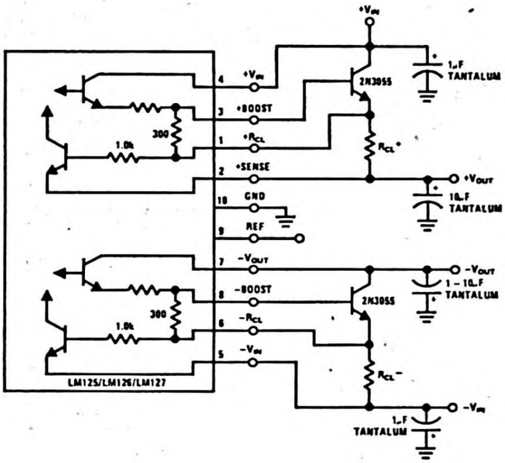

$+V_{IN}$
4
$+V_{IN}$
3
+BOOST
1
$+R_{CL}$
2
+SENSE
10
GND
9
REF
7
$-V_{OUT}$
8
–BOOST
6
$-R_{CL}$
5
$-V_{IN}$
300
1.0k
300
1.0k
LM125/LM126/LM127
2N3055
R_{CL}^+
$1\mu F$ TANTALUM
$+V_{OUT}$
$10\mu F$ TANTALUM
$-V_{OUT}$
$1-10\mu F$ TANTALUM
2N3055
R_{CL}^-
$-V_{IN}$
$1\mu F$ TANTALUM

FIGURE 10. Boosted High Current Regulator

In the boosted mode, current limiting is often a necessary requirement to insure that the external pass device is not overheated or destroyed. Experience shows this to be the usual cause of IC regulator failure. If the regulator output is grounded the pass device may fail and short, destroying the regulator. To limit the maximum output current, a series resistor (R_{CL} in Figure 10) is used to sense load current. The regulator will current limit when the voltage drop across R_{CL} equals the current limit sense voltage found in Figure 11. Figure 12 shows the external current limiting characteristics unboosted and Figure 13 shows the external current limiting characteristics in the boosted mode.

To ensure circuit stability at high currents in this configuration, it may be necessary to bypass each input with low inductance, tantalum capacitors to prevent forming resonant circuits with long input leads. A $C \geq 1\mu F$ is recommended. The same problem can also occur at the regulator output where a $C \geq 10\mu F$ tantalum will ensure stability and increase ripple rejection.

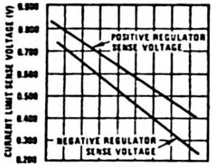
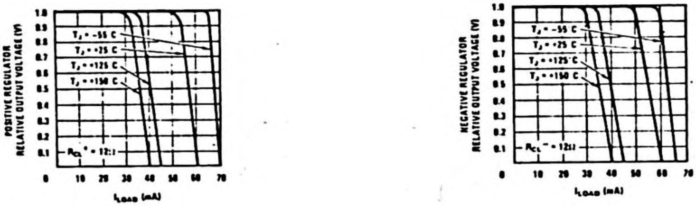


FIGURE 11. Current Limit Sense Voltage for a 0.1% Change in Regulated Output Voltage

The 2N3055 pass device is low in cost and maintains a reasonably high beta at collector currents up to several amps. The devices 2N3055 may be of either planar or alloy junction construction. The planar devices, have a high f_T providing more stable operation due to low phase shift. The alloy devices, with f_T typically less than 1.0 MHz, may require additional compensation to guarantee stability. The simplest of compensation for the slower devices is to use output filter capacitor values greater than 50µF (tantalum). An alternative is to use an RC filter to create a leading phase response to cancel some of the phase lag of the devices. The stability problem with slower pass transistors, if it occurs at all, is usually seen only on the negative regulator. This is because the positive regulator output stage is a conventional Darlington while the negative output stage contains three devices in a modified triple Darlington connection giving slightly more internal phase shift. Additional compensation may be added to the negative regulator by connecting a small capacitor in the 100 pF range from the negative boost terminal to the internal reference. Since the positive regulator uses the negative regulator output for a reference, this also offers some additional indirect compensation to the positive regulator.

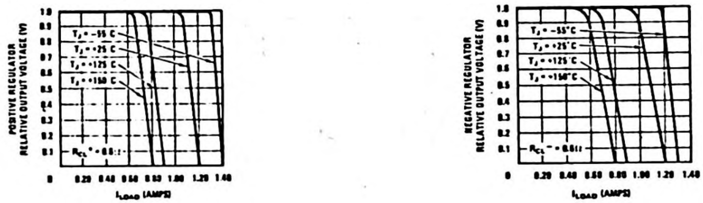
7 AMP REGULATOR

In Figure 14 the single external pass transistor has been replaced by a conventional Darlington



(A) (B)

FIGURE 12. External Current Limiting Characteristics- Unboosted



(A) (B)

FIGURE 13. External Current Limiting Characteristics- Boosted

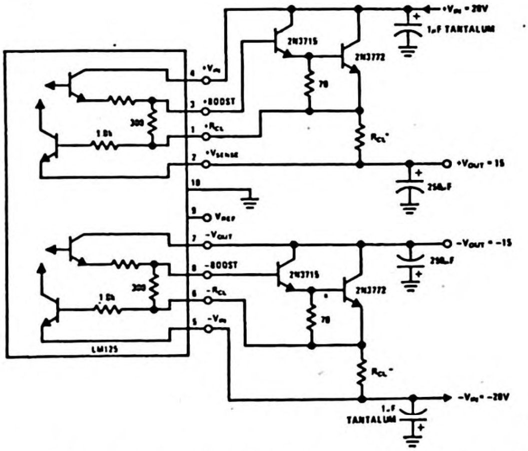

+V_IN = 20V
1µF TANTALUM
2N3715
2N3772
70
4 +V_IN
3 +BOOST
1 +R_CL
2 +V_SENSE
10
9 V_REF
7 −V_OUT
8 −BOOST
6 −R_CL
5 −V_IN
300
1.8k
R_CL+
+V_OUT = 15
25µF
−V_OUT = −15
25µF
R_CL−
−V_IN = −20V
1µF TANTALUM
LM125

FIGURE 14. High Current Regulator Using a Darlington Pair for Pass Elements

using a 2N3715 and a 2N3772. With this configuration the output current can reach values to 10A with very good stability. The external Darlington stage increases the minimum input-output voltage differential to 4.5V. When current limit protection resistor is used, as in Figure 14, the maximum output current is limited by power dissipation of the 2N3772 (150W at 25°C). During normal operation this is $(V_{IN} - V_{OUT})\ I_{OUT}$ (W), but it increases to $V_{IN}\ I_{SC}$ (W) under short circuit conditions. The short circuit output current is then:

$$I_{SC} = \frac{P_{MAX}\ (T_C = 25^{\circ}C)}{V_{IN}}$$

$$= \frac{150W}{20V\ (min)} = 7.5A \text{ max.}$$

I_L could be increased to 10A or more only if $I_{SC} < I_L$. A foldback current limit circuit will accomplish this. The typical load regulation is 40 mV from no load to a full load. (T_j = 25°C, pulsed load with 20 ms t_{ON} and 250 ms t_{OFF}.)

FOLDBACK CURRENT LIMITING

In many regulator applications, the normal operation power dissipation in the pass device can easily be multiplied by a factor of ten or more when the output is shorted. This may destroy the pass device, and possibly the regulator, unless the heat sink is oversized to handle this fault condition. A foldback current limiting circuit reduces short circuit output current to a fraction of the full load output current thus avoiding the need for larger heat sink. Figure 15 shows a foldback current limiting circuit on both positive and negative regulators.

The foldback current limiting, a fraction of the output voltage must be used to oppose the voltage across the current limit sense resistor. Current limiting does not occur until the voltage across the sense resistor is higher than this opposing voltage by the amount shown in Figure 11. When the output is grounded, the opposing voltage is no longer present so current limiting occurs at a lower level. This is accomplished in Figure 15 by using a programmable current source to give a constant voltage drop across R5 for the negative regulator, and by a simple resistor divider for the positive regulator. The reason for the difference between the two is that the negative regulator current limiting circuit is located between the output pass transistor and the unregulated input while the positive regulator current limiter is between the output pass transistor and the regulated output.

The operation of the positive foldback circuit is similar to that described in NSC application note AN-23. A voltage divider R1 and R2 from V_E to ground creates a fixed voltage drop across R1 opposite in polarity to the drop across R_{CL}^+. When the load current increases to the point where the drop across R_{CL}^+ is equal to the drop across R1 plus the current limit sense voltage given in Figure 11, the positive regulator will begin to current limit. As the positive output begins to drop, the voltage across R1 will also decrease so that it now requires less load current to produce the current limit sense voltage. With

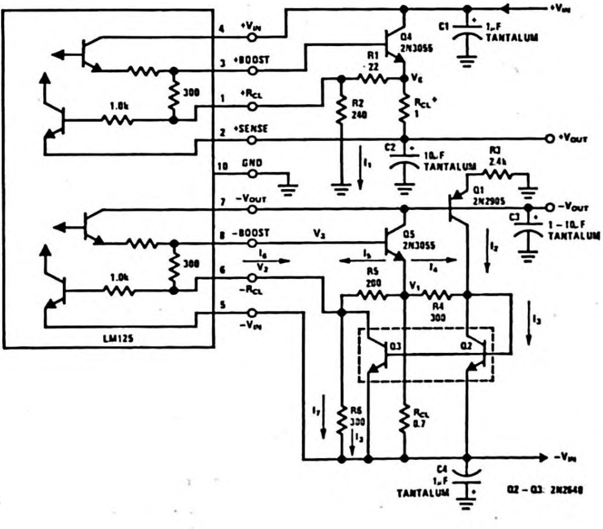


FIGURE 15. Foldback Current Limiting Circuit

the regulator output fully shorted to ground ($+V_{OUT} = 0$) the current limit will be set by the value of $+R_{CL}$ alone.

If $\frac{I_{FB}}{I_{SC}} \leq 5$

then the following equations can be used for calculating the positive regulator foldback current limiting resistors.

$$R_{CL}^+ = \frac{V_{SENSE}}{I_{SC}} \tag{1}$$

where V_{SENSE} is from Figure 11.

At the maximum load current foldback point:

$$V_{RCL}^+ = I_{FB}\, R_{CL}^+ \tag{2}$$

$$V_{R1} = V_{RCL}^+ - V_{SENSE} \tag{3}$$

$$V_{R1} = I_{FB}\, R_{CL}^+ - V_{SENSE} \tag{4}$$

Then

$$R1 = \frac{V_{R1}}{I_1} \tag{5}$$

and

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} \tag{6}$$

The only point of caution is to ensure that the total current (I_1) through R2 is much greater than the current contribution from the internal 300Ω resistor. This can be checked by:

$$\frac{I_{FB}\, R_{CL}^+}{300} \ll I_1 \tag{7}$$

Note: The current from the internal 300Ω resistor is $V_{3\text{-}1}/300\Omega$, but $V_{3\text{-}1} = V_{BE} + V_{RCL} - V_{SENSE}^+$ assuming $V_{BE} \approx V_{SENSE}^+$ at the foldback point, $V_{3\text{-}1} \approx V_{RCL}^+ = I_{FB}\, R_{CL}^+$.

Design example: 2 amp regulator LM125 positive foldback current limiting (see Figure 15).

Given:

$I_{FOLDBACK} = 2.0A$

$I_{SHORT\text{-}CIRCUIT} = 500\ mA$

V_{SENSE} (See Figure 11)

$+V_{IN} = 25V$

$+V_{OUT} = 15V$

$\beta_{PASS\ DEVICE} = 70$

$\theta_{JA} = 150°C/W$

$T_A = 50°C$

With a beta of 70 in the pass device and a maximum output current of 2.0A the regulator must deliver:

$$\frac{2A}{\beta} = \frac{2A}{70} = 29\ mA$$

The LM125 power dissipation will be calculated ignoring any negative output current for this example.

$$\begin{aligned} P_{LM125} &= (V_{IN} - V_{OUT})\, I_{OUT} \\ &= (25 - 15)\ 29\ mA \\ &= 290\ mW \end{aligned}$$

$$T_{RISE} \ @\ \theta_{JA} = 150°C/W = 150°C \times 0.29 = 44°C$$

$$T_J = T_A + T_{RISE} = 50°C + 44°C = 94°C$$

From Figure 11:

$$V_{SENSE} \ @\ (T_J = 94°C) = 520\ mW$$

From equation (1)

$$R_{CL}^+ = \frac{V_{SENSE}}{I_{SC}} = \frac{520\ mV}{500\ mA} \cong 1\Omega$$

From equation (2)

$$V_{RCL}^+ = I_{FB}\, R_{CL}^+ = 2A \cdot 1\Omega = 2V$$

From equation (3)

$$V_{R1} = V_{RCL}^+ - V_{SENSE}$$

$$V_{R1} = 2V - 520\ mV = 1.480V$$

A value for I_1 can now be found from equation (7)

$$\frac{I_{FB}\, R_{CL}^+}{300} = \frac{2A \cdot 1\Omega}{300\Omega} = 6.6\ mA$$

So set $I_1 = 10 \times 6.6\ mA = 66\ mA$

From equations (5) and (6)

$$R1 = \frac{V_{R1}}{I_1} = \frac{1.480V}{66\ mA} \cong 22\Omega$$

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} = \frac{15 + 0.520}{66\ mA}$$

$$\cong 240\Omega$$

The foldback limiting characteristics are shown in Figure 16 for the values calculated above at various operating temperatures.

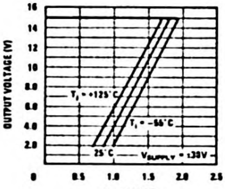


FIGURE 16. Positive Regulator Foldback Current Limiting Characteristics

The negative regulator foldback current limiting works essentially the same way as the positive side. Q1 forces a constant current, I_2, determined by $-V_{OUT}$ and R3, through Q2. Transistors Q2 and Q3 are matched so a current identical to I_3 will flow through Q3. With the output short-circuited ($-V_{OUT} = 0$), Q1 will be OFF, setting $I_2 = 0$. The load current will be limited when V_1 increases sufficiently due to load current to make V_2 higher than $-V_{IN}$ by the current limit sense voltage.

The short circuit current is:

$$I_{SC} \simeq \frac{V_{SENSE}}{R_{CL}^-} \qquad (8)$$

For calculating the maximum full load current with the output still in regulation, current I_2

$$I_2 = \frac{V_{OUT} - V_{BEQ1}}{R3} \qquad (9)$$

At the point of maximum load current, I_{FB}, where the regulator should start folding back:

$$V_1 = -V_{IN} + I_{FB} R_{CL}^- \qquad (10)$$

and

$$V_2 = -V_{IN} + V_{SENSE} \qquad (11)$$

The current through Q2 (and Q3) will have increased from I_2 by the amount of I_4 due to the voltage V_1 increasing above its no-load quiescent value. Since the voltage across Q2 is simply the diode drop of a base-emitter junction:

$$I_4 = \frac{[V_1 - (-V_{IN})] - V_{BE}}{R4}$$

Substituting in equation (10) gives:

$$I_4 = \frac{I_{FB} R_{CL}^- - V_{BE}}{R4}$$

$$= \frac{I_{FB} R_{CL}^- - V_{BE}}{300\Omega} \qquad (12)$$

The current through Q2 is now

$$I_3 = I_2 + I_4 \qquad (13)$$

and the current through Q3 is:

$$I_3 = I_5 + I_6 - I_7 \qquad (14)$$

The drop accross R5 is found from:

$$V_1 - V_2 = (-V_{IN} + I_{FB} R_{CL}^-) - [V_{SENSE} + (-V_{IN})];$$

simplifying,

$$V_1 - V_2 = I_{FB} R_{CL}^- - V_{SENSE} \qquad (15)$$

Since V_{SENSE} is the base to emitter voltage drop of the internal limiter transistor, the V_{SENSE} in equation (15) very nearly equals the V_{BE} in equation (12). Therefore the drop across R5 approximately equals the drop across R4. The current through R5, I_5, can now be determined as:

$$I_5 = \frac{I_{FB} R_{CL}^- - V_{SENSE}}{R5} \qquad (16)$$

Summing the currents through Q3 is now possible assuming the base-emitter drop of the 2N3055 pass device can be given by $V_{BE} \approx V_{SENSE}$:

$$I_6 = \frac{V_3 - V_2}{300} \qquad (17)$$

where $V_3 = V_1 + V_{BE} \approx V_1 + V_{SENSE}$

$$I_6 = \frac{V_1 + V_{SENSE} - V_2}{300}$$

Substituting in equation (15)

$$I_6 = \frac{I_{FB} R_{CL}^-}{300}$$

$$I_7 = \frac{V_2 - (-V_{IN})}{R6} = \frac{V_{SENSE}}{R6} \qquad (18)$$

Equating equation (13) with equation (14) and inserting resistor values shown in Figure 15,

$$I_2 + I_4 = I_5 + I_6 - I_7$$

$$I_2 + \frac{I_{FB}\,R_{CL}^- - V_{SENSE}}{300} = \qquad (19)$$

$$I_5 + \frac{I_{FB}\,R_{CL}^-}{300} - \frac{V_{SENSE}}{300}$$

Canceling, we find:

$$I_2 = I_5 \qquad (20)$$

This is the key to the negative foldback circuit. Current source Q1 forces current I_2 to flow through resistor R5. The voltage drop across R5 opposes the normal current limit sense voltage so that the regulator will not current limit until the drop across R_{CL}^- due to load current, equals the controlled drop across R5 plus V_{SENSE} (given in Figure 11). This can be written as:

$$I_{FB} = \frac{V_{SENSE} + I_2\,R5}{R_{CL}^-}$$

$$I_{FB} = \frac{V_{SENSE} + 200\,I_2}{R_{CL}^-} \qquad (21)$$

A design example is now offered:

Given:

$I_{FOLDBACK} = 2.5A$

$I_{SHORT\text{-}CIRCUIT} = 750\text{ mA}$

V_{SENSE} (See Figure 11)

$-V_{IN} = 25V$

$-V_{OUT} = -15V$

$\beta_{PASS\ DEVICE} = 90$

$\theta_{JA} = 150°C/W$

$T_A = 25°C$

The same calculations are used here to figure V_{SENSE} as with the positive regulator foldback example maximum regulator output current is calculated from:

$$I_{OUT} = \frac{2.5\text{ A}}{90} = 28\text{ mA}$$

$$\begin{aligned} P_{LM125} &= (V_{IN} - V_O)\,I_{OUT} \\ &= 10V \times 28\text{ mA} \\ &= 280\text{ mW} \end{aligned}$$

$$T_{RISE} = 150°C/W \times 0.28W = 42°C$$

$$T_J = T_A + T_{RISE} = 25°C + 42°C = 67°C$$

From Figure 11:

$$V_{SENSE} = 500\text{ mV}$$

From equation (8):

$$R_{CL}^- = \frac{500\text{ mV}}{750\text{ mA}} = 0.68\Omega$$

From equation (21):

$$I_2 = \frac{I_{FB}\,R_{CL}^- - V_{SENSE}}{200\Omega} = 6.0\text{ mA}$$

From equation (9):

$$R3 = \frac{V_{OUT} - V_{BEQ1}}{I_2}$$

$$R3 \simeq \frac{14.3}{6.0\text{ mA}} = 2.4k$$

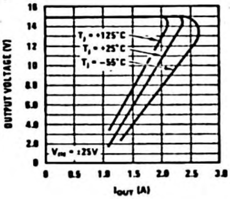


FIGURE 17. Negative Regulator Foldback Current Limiting Characteristics

Figure 16 and 17 show the measured foldback characteristics for the values derived in the design examples. The value of R5 is set low so that the magnitude of I_5 for foldback is greater than I_4 through I_6. This reduces the foldback point sensitivity to the TC of the internal 300Ω resistor and any mismatch in the TC of Q2, Q3 or the pass device.

R6 can be computed from equation (18):

$$R6 = \frac{V_{SENSE}^-}{I_7} = \frac{V_{SENSE}^-}{I_5 + I_6 - I_3}$$

combining (13) and (20).

$$R6 = \frac{V_{SENSE}^-}{I_6 - I_4} = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left(\frac{1}{300} - \frac{1}{R4}\right) + \frac{V_{BE}}{R4}} \quad (22)$$

Setting $V_{BE} \simeq V_{SENSE}$ and $R4 = 300$ to match the internal 300Ω (22) becomes:

$$R6 = R4$$

$$\text{Also setting } \frac{I_4}{I_5} = \frac{2}{3} \rightarrow R5 = 200$$

A 10 AMP REGULATOR

Figure 18 illustrates the complete schematic of a 10A regulator with foldback current limiting. The design approach is similar to that of the 2A regulator. However, in this design, the current contribution from the internal 300Ω resistor is greater due to the 2 V_{BE} drop across the Darlington pair. Expression (7) becomes:

$$\frac{I_{FB}\, R_{CL}^+ + V_{BE}}{300} << I_1 \; ; \quad (23)$$

and, for the negative regulator, expression (22) becomes:

$$R6 = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left[\frac{1}{300} - \frac{1}{R4}\right] + V_{BE}\left[\frac{1}{300} + \frac{1}{R4}\right]} \quad (24)$$

The disagreement between the theoretical and experimental values for the negative regulator is not alarming. In fact R_{CL} was based on equation (8), which is correct if for zero V_{OUT}, I_5 is zero as well. This implies:

$$V_{SENSE}\ (\text{at SC}) = \frac{V_{BEQ4} + V_{BEQ5}}{2}\ (\text{at SC})$$

which is a first order approximation.

Figure 19 illustrates the power dissipation in the external power transistor for both sides. Maximum power dissipation occurs between full load and short circuit so the heat sink for the 2N3772 must be designed accordingly, remembering that the 2N3772 must be derated according to 0.86W/°C above 25°C. This corresponds to a thermal resistance junction to case of 1.17°C/W.

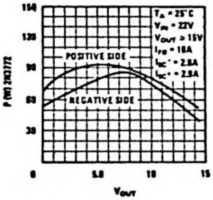
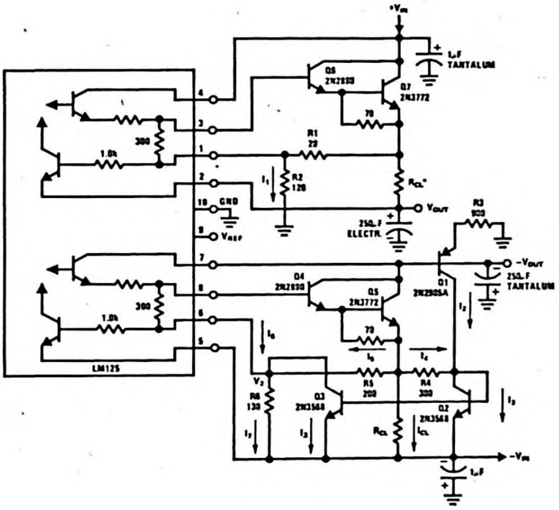


FIGURE 19. Power Dissipation in the External Pass Transistor (Q5, Q7)



+V_{IN}
1μF TANTALUM
Q6 2N2880
Q7 2N3772
70
R1 22
R2 120
I_1
R_{CL}^+
V_{OUT}
GND
V_{REF}
25μF ELECTR.
R3 900
300
1.0k
4
3
1
2
10
9
7
8
6
5
LM125
$-V_{OUT}$
25μF TANTALUM
Q4 2N2880
Q5 2N3772
Q1 2N2905A
I_2
I_6
I_5
I_4
R5 200
R4 300
V_2
R6 130
Q3 2N3568
Q2 2N3568
I_3
I_7
R_{CL}
I_{CL}
$-V_{IN}$
1μF

FIGURE 18. 10A Regulator with Foldback Current Limiting

Example

Positive Side	Theoretical Value	Experimental Results
$I_{FB} = 10$ A	$I_{125} = 13$ mA	$I_{FB} = 9.8$ A
$I_{SC} = 2.5$ A	$P_{LM125} = 150$ mW	$I_{SC} = 2.9$ A
$V_{IN} = 22V$	$R_{CL}{}^{+} = 0.26\Omega$	$R_{CL}{}^{+} = 0.26\Omega$
$V_{OUT} = 15V$	$R1 = 21\Omega$	R1: adjusted to 20Ω
$\beta = \beta 1\ \beta 2 = 15 \times 50 = 750$ min	$R2 = 130\Omega$	R2: adjusted to 120Ω
$T_A = 25°C$	$V_{SENSE}{}^{+} = 650$ mV	

Negative Side	Theoretical Value	Experimental Results
$I_{FB} = 10$ A	$R_{CL}{}^{-} = 0.22\Omega$	$I_{FB} = 10$ A
$I_{SC} = 2.5$ A	$R4 = 300\Omega$	$I_{SC} = 2.9$ A
$V_{IN} = 22V$	$R5 = 200\Omega$	R_{CL}: adjusted to 0.3Ω
$V_{OUT} = 15V$	$R6 = 150\Omega$	R6: adjusted to 130Ω
$\beta = 800$	$R3 = 1.6$ kΩ	R3: adjusted to 900Ω
$T_A = 25°$	$V_{SENSE}{}^{-} = 550$ mV	
$\frac{I_4}{I_5} = \frac{2}{3}$		

Note: For this example, in designing each side, the power dissipation of the opposite side has not been taken into the account.

POSITIVE CURRENT DEPENDENT SIMULTANEOUS CURRENT LIMITING

The LM125/LM126/LM126 uses the negative output as a reference for the positive regulator. As a consequence, whenever the negative output current limits, the positive output follows tracks to within 200 – 800 mV of ground. If, however, the positive regulator should current limit the negative output will remain in full regulation. This imbalance in output voltages could be a problem in some supply applications.

As a solution to this problem, a simultaneous limiting scheme, dependent on the positive regulator output current, is presented in Figure 20. The output current causes an I-R drop across R1 which brings transistor Q1 into conduction. As the positive load current increases I_1 increases until the voltage drop across R2 equals the negative current limit sense voltage. The negative regulator will then current limit, and positive side will closely follow the negative output down to a level of 700 – 800 mV. For $V_{OUT}{}^{+}$ to drop the final 700 – 800 mV with small output current change, $R_{CL}{}^{+}$ should be adjusted so that the positive current limit is slightly larger than the simultaneous limiting. Figure 21 illustrates the simultaneous current limiting of both sides.

The following design equations may be used:

$$R1\ I_{CL}{}^{+} = R3\ I_1 + V_{BEQ1} \qquad (25)$$

$$I_1 = \frac{V_{SENSE}{}^{-}}{R2} \qquad (26)$$

Combining (25) and (26),

$$I_{CL}{}^{+} = \frac{\frac{R3}{R2} V_{SENSE}{}^{-} + V_{BEQ1}}{R1} \qquad (27)$$

with

$$R_{CL}{}^{+} = \frac{V_{SENSE}{}^{+}}{1.1\ I_{CL}{}^{+}} \qquad (28)$$

The negative current limit (independent of $I_{CL}{}^{+}$) can be set at any desired level.

$$I_{CL}{}^{-} = \frac{V_{SENSE}{}^{-} + V_{DIODE}}{R_{CL}{}^{-}} \qquad (29)$$

Transistor Q2 turns off the negative pass transistor during simultaneous current limiting.

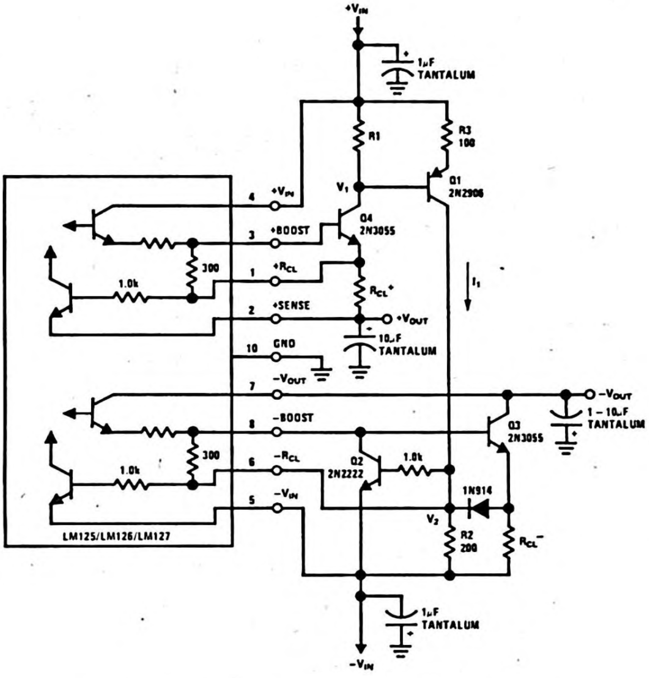

+V_IN
1µF TANTALUM
R1
R3 100
V_1
Q1 2N2906
Q4 2N3055
4 +V_IN
3 +BOOST
1 +R_CL
2 +SENSE
10 GND
7 -V_OUT
8 -BOOST
6 -R_CL
5 -V_IN
300
1.0k
R_CL+
+V_OUT
10µF TANTALUM
I_1
-V_OUT
1 - 10µF TANTALUM
Q3 2N3055
Q2 2N2222
1.0k
1N914
V_2
R2 200
R_CL-
LM125/LM126/LM127
1µF TANTALUM
-V_IN

FIGURE 20. Positive Current Dependent Simultaneous Current Limiting

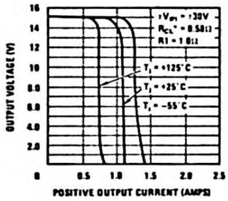


FIGURE 21. Positive Current Dependent Simultaneous Shutdown

ELECTRONIC SHUTDOWN

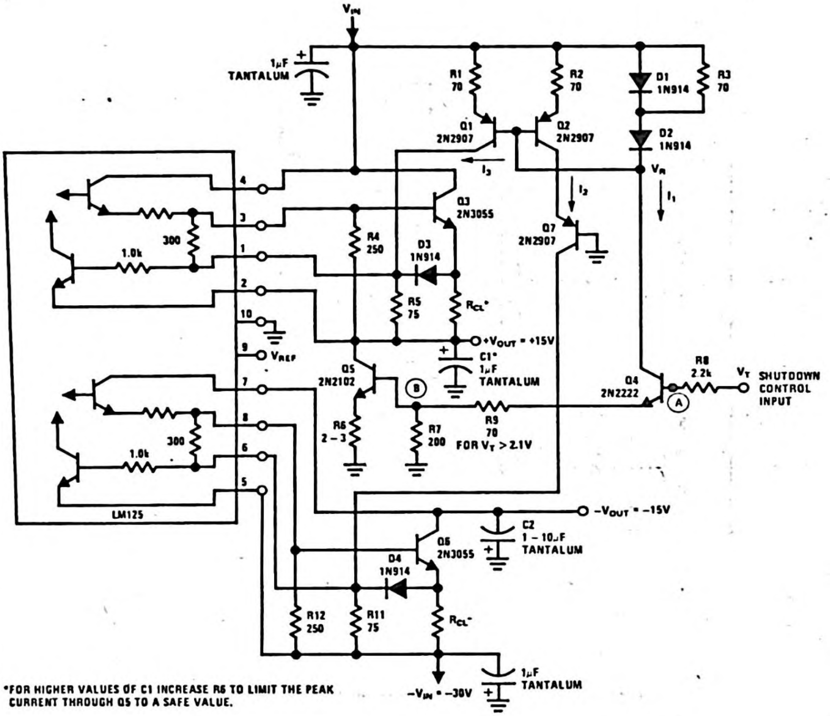
In some regulated supply applications it is desirable to shutdown the regulated outputs ($\pm V_O = 0$) without having to shutdown the unregulated inputs (which may be powering additional equipment). Various shutdown methods may be used. The simplest is to insert a relay, a saturated bipolar device, or some other type switch in series with either the regulator inputs or outputs. The switch must be able to open and close under maximum load current which, may be several amps.

As an alternate solution, the internal reference voltage of the regulator may be shorted to ground. This will force the positive and negative outputs to approximately +700 mV and +300 mV respectively. Both outputs are fully active so the full output current can still be supplied into a low impedance load. If this is unacceptable, another solution must be found.

The circuit in Figure 22 provides complete electronic shutdown of both regulators. The shutdown control signal is TTL compatible but by adjusting R8 and R9 the regulator may be shutdown at any desired level above 2 V_{BE}, calculated as follows:

$$V_T \simeq \left[\frac{R8}{R3\,\beta\,Q4} + \frac{R9}{R3}\right] V_{BE} + 2\,V_{BE} \qquad (30)$$

Positive and negative shutdown operations are similar. When a shutdown signal V_T is applied, Q4 draws current through R3 and D2 establishing a voltage V_R which starts the current sources Q1 and Q2. Assuming that Q1 and Q2 are matched, and making R1 = R2 = R3, the currents I_1, I_2, I_3 are equal and both sides of the regulator shutdown simultaneously.


V_IN
1µF TANTALUM
R1 70
R2 70
D1 1N914
R3 70
Q1 2N2907
Q2 2N2907
D2 1N914
I3
V_R
I2
I1
Q3 2N3055
Q7 2N2907
R4 250
D3 1N914
R5 75
R_CL*
+V_OUT = +15V
C1* 1µF TANTALUM
V_REF
Q5 2N2102
B
R6 2 – 3
R7 200
R9 70
FOR V_T > 2.1V
Q4 2N2222
A
R8 2.2k
V_T SHUTDOWN CONTROL INPUT
300
1.0k
LM125
4
3
1
2
10
9
7
8
6
5
–V_OUT = –15V
C2 1 – 10µF TANTALUM
Q6 2N3055
D4 1N914
R12 250
R11 75
R_CL–
1µF TANTALUM
–V_IN = –30V

*FOR HIGHER VALUES OF C1 INCREASE R6 TO LIMIT THE PEAK CURRENT THROUGH Q5 TO A SAFE VALUE.

FIGURE 22. Electronic Shutdown for the Boosted Regulator

The current I_3 creates a drop across R5, which equals or exceeds the limit sense voltage of the positive regulator, causing it to shutdown. Since I_3 has no path to ground except through the load, a fixed load is provided by Q5, which is turned on by the variable current source Q4. C1 also discharges through Q5 and current limiting resistor R6. Resistor R4 prevents Q3 turn on during shutdown, which could otherwise occur due to the drop across R5 plus the internal 300Ω resistor. Diode D3 prevents I_3 from being shunted through R_{CL}.

C2 discharges through the load. Q7 shares the total supply voltage with Q2, thus limiting power dissipation of Q2. Another power dissipation problem may occur when the design is done for $V_T = 2.0V$ for example, and V_T is increased above the preset threshold value. I_1 is increased and Q4 has to dissipate $(V_{IN} - 3\ V_{BE} - V_T)\ I_1$ (W). The simplest solution is to increase R8. If this is insufficient, a set of diodes may be added between nodes A and B to clamp. I_1 to a reasonable value. This is illustrated in Figure 23:

$$I_1 = \frac{V_{R9}}{R9} \simeq \frac{V_T - V_{BE} - \left[V_T - 2\ V_{BE}\right]}{R9}$$

$$= \frac{V_{BE}}{R9}$$

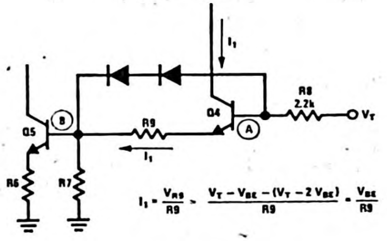

I1
Q5
B
Q4
A
R8 2.2k
V_T
R9
I1
R6
R7
I1 = V_R9/R9 ≈ (V_T − V_BE − (V_T − 2 V_BE))/R9 = V_BE/R9

FIGURE 23.

So I_1 is made independent of V_T and by setting a minimum value of 10 mA (R9 = 70Ω). The regulator will shutdown at any desired level above 3 V_{BE}, without overheating transistor Q4. Also using

AN-87 Comparing the High Speed Comparators

Comparing the High Speed Comparators

National Semiconductor
Application Note 87
Interface
Development Group
June 1973

INTRODUCTION

Several integrated circuit voltage comparators exist which were designed with high speed and complementary TTL outputs as the main objectives. The more common applications for these devices are high speed analog to digital (A to D) converters, tape and disk-file read channels, fast zero-crossing detectors, and high speed differential line receivers. This note compares the National Semiconductor devices to similar devices from other manufacturers.

The product philosophy at National was to create pin-for-pin replacement circuits that could be considered as second-sources to the other comparators, while simultaneously containing the improvements necessary to make a more optimum device for the intended usage. Optimized parameters include speed, input accuracy and impedance, supply voltage range, fanout, and reliability. The LM160/LM260/LM360 are replacement devices for the µA760, while the LM161/LM261/LM361 replace the SE/NE529. Tables I and II compare the critical parameters of the National commercial range devices to their respective counterparts.

SPEED

Throughout the universe the subject of speed must be approached with caution; the same holds true here. Speed (propagation delay time) is a function

TABLE I. LM360/µA760C Comparison $0^\circ \leq T_A \leq +70^\circ C$, $V^+ = +5.0V$, $V^- = -5.0V$

PARAMETER	LM360	µA760C	UNITS
Input Offset Voltage	5.0	6.0	mV max
Input Offset Current	3.0	7.5	µA max
Input Bias Current	20	60	µA max
Input Capacitance	4.0	8.0	pF typ
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±4.0	±4.0	V typ
Gain	3.0	3.0	V/mV typ 25°
Fanout	4.0	2.0	74 Series TTL Loads
Propagation Delays:			
(1) 30 mV$_{P\text{-}P}$ 10 MHz Sinewave in	25	30	ns max 25°
(2) 2.0 V$_{P\text{-}P}$ 10 MHz Sinewave in	20	25	ns max 25°
(3) 100 mV Step + 5.0 mV Overdrive	14	22	ns typ 25°

TABLE II. LM261/NE529 Comparison $0^\circ \leq T_A \leq +70^\circ C$, $V^+ = +10V$, $V^- = -10V$, $V_{CC} = +5.0V$

PARAMETER	LM261	NE529	UNITS
Input Offset Voltage	3.0	10	mV max
Input Offset Current	3.0	15	µA max
Input Bias Current	20	50	µA max
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±6.0	±6.0	V typ
Gain	3.0	4.0	V/mV typ 25°
Fanout	4.0	6.0	74 Series TTL Loads
Propagation Delay – 50 mV Overdrive	20	22	ns max 25°

of the measurement technique. The earlier "standard" of using a 100 mV input step with 5.0 mV overdrive has given way to seemingly endless variations. To be meaningful, speed comparisons must be made with identical conditions. It is for this reason that the speed conditions specified for the National parts are the same as those of the parts replaced.

Probably the most impressive speed characteristic of the six National parts is the fact that propagation delay is essentially independent of input overdrive (Figure 1); a highly desirable characteristic in A to D applications. Their delay typically varies only 3 ns for overdrive variations of 5.0 mV to 500 mV, whereas the other parts have a corresponding delay variation of two to one. As can be seen in Tables I and II, the National parts have an improved maximum delay specification. Further, the 20 ns maximum delay is meaningful since it is specified with a representative load: a 2.0 kΩ resistor to +5.0V and 15 pF total load capacitance. Figure 2 shows typical delay variation with temperature.

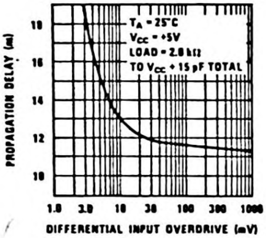


FIGURE 1. Delay vs Overdrive

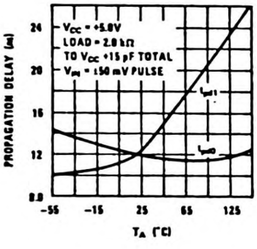


FIGURE 2. Delay vs Temperature

INPUT PARAMETERS

The A to D, level detector, and line receiver applications of these devices require good input accuracy and impedance. In all these cases the differential input voltage is relatively large, resulting in a complete switch of input bias current as the input signal traverses the reference voltage level. This effect can give rise to reduced gain and threshold inaccuracy, dependent on input source impedances and comparator input bias currents. Tables I and II show that the National parts have a substantially lower maximum bias current to ease this problem. This was done without resorting to Darlington input stages whose price is higher offset voltages and longer delay times. The lower bias currents also raise input resistance in the threshold region. Lower input capacitance and higher input resistance result in higher input impedance at high frequencies.

Even with low source impedances, input accuracy is still dependent on offset voltage. Since none of the devices under discussion has internal offset null capability, ultimate accuracy was improved by designing and specifying lower maximum offset voltage. Refer to Figure 3 for typical offset voltage drift with temperature.

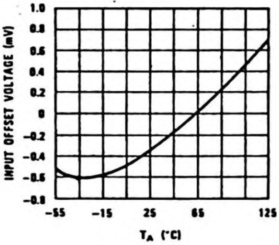


FIGURE 3. Offset Temperature Coefficient

OTHER PERFORMANCE AREAS

In the case of the LM160/LM260/LM360, fanout was doubled over the previous device. For the LM161/LM261/LM361, operating supply voltage range was extended to ±15V op amp supplies which are often readily available where such a comparator is used. Figure 4 reveals the common mode range of the latter device.

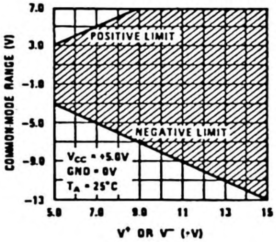


FIGURE 4. LM161 Common Mode Range

The performance improvements previously mentioned were a result of circuit design (Figures 5 and 6) and device processing. Schottky clamping, which can give rise to reliability problems, was not used. Gold doping, which results in processing dependent speeds and low transistor beta, was not used. Instead a non-gold-doped process with high breakdown voltage, high beta, and high f_T (≈ 1.5 GHz) was selected which produced remarkably consistent performance independent of normal process variation. The higher breakdown voltage allows the LM161/LM261/LM361 to operate on ±15V supplies and results in lower transistor capacitance; higher beta provides lower input bias currents; and higher f_T helps reduce propagation time.

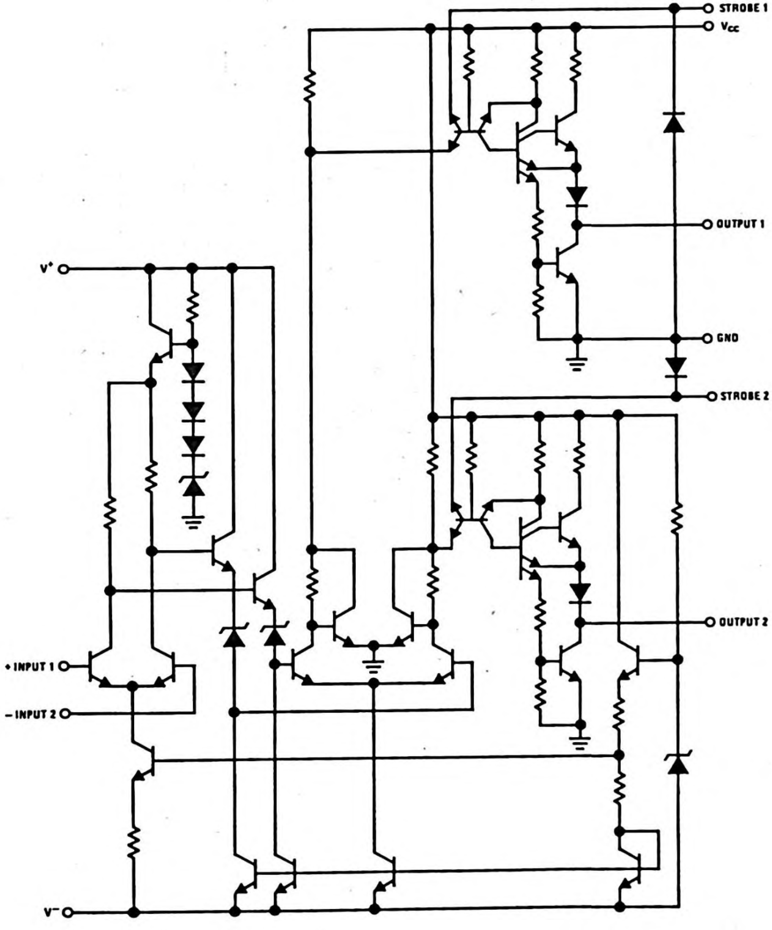


FIGURE 5. LM161 Schematic Diagram

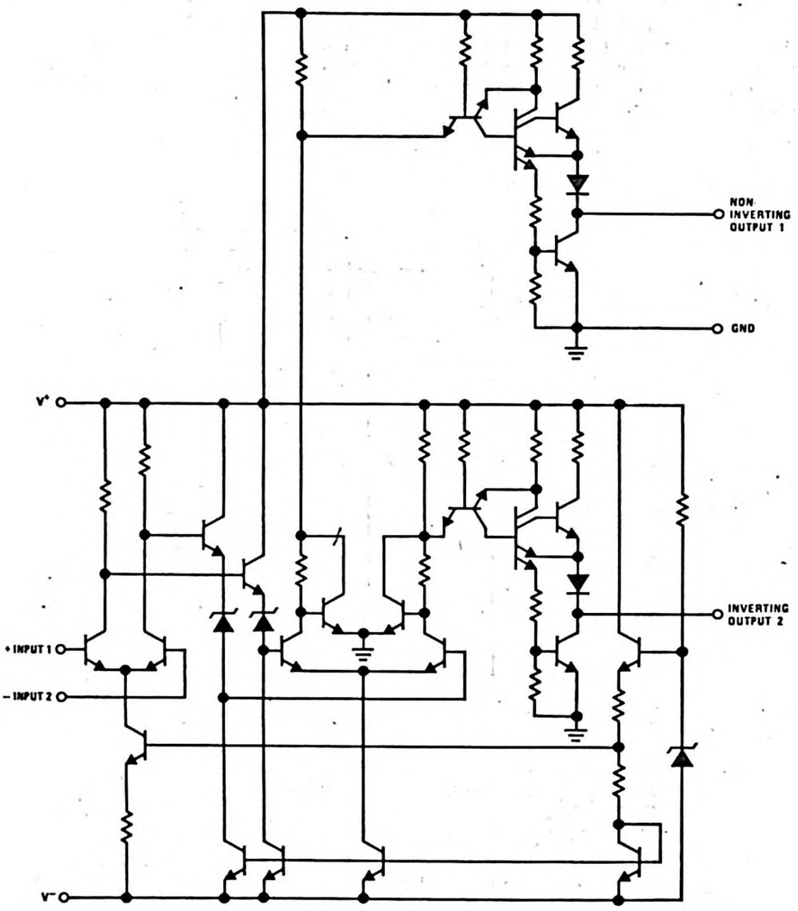
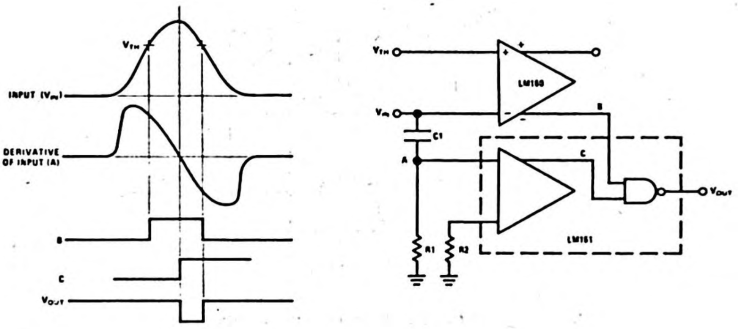


FIGURE 6. LM160 Schematic Diagram

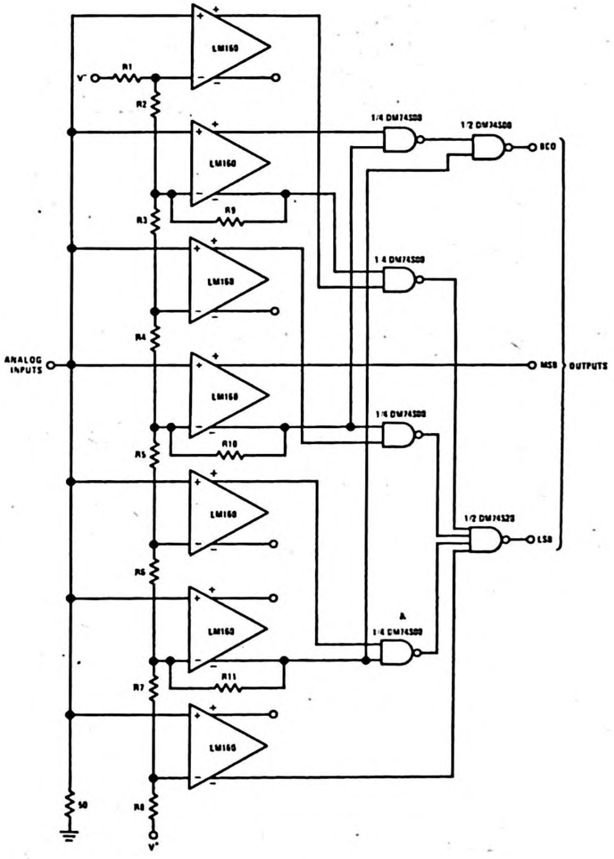
APPLICATIONS

Typical applications have been mentioned previously. The LM160 and LM161 may be combined as in Figure 7 to create a fast, accurate peak detector for use in tape and disk-file read channels. A 3-bit A to D converter with 21 ns typical conversion time is shown in Figure 8. Although primarily intended for interfacing to TTL logic, direct connection may be made to ECL logic from the LM161 by the technique shown in Figure 9. When used this way the common mode range is shifted from that of the TTL configuration. Finally level detectors or line receivers may be implemented with hysteresis in the transfer characteristic as seen in Figure 10.



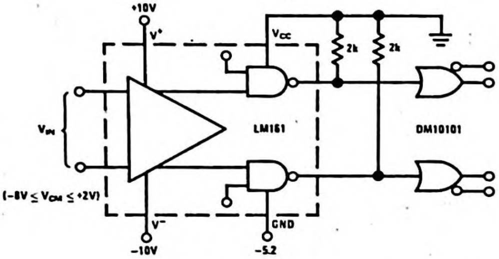
V_{TH}
INPUT (V_{IN})
DERIVATIVE OF INPUT (A)
B
C
V_{OUT}
V_{TH}
LM160
V_{IN}
C1
A
B
C
V_{OUT}
LM161
R1
R2

FIGURE 7. Peak Detector



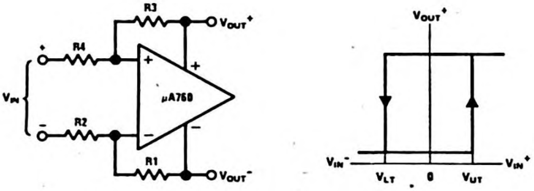
LM160
V^-
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
1/4 DM74S00
1/2 DM74S00
BCO
ANALOG INPUTS
MSB
OUTPUTS
1/2 DM74S20
LSB
A
50
V^+

FIGURE 8. High Speed 3-bit A to D Converter



+10V
V+
VCC
2k
2k
LM161
DM10101
VIN
(−8V ≤ VCM ≤ +2V)
V−
GND
−10V
−5.2

FIGURE 9. Direct Interfacing to ECL



R3
VOUT+
+
R4
VIN
μA760
−
R2
R1
VOUT−
VOUT+
VIN−
VIN+
VLT
0
VUT

$$V_{UT} = V_{OH}\left(\frac{R2}{R1}\right) - V_{OL}\left(\frac{R4}{R3}\right)$$

$$V_{LT} = V_{OL}\left(\frac{R2}{R1}\right) - V_{OH}\left(\frac{R4}{R3}\right)$$

FIGURE 10. Level Detector with Hysteresis

CMOS Linear Applications

National Semiconductor
Application Note 88
Gene Taatjes
July 1973

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

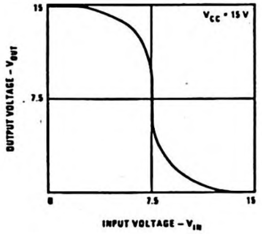


FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

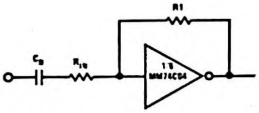


FIGURE 2. A 74CMOS Inverter Biased for Linear Mode Operation.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

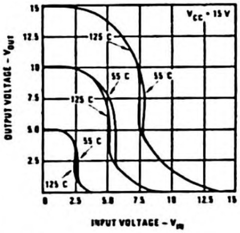


FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

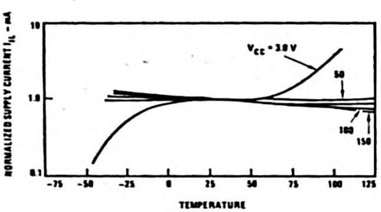


FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

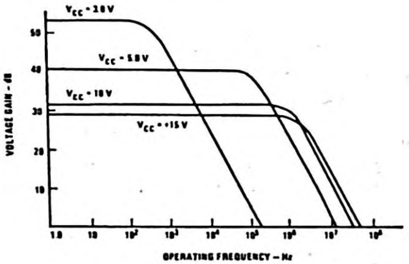


FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.

APPLICATIONS

Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

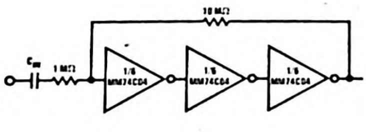


FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.

Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

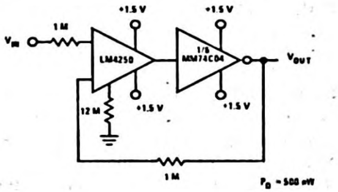


FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

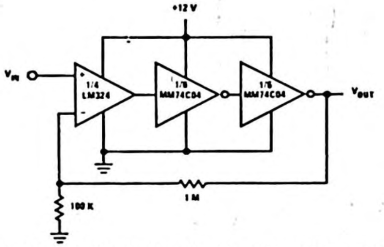


FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA from the V_{CC} supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

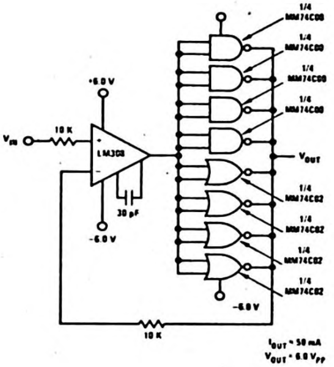

1/4 MM74C00
1/4 MM74C00
1/4 MM74C00
1/4 MM74C00
+6.0 V
10 K
V_{IN}
LM308
30 pF
-6.0 V
V_{OUT}
1/4 MM74C02
1/4 MM74C02
1/4 MM74C02
1/4 MM74C02
-6.0 V
10 K
I_{OUT} = 50 mA
V_{OUT} = 6.0 V_{PP}

FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive.

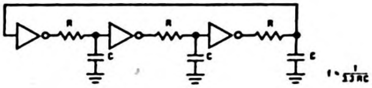
Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

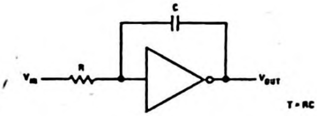
Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

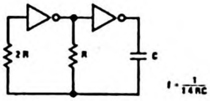
Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.


R
R
R
C
C
C
f ≈ 1/5.3 RC

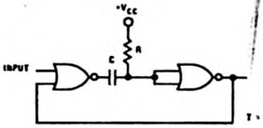
Phase Shift
Oscillator Using MM74C04


C
R
V_{IN}
V_{OUT}
T = RC

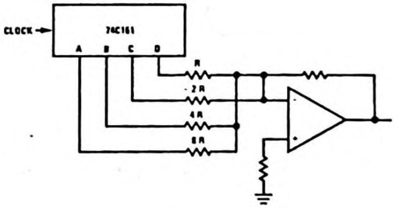
Integrator Using
Any Inverting CMOS Gate


2 R
R
C
f ≈ 1/1.4 RC

Square Wave Oscillator


+V_{CC}
R
C
INPUT
T ≈ 1.4 RC

One Shot


CLOCK
74C161
A
B
C
D
R
2 R
4 R
8 R

Staircase Generator

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.

Versatile Timer Operates from Microseconds to Hours

National Semiconductor
Application Note 97
Carl Nelson
December 1973

INTRODUCTION

Timing functions, until recently, have been somewhat neglected by integrated circuit manufacturers. The primary reason was the extremely wide range of input and output signals currently incorporated in discrete designs. In addition, power supply voltages varied over a ten to one range and timing periods were as short as microseconds and as long as hours.

The LM122 timer has been designed to operate over a very wide range of input/output signal levels, supply voltages, and timing periods. It will replace most discrete designs with improved performance and reliability. This new timer overcomes many of the problems incurred in discrete or early IC designs.

First, it locks out trigger signals during the timing period to guarantee a precise output regardless of trigger level — while maintaining the ability to be retriggered almost immediately following the end of the timing pulse. (Duty cycles up to 99.9% can be achieved). Secondly, the timing period is free from jitter caused by supply fluctuations because the timing components are driven from an internal regulated source. Supply voltage for the timer can vary from 4.5V to 40V even during the timing period! An additional feature is the ±40V excursion allowed on the trigger input and the 40V/50 mA drive capability of the output transistor. These two specifications allow the LM122 to interface directly to present designs without level shift or power boosting problems. Finally, the LM122 will generate stable timing periods from several microseconds to hours—a useful range of eight decades. Worst case guarantees on comparator bias current and threshold level allow the user to easily select timing components for maximum accuracy.

CIRCUIT DESCRIPTION

The LM122 circuitry can be divided into five separate sections: output stage, bias network, voltage regulator, comparator, and logic. These sections are grouped on the schematic in Figure 1 to simplify understanding of the timer.

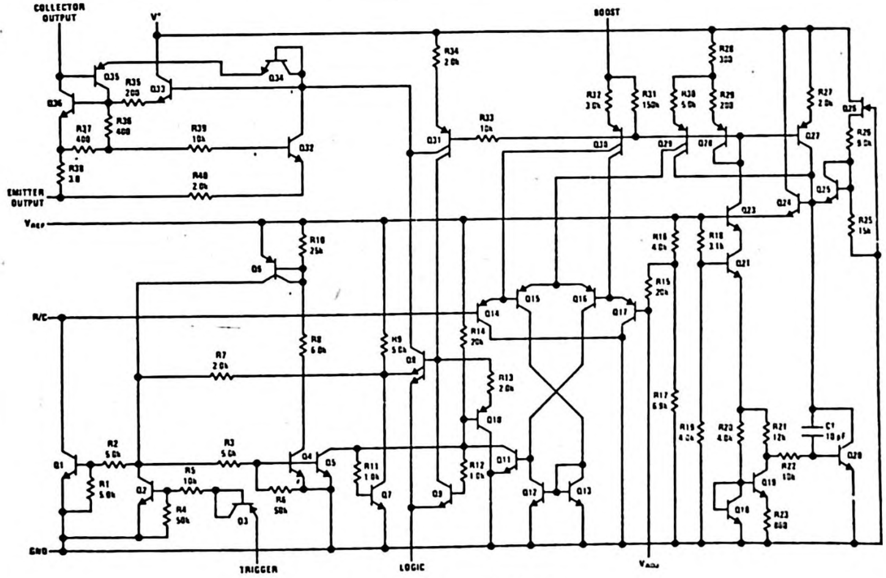

COLLECTOR OUTPUT
V+
BOOST
EMITTER OUTPUT
VREF
R/C
GND
TRIGGER
LOGIC
VADJ
Q35
R35 200
Q33
Q34
Q36
R37 400
R36 400
R39 10k
Q32
R38 3.8
R40 2.0k
R34 2.0k
R33 10k
Q31
R32 3.0k
R31 150k
R30 5.0k
R28 300
R29 200
Q30
Q29
Q28
R27 2.0k
Q26
Q27
R25 5.0k
Q25
Q24
Q23
R26 15k
R10 25k
Q6
R16 4.0k
R18 3.1k
Q21
R15 20k
Q15
Q16
Q14
Q17
R8 6.0k
R9 5.0k
Q8
R14 20k
R7 2.0k
R13 2.0k
Q10
R17 6.9k
R19 4.0k
R20 4.0k
R21 12k
C1 10 pF
R22 10k
Q20
R2 5.0k
R3 5.0k
Q1
Q4
Q5
R11 1.0k
R12 1.0k
Q11
R1 5.0k
Q2
R5 10k
R6 50k
R4 50k
Q3
Q7
Q9
Q12
Q13
Q19
Q18
R23 660

FIGURE 1. Schematic Diagram

The floating transistor output stage of the LM122 consists of Q32 through Q36. Q36 is the actual output transistor and is driven by emitter follower, Q33. Q34 and Q35 are antisaturation clamps to reduce stored charge in Q36 and to limit current through Q33. Q32 acts as a current limiter with the limit set at about 120 mA.

The regulator built into the LM122 is a $V_{BE}/\Delta V_{BE}$* type with a typical output voltage of 3.15V at up to 5.0 mA load current. Q18 and Q19 generate a 100μA current through Q19 which has a positive temperature coefficient of 0.33%/°C. This generates 1.2V and +4 mV/°C TC across R21. When added to the base emitter diode voltages of Q20 and Q21, a 2.4V, zero TC reference is established at the base of Q21. R18 and R19 form a divider to raise the regulated voltage to 3.15V. (This particular voltage was chosen because it can be operated off a single 5.0V supply and because one RC time constant is exactly 2.0V out of 3.15V.) Q23 buffers Q21 from supply fluctuations and sets up the currents for the bias section of the timer. Q20 is a single stage of voltage gain for the regulator. It is buffered by the series pass transistor, Q24. Q25, Q26, R25, and R26 are included for starting purposes and do not affect operation once current is flowing in the regulator section.

The function of the comparator is to cause an output change of state when the timing capacitor has charged to one RC time constant. Q11 through Q17 perform this function. Q14, Q15, Q16, and Q17 are a Darlington differential stage driving an active load formed by Q12 and Q13. Q11 is a second stage operating as a common emitter amplifier with R14 as its load resistor. For long timing intervals, the Darlington is run with no bleed current from Q30. Operating current for Q15 and Q16 is about 5μA per side. The specially processed lateral PNP's have h_{FE}'s of about 200, so operating current for Q14 and Q17 is typically 25 nA. At these current levels, the substrate PNP's have h_{FE}'s of 80, giving comparator input currents of 300 pA! One side of the comparator is tied to a divider (R16 and R17) which is set at 63.2% of the reference voltage — one RC time constant. The other side is connected to the external timing resistor and capacitor.

The logic section of the LM122 performs four functions: first, it provides a latching action to make the circuitry immune to retriggering during the timing interval; second, it simulates the action of an exclusive OR gate to generate a logic reverse function; additionally, it translates the low level output from the comparator to the high level swing needed to drive the floating transistor output; and finally, it drives the discharge transistor to reset the timing capacitor. Q2 and Q3 makeup the TTL compatible trigger input to the logic section. Q3 is a lateral PNP with 60V reverse emitter-base breakdown voltage, allowing negative inputs as high as −40V without harm to the chip. R5 is an epitaxial resistor which pinches off at 30V and has a breakdown of 80V. This allows positive input voltages of up to 40V on the trigger terminal even when operating the timer from a supply voltage of only 5.0V. Typical current drawn by the trigger terminal is 40μA at 2.0V and 600μA at 40V. Q4 and Q6 form a latch which self-limits at about 400μA and can be turned off by Q2. Q5 and Q7 interface the latch to the comparator so that the comparator can fire the latch at the end of the timing period. Q8, Q9, and Q10 perform the level shifting required to drive the output transistor and double as an exclusive OR gate, with the emitters of Q8 and Q9 as one input and the collectors of Q5 and Q11 as the second input. Grounding the Q8 and Q9 emitters reverses the effect of a signal appearing at the collector of Q11.

Biasing for the various circuits in the timer is generated by a string of PNP current sources consisting of Q27 through Q31. Current levels are established by the constant current source, Q23, driving diode connected Q28. The current from Q23 is 400μA, setting the drop across the emitter resistor, R28 plus R29, at 200 mV. Q29 delivers 10μA to the comparator and Q31 supplies a total of 100μA to the output transistor and logic circuitry. Part of Q29's collector is returned to Q27 to avoid having to use a large value resistor for R30. Q30 is completely off when using the timer for long timing periods. Shorting the boost terminal to V^+ adds about 5μA bleed current at the emitters of Q14 and Q17. This extra current is needed to slew the emitters of the comparator for timing periods less than 1 ms.

DESCRIPTION OF PIN FUNCTIONS

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on V^+ is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature controllers. Typical temperature drift of the reference is less than 0.01%/°C.

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*See AN-42, "On Card Regulator for Logic Circuits"

The trigger terminal is used to start timing. Threshold is typically 1.6V at +25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the trigger source is typically 20μA at threshold, rising to 600μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region.

If the trigger terminal is held high as the timing period ends, the output pulse will appear normally, but the timing capacitor will not be discharged. This is a necessary circuit action to prevent repetitive cycles when the trigger is held high. After the timing period, the capacitor is discharged when the trigger decreases below the threshold, without affecting the output.

The R/C pin is tied to the uncommitted side of the comparator and to the collector of the capacitor discharge transistor. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). The internal discharge transistor turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the R/C pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Input current to the R/C pin is typically 300 pA when the voltage is negative with respect to the V_{ADJ} terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is 30 nA. Gain of the comparator is very high, 200,000 or more depending on the state of the logic reverse pin and the connection of the output transistor.

The ground pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the V^+ terminal. Level shifting may be necessary for the input trigger if the trigger voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the ground terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the ground pin of the LM122 was tied to a negative supply.

The terminal labeled V_{ADJ} is tied to one side of the comparator and to a voltage divider between V_{REF} and ground. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to V_{ADJ}. This resistor is a pinched type with a typical variation in absolute value of ±100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between V_{REF} and ground) connected to V_{ADJ} should have a source resistance as low as possible. For small changes in V_{ADJ}, up to several kΩ is all right, but for large variations 250Ω or less should be maintained. This can be accomplished with a 1.0k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on V_{ADJ} from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The V_{ADJ} pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high when the V_{ADJ} pin is grounded. In this case, the output changes state, but the capacitor does not discharge. If the trigger drops while V_{ADJ} is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when V_{ADJ} is released, the output may or may not change state, depending the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output.

In noisy environments or in comparator-type applications, a bypass capacitor on the V_{ADJ} terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The emitter and the collector outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the emitter is tied to the ground pin and the signal is taken from the collector, or the collector is tied to V^+ and the signal is taken from the emitter. Variations on these basic connections are possible. The collector can be tied to any positive voltage up to 40V when the signal is taken from the emitter. However, the emitter will not be pulled higher than the supply voltage on the V^+ pin. Connecting the collector to a voltage less than the V^+ voltage is allowed. The emitter should not be connected to a hard source other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with collector-emitter voltages up to 40V. The power time product, however, must not exceed 15 watt·seconds for power levels above the maximum rating of the package. A short to 30V, for instance, can not be held for more than 4 seconds. These levels are based on a 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A boost pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current. For short time intervals where low input current is not needed, comparator operating current can be increased several orders of magnitude for fast operation. Shorting the boost terminal to V^+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5.0μA.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used.

The "Logic" pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the logic pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the logic pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the logic is typically 150 mV with 150μA flowing out of the terminal. If an active drive to the logic pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 75 mV at 200μA is required. A typical example of active drive to the logic pin is the pulse width discriminator shown in Figure 16.

CALCULATING WORST CASE TIMING ERROR

Timing errors for the LM122 come from the following sources:

1. Timing ratio error
2. Capacitor saturation voltage
3. Internal switching delays
4. Comparator bias current
5. External resistor and capacitor tolerance
6. Capacitor and board leakage

In general, errors 1 and 5 are the most significant, so they will be treated first.

For most applications, the major contribution to timing error from the LM122 itself is variation in timing ratio, which is the ratio of the comparator threshold voltage (typically 2.0V) to the voltage at the V_{REF} pin. A 1% error in this ratio results in a 1.8% initial timing error. Timing ratio error comes from variations in the internal divider ratio and from offset voltage in the comparator. The LM122 is specified to have a timing ratio from 0.626 to 0.638 at +25°C, giving a ±1.8% worst case contribution to initial timing period error. Over temperature, the worst case figures doubles to ±3.6%. If the initial error is trimmed out externally however, timing error drift due to timing ratio will generally be less than ±0.5% over temperature.

Adding all the contributions to timing error from the LM122 itself will usually give a figure in the 2% to 3% range at +25°C. External timing components (R_t and C_t) will normally contribute much more error than this unless selected components are used. ±5% tolerance on R_t and C_t will increase the worst case error to 12% to 13%. By trimming out initial component errors, an exact initial timing period can be obtained, but temperature drift then becomes the limiting factor. For most applications, the contributions to timing period drift due to the LM122 itself will be in the 0.005%/°C to 0.02%/°C range.

If accurate timing over temperature is required, low drift components must be used for R_t and C_t. Capacitors are available with temperature coefficients of 100 to 200 ppm/°C. Resistors, at least in the lower ranges, are available with TC's much better than this. Above 1 MΩ, however, care must be used in the selection of a low TC resistor. Units are available up to 100 MΩ with less than 100 ppm/°C drift.

Capacitor saturation voltage is the voltage still remaining on the timing capacitor after it has been reset to as near ground as the internal discharge transistor can drive it. For timing resistors 1 MΩ or greater, this remaining voltage is typically 2.5 mV. For smaller timing resistors, the capacitor saturation voltage can be calculated by the following formula:

$$V_C \approx 2.5\text{ mV} + \frac{(V_{REF})^{*}\,(80\Omega)}{R_t}$$

$^{*}V_{REF} = 3.15\text{V}$

The effect of V_C on timing period is linear at 0.03%/mV. Temperature dependence of V_C is typically +0.2%/°C for $R_t \leq 300\text{k}\Omega$, rising to 0.4%/°C for $R_t = 10\text{ k}\Omega$. This gives a typical temperature coefficient of timing error *due to V_C* of (0.002) (2.5 mV) (0.03%/mV) = 0.0015%/°C for $R_t \geq 1\text{ M}\Omega$ and (0.004) (24 mV) (0.03%/mV) ≈ 0.003%/°C for $R_t = 10\text{ k}\Omega$. Since most applications can use timing resistors in the range of 100 kΩ and up, error *from capacitor saturation voltage* rarely exceeds 0.15% initially, with ±0.05% variation over the full temperature range.

Internal switching delays cause errors which tend to be a fixed time rather than a percentage of the timing period. In the boosted mode this delay is typically 800 ns, and with the boost off; the delay is about 25μs. These times can be added directly to the calculated timing period for worst case analysis. For timing periods longer than 25 ms, the 25μs delay gives an error of 0.1% or less. In the range of 1 or 25 ms, error due to delays is 0.1% or less for the boosted mode, rising to a maximum of 4.0% in the unboosted mode. At $\tau = 10\mu s$, delay is the major contribution to timing error ($\approx$ 8%).

Comparator bias current contributes a negligible timing error for all but very long time timing periods. Error can be calculated with a simple formula:

Error (%) = $-50 \cdot R_t \cdot I_b$ (Note sign)
I_b = Comparator Bias Current
R_t = Timing Resistor

For R_t = 100 MΩ and I_b = 0.3 nA (typical) a 1.5% reduction in timing period is incurred. For worst case calculations at +25°C, an I_b of 1 nA maximum is specified in the unboosted mode and 100 nA in the boosted mode. At temperatures below +25°C, these numbers still hold. At +125°C, I_b increases due to leakage to a maximum of ±5 nA unboosted. For worst case calculations below +125°C, the leakage error (5 nA) can be assumed to halve for each 10°C drop below +125°C. At +95°C for instance, the leakage component of I_b would be (5 nA/8) $\approx$ 0.6 nA for a total I_b of 1.6 nA worst case. For the commercial LM322 and LM3905, worst case I_b is 2 nA at +75°C, and for the LM2905 I_b is 2 nA maximum at +85°C. For temperatures between −25°C and +85°C, the TC of I_b is typically 5 pA/°C in the unboosted mode and 100 pA/°C in the boosted mode. For a 100 MΩ R_t, this 5 pA/°C contributes −0.025%/°C to timing period drift.

$$\text{Error}(\%/^\circ C) = (-50)(\Delta I_b/\Delta T)(R_t)$$

For worst case calculations a $\Delta I_b/\Delta T$ ($-25 \leq T_A \leq +85^\circ C$) of 12 pA/°C may be used for the LM122/LM222 and 20 pA/°C for the LM322 and LM2905/LM3905.

External leakage paths may cause timing errors for large values of R_t and high board temperatures. Connections made to the R/C pin should be kept free of dust, moisture, and soldering flux if long time intervals are to be kept accurate. All package types have the R/C pin located between V_{REF} and the ground pin to minimize these leakages.

DESIGN HINTS

Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will start a timing cycle automatically (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in Figure 2. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

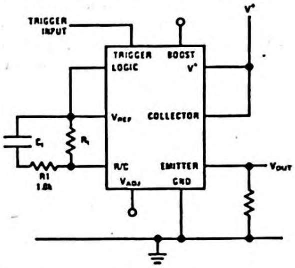


FIGURE 2. Eliminating Initial Timing Cycle

Using Electrolytic Timing Capacitors

Electrolytic capacitors are not usually recommended for timing because of their unstable capacitance and high leakage. For long timing periods (> 10 seconds) at moderate temperatures (0°C to 50°C) however, an electrolytic may be attractive because of its low cost per microfarad Solid tantalum capacitors such as the Kemet* C series T310 (molded epoxy) or T110 (hermetic) are recommended. These units have long term stabilities of 2% to 3% and a temperature coefficient of +0.2%/°C. Selected units are available for timing use with very low leakage.

Reset Time

The timing capacitor used with the LM122 is reset with an internal transistor which has a collector offset voltage of 2.5 mV @ 1μA with approximately 80Ω of collector resistance The time required to reset this capacitor determines the minimum time between timing pulses. An approximate formula for reset time is:

$$\text{Reset Time} = (80\ \Omega)\,(C_t{}^{\dagger})\,(5)$$

$^\dagger C_t$ = External timing capacitor.

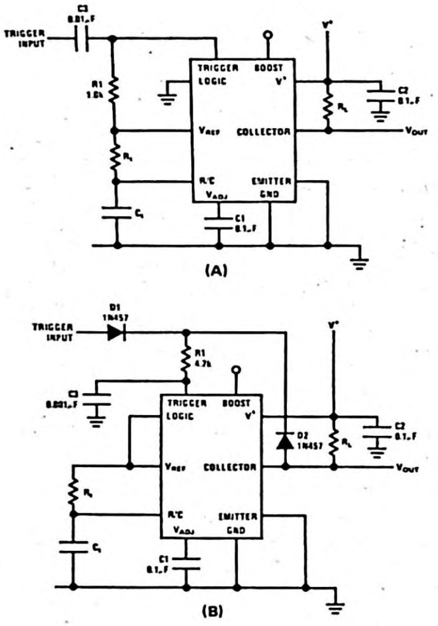
NOISY ENVIRONMENTS

The LM122 is relatively insensitive to noise on supply lines and to radiated energy. In *extremely* noisy environments however, it may be necessary to configure the LM122 differently, both to eliminate false triggering and to prevent premature end of a timing period. The circuit "a" shown in Figure 3 has been set up for maximum noise rejection. C1 bypasses the V_{ADJ} pin because of the relatively high impedance ($\simeq$ 30 kΩ) of this point. Negative spikes on the V_{ADJ} pin will cause premature end of the timing period. C2 bypasses the supply for rejection of fast transients. R1 sets up the trigger pin to a "normally high" condition. This prevents extremely high electromagnetic fields from triggering the internal flip-flop during a timing period. The input trigger signal is capacitively coupled through C3. Triggering occurs on the *negative* edge of the trigger pulse as shown in the waveform sketch next to Figure 21.

---

*Manufactured by Union Carbide

If the output voltage from the LM122 can be set up to go "high" during the timing cycle, the alternate connection shown in "b" can be used. Here, the trigger is held high by D2 during the timing period. When the output goes low after the timing period is over, the circuit may be retriggered immediately via D1. R1 and C3 suppress unwanted spikes at the trigger input.


TRIGGER INPUT
C3 0.01µF
R1 1.0k
TRIGGER LOGIC
BOOST
V+
VREF
COLLECTOR
R/C
VADJ
EMITTER
GND
Rt
Ct
RL
C1 0.1µF
C2 0.1µF
VOUT
D1 1N457
R1 4.7k
C3 0.001µF
D2 1N457
(A)

(B)

FIGURE 3. Maximum Noise Immunity

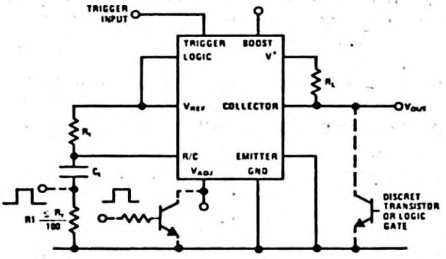
ABORTING A TIMING CYCLE (Figure 4)

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300µA.

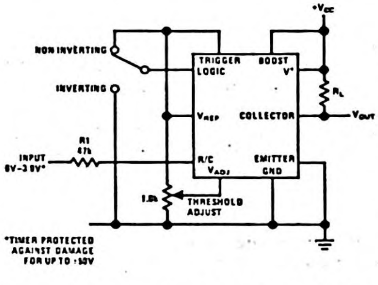
A timing cycle may be also ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.


TRIGGER INPUT
TRIGGER LOGIC
BOOST
V+
VREF
COLLECTOR
R/C
VADJ
EMITTER
GND
RL
Rt
Ct
VOUT
R1 ≤ Rt/100
DISCRET TRANSISTOR OR LOGIC GATE
FIGURE 4. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

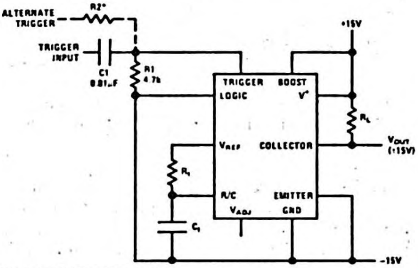
Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25µV/°C in the boosted mode and 50µV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in Figure 5. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply should make this comparator very useful.


+VCC
NON INVERTING
INVERTING
TRIGGER LOGIC
BOOST
V+
RL
VREF
COLLECTOR
VOUT
R1 47k
INPUT 0V-3.0V*
R/C
VADJ
EMITTER
GND
1.0k
THRESHOLD ADJUST
*TIMER PROTECTED AGAINST DAMAGE FOR UP TO ±50V
FIGURE 5. Comparator With 0 Volts to 3.0 Volts Threshold

Using Dual Supplies

The LM122 can be operated off dual supplies as shown in Figure 6. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.

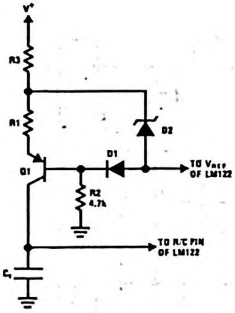

ALTERNATE TRIGGER
R2*
TRIGGER INPUT
C1
0.01µF
R1
4.7k
+15V
TRIGGER LOGIC
BOOST V+
RL
VREF
COLLECTOR
VOUT (±15V)
Rt
R/C VADJ
EMITTER GND
Ct
−15V

*SELECT FOR PROPER LEVEL SHIFT
EMITTER TERMINAL OR EMITTER LOAD MUST BE TIED TO GND PIN OF TIMER.

FIGURE 6. Operating Off Dual Supplies

LINEARIZING THE CHARGING SWEEP

In some applications (such as a linear pulse width modulator) it may be desireable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in the accompanying sketch.


V+
R3
R1
D2
D1
Q1
TO VREF OF LM122
R2
4.7k
TO R/C PIN OF LM122
Ct

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability if not critical. With D1 and R2 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

APPLICATIONS

Basic Timers

Figure 7 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch alongside Figure 7.

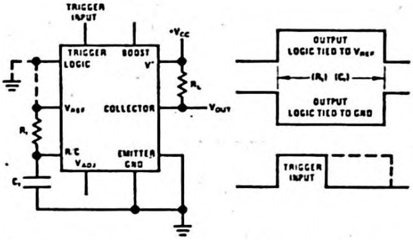

TRIGGER INPUT
+VCC
TRIGGER LOGIC
BOOST V+
RL
VREF
COLLECTOR
VOUT
Rt
R/C VADJ
EMITTER GND
Ct
OUTPUT LOGIC TIED TO VREF
(Rt) (Ct)
OUTPUT LOGIC TIED TO GND
TRIGGER INPUT

FIGURE 7. Basic Timer-Collector Output and Timing Chart

Figure 8 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

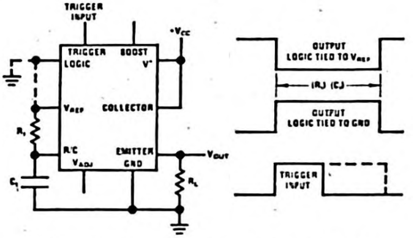

TRIGGER INPUT
+VCC
TRIGGER LOGIC
BOOST V+
VREF
COLLECTOR
Rt
R/C VADJ
EMITTER GND
VOUT
RL
Ct
OUTPUT LOGIC TIED TO VREF
(Rt) (Ct)
OUTPUT LOGIC TIED TO GND
TRIGGER INPUT

FIGURE 8. Basic Timer-Emitter Output and Timing Chart

Figure 9 shows the timer interfacing 5V logic to a high voltage relay. Although the V^+ terminal could be tied to the +28V supply, this would be an unnecessary waste of power in the IC. In any case, the threshold for the trigger is 1.6V regardless of where V^+ is tied.

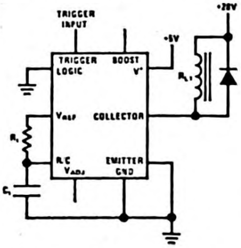

TRIGGER INPUT
+28V
+5V
TRIGGER LOGIC
BOOST V+
RL
VREF
COLLECTOR
Rt
R/C VADJ
EMITTER GND
Ct

FIGURE 9. 5 Volt Logic Supply Driving 28 Volt Relay

Figure 10 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL.

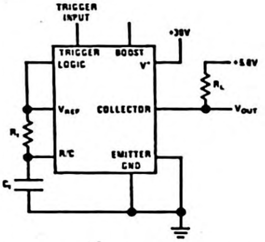

TRIGGER INPUT
+30V
TRIGGER LOGIC
BOOST
V+
+5.0V
R_L
V_{REF}
COLLECTOR
V_{OUT}
R_t
R/C
EMITTER GND
C_t

FIGURE 10. 30 Volt Supply Interfacing to 5 Volt Logic

Figure 11 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. Figure 12 is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.

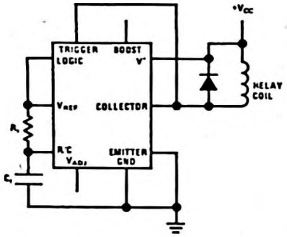

+V_{CC}
TRIGGER LOGIC
BOOST
V+
RELAY COIL
V_{REF}
COLLECTOR
R_t
R/C
V_{ADJ}
EMITTER GND
C_t

FIGURE 11. Time Out on Power Up (Relay Energized R_tC_t Seconds After V_{CC} is Applied)

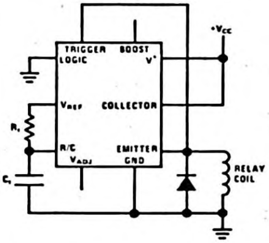
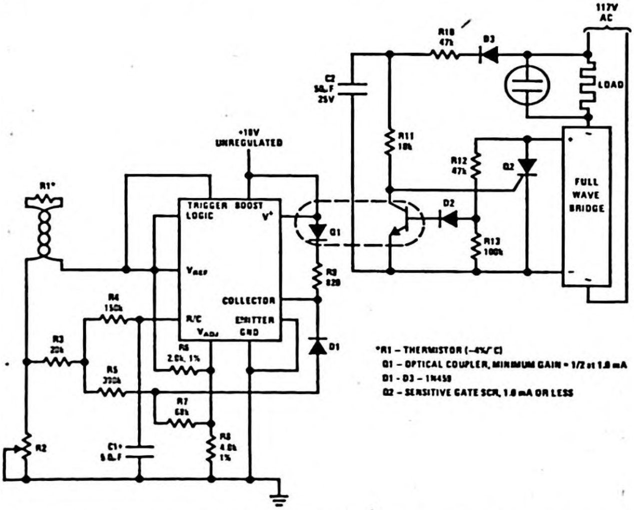

+V_{CC}
TRIGGER LOGIC
BOOST
V+
V_{REF}
COLLECTOR
R_t
R/C
V_{ADJ}
EMITTER GND
RELAY COIL
C_t

FIGURE 12. Time Out on Power Up (Relay Energized *Until* R_tC_t Seconds After V_{CC} is Applied)

Figure 13 is a more advanced application of the LM122 as a proportioning temperature controller with optical isolation and synchronized zero crossing features. The timing function is not used. Instead the trigger terminal is held high and the LM122 is used as a high gain comparator with a built in reference. R1 is a thermistor with a −4%/°C temperature coefficient used as the sensor. R2 is used to set the temperature to be controlled by R1. R3 through R8 set up the proportioning action. R3 raises the impedance of the R1/R2 divider so that R5 sees a relatively constant impedance independent of the set point temperature. R6 and R8 reduce the V_{ADJ} impedance so that internal variations in divider impedance do not affect proportioning action. R5 and R7 set


117V AC
R10 47k
D3
LOAD
C2 50µF 25V
+10V UNREGULATED
R11 10k
R12 47k
Q2
FULL WAVE BRIDGE
R1*
TRIGGER LOGIC
BOOST
V+
Q1
D2
R13 100k
V_{REF}
R9 820
COLLECTOR
R4 150k
R/C
V_{ADJ}
EMITTER GND
D1
R3 20k
R6 2.0k, 1%
R5 330k
R7 68k
R2
C1* 5.0µF
R8 4.0k 1%

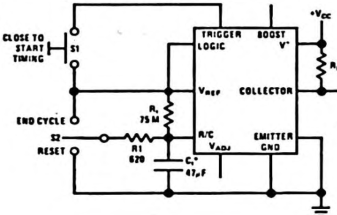
*R1 – THERMISTOR (−4%/°C)
Q1 – OPTICAL COUPLER, MINIMUM GAIN = 1/2 at 1.0 mA
D1 - D3 – 1N459
Q2 – SENSITIVE GATE SCR, 1.0 mA OR LESS

FIGURE 13. Proportioning Temperature Controller with Synchronized Zero-Crossing

the actual width of the proportioning band and can be scaled as necessary to alter the width of the band. Larger resistors make the band narrower. The values shown give approximately a 1°C band. R4 and C1 determine the proportioning frequency which is about 1 Hz with the values shown. C1 or R4 can change to alter frequency, but R4 should be between 50k and 500k, and C1 must be a low leakage type to prevent temperature shifts. D1 prevents supply voltage fluctuations from affecting set point or proportioning band. Any unregulated supply between 6V and 15V is satisfactory.

Q1 is an optical isolator with a minimum gain of 0.5. With the values shown for R9, R10, and R11, Q1 is over-driven by at least 3 to 1 to insure deep saturation for reliable turn off of the SCR. Q2 must be a sensitive gate device with a worst case gate firing current of 0.5 mA. R12, R13, and D2 implement the synchronized zero-crossing feature by preventing Q1 from turning off after the voltage across Q2 has climbed above 2.5V. D3, R10, and C2 provide a source of semifiltered dc current for SCR gate drive. D3 and Q2 must have a minimum breakdown of 200V.

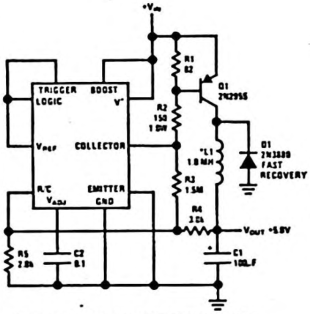
Figure 14 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released. The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.


CLOSE TO START TIMING
S1
TRIGGER
LOGIC
BOOST
V+
+VCC
RL
VREF
COLLECTOR
VOUT
END CYCLE
Rt
75 M
S2
RESET
R1
620
R/C
VADJ
EMITTER
GND
Ct*
47μF

*DEARBORN ELECTRONICS LP3A1A476K POLYCARBONATE

FIGURE 14. One Hour Timer With Reset and Manual Cycle End

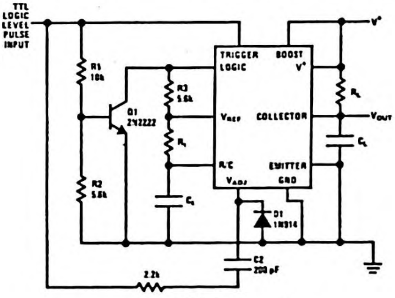
Figure 15 is another application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP switch transistor. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω the Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.


+VIN
R1
82
Q1
2N2955
TRIGGER
LOGIC
BOOST
V+
R2
150
1.5W
VREF
COLLECTOR
*L1
1.0 MH
D1
2N3880
FAST
RECOVERY
R3
1.5M
R/C
VADJ
EMITTER
GND
R4
3.0k
VOUT +5.0V
R5
2.8k
C2
0.1
C1
100μF

*NO. 22 WIRE WOUND ON MOLYBDENUM PERMALLOY CORE

FIGURE 15. 5 Volt Switching Regulator With 1.0 Amp Output and 5.5 Volt Minimum Input

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made (Figure 16).


TTL LOGIC LEVEL PULSE INPUT
V+
R1
10k
TRIGGER
LOGIC
BOOST
V+
RL
R3
5.6k
Q1
2N2222
VREF
COLLECTOR
VOUT
Rt
Ct
R2
5.6k
R/C
VADJ
EMITTER
GND
Ct
D1
1N914
C2
200 pF
2.2k

$^*V_{OUT} = 0$ FOR $W < R_t C_t$

PULSE OUT $= W - R_t C_t$ FOR $W > R_t C_t$

FIGURE 16. Pulse Width Detector

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \cdot C_t$. C2 insures no output pulse for short (< RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops.

C_L filters the narrow spikes which would occur at the output due to interval delays during switching.

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In Figure 17, the timer is used to drive a relay "on" R_t C_t seconds after application of power. "off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

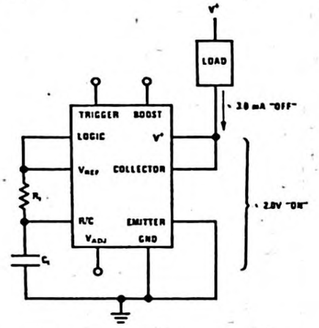

V⁺
LOAD
3.0 mA "OFF"
TRIGGER LOGIC
BOOST V⁺
V_REF
COLLECTOR
R_t
R/C V_ADJ
EMITTER GND
2.8V "ON"
C_t

FIGURE 17. Two-Terminal Time Delay Switch

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in Figure 18. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

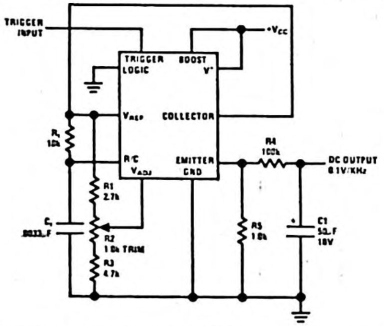

TRIGGER INPUT
+V_CC
TRIGGER LOGIC
BOOST V⁺
V_REF
COLLECTOR
R_t 10k
R/C V_ADJ
EMITTER GND
R4 100k
DC OUTPUT 0.1V/KHz
R1 2.7k
C_t .0033 μF
R2 10k TRIM
R3 4.7k
R5 10k
C1 50 μF 10V

FIGURE 18. Frequency to Voltage Converter (Tachometer) Output Independent of Supply Voltage

In some applications it is desirable to reduce supply drain to zero between timing cycles. In Figure 19 this is accomplished by using an external PNP as a latch to drive the V⁺ pin of the timer.

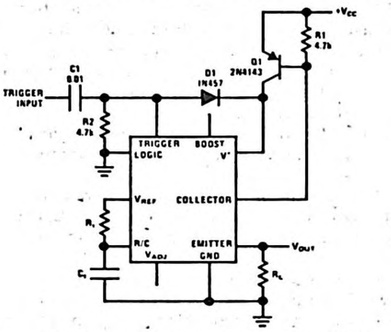

+V_CC
R1 4.7k
Q1 2N4143
C1 0.01
D1 1N457
TRIGGER INPUT
R2 4.7k
TRIGGER LOGIC
BOOST V⁺
V_REF
COLLECTOR
R_t
R/C V_ADJ
EMITTER GND
V_OUT
C_t
R_L

FIGURE 19. Zero Power Dissipation Between Timing Intervals

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents coupling back into the trigger signal from the dc load created by the trigger input. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in Figure 20. Operating frequency is $1/(R_t\ C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2\ C_f$. For optimum frequency

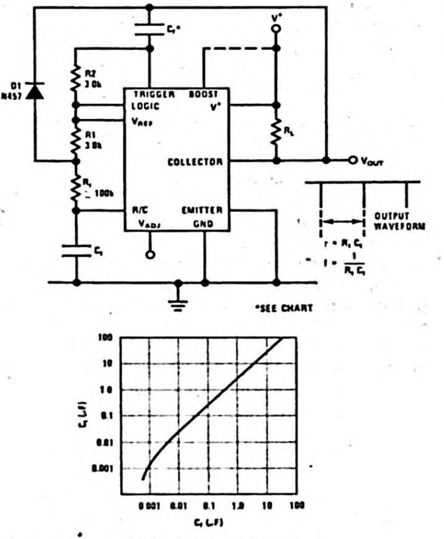

C_f*
V⁺
D1 1N457
R2 3.0k
TRIGGER LOGIC
BOOST V⁺
V_REF
R1 3.0k
R_L
COLLECTOR
V_OUT
R_t 100k
R/C V_ADJ
EMITTER GND
OUTPUT WAVEFORM
τ = R_t C_t
f = 1/(R_t C_t)
C_t
*SEE CHART
100
10
1.0
0.1
0.01
0.001
C_f (μF)
0.001
0.01
0.1
1.0
10
100
C_t (μF)

FIGURE 20. Oscillator

stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be chosen from the graph included with Figure 20. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t > 500k$.

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In Figure 21, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with Figure 21 shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately 0.5 to 1.5 R1 C1 depending on the trigger amplitude, or about 2.5 to 7.5µs with the values shown. This time will have to be increased for C_t larger than 0.01µF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

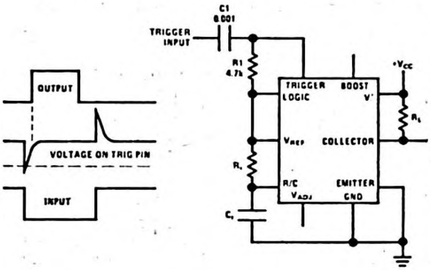

C1
0.001
TRIGGER INPUT
R1
4.7k
OUTPUT
VOLTAGE ON TRIG PIN
INPUT
TRIGGER LOGIC
BOOST V⁺
+Vcc
R_L
V_{REF}
COLLECTOR
R_t
R/C V_{ADJ}
EMITTER GND
C_t

FIGURE 21. Timer Triggered by Negative Edge of Input Pulse

The LM122 can be connected as a chain of timers quite easily with no interface required. In Figure 22A and 22B, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.

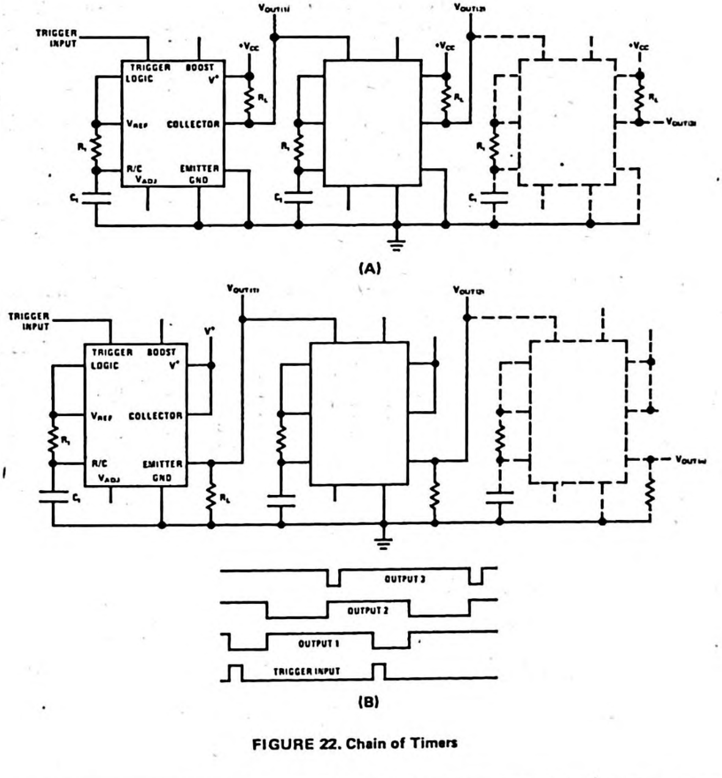
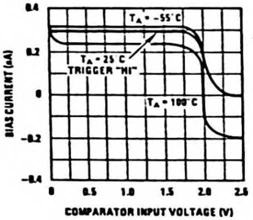

TRIGGER INPUT
TRIGGER LOGIC
BOOST V⁺
V_{REF}
COLLECTOR
R/C V_{ADJ}
EMITTER GND
+Vcc
$V_{OUT(1)}$
$V_{OUT(2)}$
$V_{OUT(3)}$
R_L
R_t
C_t
(A)
V⁺
OUTPUT 3
OUTPUT 2
OUTPUT 1
TRIGGER INPUT
(B)

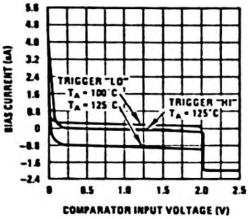
FIGURE 22. Chain of Timers

typical performance characteristics

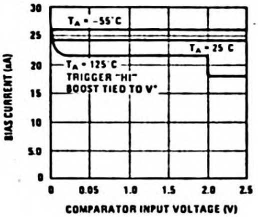
Comparator Bias Current



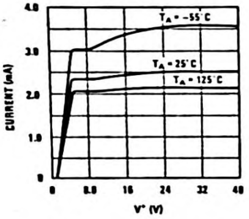
Comparator Bias Current



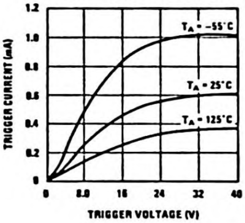
Comparator Bias Current



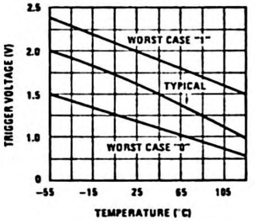
Supply Current



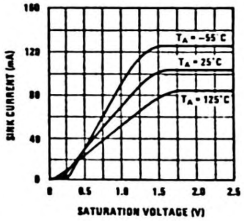
Trigger Input Characteristics



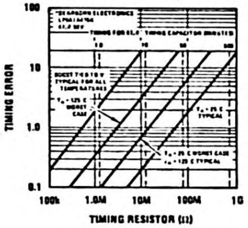
Trigger Threshold



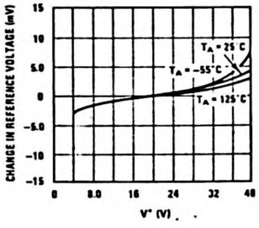
Collector Output Saturation Characteristics at High Current



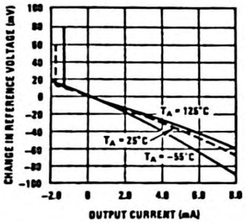
Timing Error Due to Comparator Bias Current



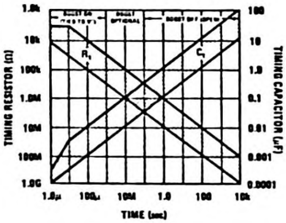
Reference Regulation



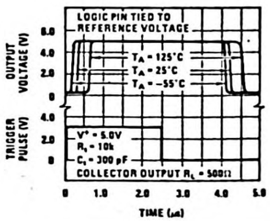
Reference Regulation



Suggested Timing Components



Short Output Pulse



LM340 Series Three Terminal Positive Regulators

National Semiconductor
Application Note 103
Nello Sevastopoulos
George Cleveland
Jim Sherwin
March 1974

INTRODUCTION

The LM340-XX are three terminal 1.0A positive voltage regulators with preset output voltages of 5.0V, 6.0V, 8.0V, 12V, 15V, 18V or 24V. The LM340 regulators are complete 3-terminal regulators requiring no external components for normal operation. However, by adding a few parts, one may improve the transient response, provide for a variable output voltage, or increase the output current. Included on the chip are all of the functional blocks required of a high stability voltage regulator; these appear in Figure 1. The error amplifier is internally compensated; the voltage reference is especially designed for low noise and high predictability; and, as the pass element is included, the regulator contains fixed current limiting and thermal protection. The LM340 is available in either metal can TO-3 or plastic TO-220 package.

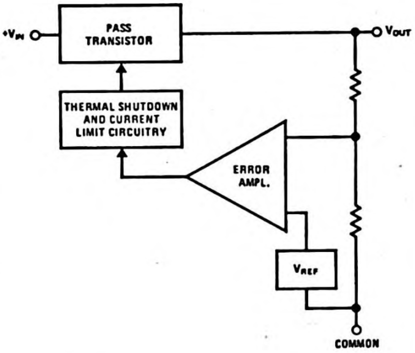


FIGURE 1. Functional Block of the LM340

1. CIRCUIT DESIGN

Voltage Reference

Usually IC voltage regulators use temperature-compensated zeners as references. Such zeners exhibit BV > 6.0V which sets the minimum supply voltage somewhat above 6.0V. Additionally they tend to be noisy, thus a large bypass capacitor is required.

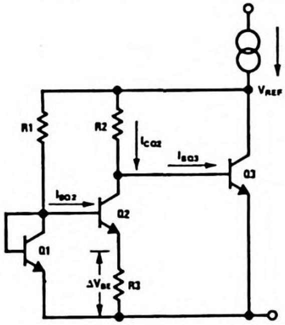


FIGURE 2. Simplified Volt Reference

Figure 2 illustrates a simplified reference using the predictable temperature, voltage, and current relationship of emitter-base junctions.

Assuming $J_{Q1} > J_{Q2}$, $I_{CQ2} >> I_{BQ2} = I_{BQ3}$, Area (emitter Q1) = Area (emitter Q2),

and $V_{BEQ1} = V_{BEQ3}$, then (1-1)

$$V_{REF} \simeq \left(\frac{kT}{q} \ln \frac{R2}{R1}\right) \frac{R2}{R3} + V_{BEQ3} \qquad (1\text{-}2)$$

Simplified LM340

In Figure 3 the voltage reference includes R1 – R3 and Q1 – Q5. Q3 also acts as an error amplifier and Q6 as a buffer between Q3 and the current source. If the output drops, this drop is fed back, through R4, R5, Q4, Q5, to the base of Q3. Q7 then conducts more current re-establishing the output given by:

$$V_{OUT} = V_{REF} \frac{R4 + R5}{R4}$$

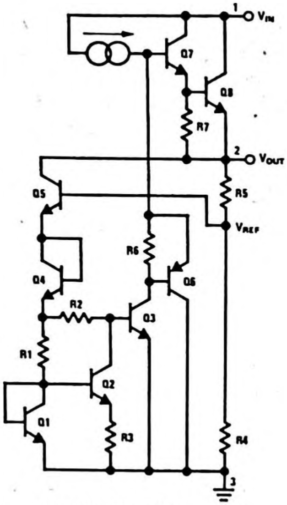

1
V_{IN}
Q7
Q8
R7
2
V_{OUT}
Q5
R5
V_{REF}
R6
Q4
Q6
R2
Q3
R1
Q2
Q1
R3
R4
3

FIGURE 3. LM340 Simplified

Complete Circuit of the LM340 (Figure 4)

Here $(J_{Q2}, J_{Q3}) > (J_{Q4}, J_{Q5})$ and a positive TC ΔV_{BE} appears across R6. This is amplified by 17, (R6/R6 = 17) and is temperature compensated by the V_{BE} of Q6, Q7, Q8 to develop the reference voltage. R17 is changed to get the various fixed output voltages.

Short Circuit Protection

A) $V_{IN} - V_{OUT} < 6.0V$: There is no current through D2 and the maximum output current will be given by:

$$I_{OUT\,MAX} = \frac{V_{BEQ14}}{R16} \simeq 2.2A \; (T_j = 25°C) \qquad (1\text{-}4)$$

B) $V_{IN} - V_{OUT} > 6.0V$: To keep Q16 operating within its maximum power rating the output current limit must decrease as $V_{IN} - V_{OUT}$ increases. Here D2 conducts and the drop across R16 is less than V_{BE} to turn on Q14. In this case I_{OUT} maximum is:

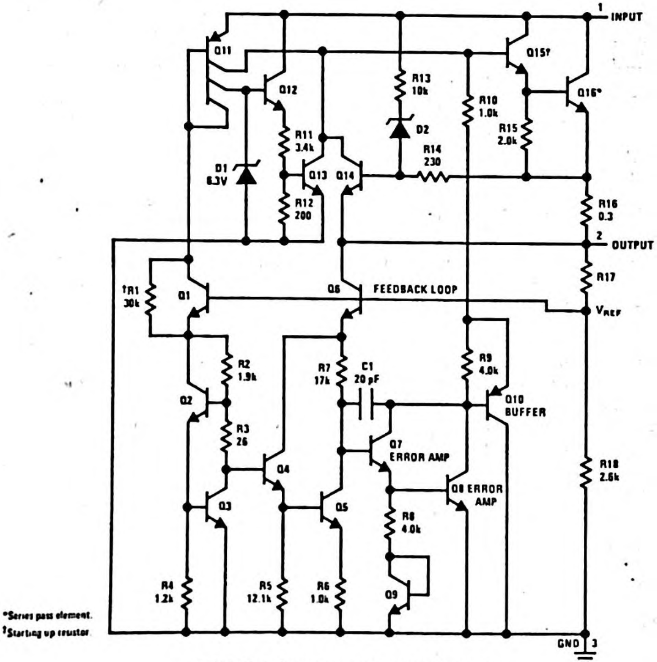
$$I_{OUT\,MAX} = \frac{1}{R16}\left(V_{BEQ14} - \frac{\left[(V_{IN} - V_{OUT}) - V_{ZD2} - V_{BEQ14}\right]}{R13} R14\right) \qquad (1\text{-}5)$$

$$= 0.077\,[37.2 - (V_{IN} - V_{OUT})]\ (A)$$

at $T_j = 25°C$

Thermal Shut Down

In Figure 4 the V_{BE} of Q13 is clamped to 0.4V. When the die temperature reaches approximately +175°C the V_{BE} to turn on Q13 is 0.4V. When Q13 turns on it removes all base drive from Q15


1
INPUT
Q11
Q12
Q15†
Q16*
R13
10k
R10
1.0k
D2
R15
2.0k
R11
3.4k
R14
230
D1
6.3V
Q13
Q14
R12
200
R16
0.3
2
OUTPUT
R17
†R1
30k
Q1
Q6
FEEDBACK LOOP
V_{REF}
R2
1.9k
R7
17k
C1
20 pF
R9
4.0k
Q2
Q10
BUFFER
R3
26
Q7
ERROR AMP
Q4
R18
2.6k
Q8 ERROR
AMP
Q3
Q5
R8
4.0k
R4
1.2k
R5
12.1k
R6
1.0k
Q9
GND
3

*Series pass element.

†Starting up resistor

FIGURE 4. Complete Circuit of the LM340

which turns off the regulator thus preventing a further increase in die temperature.

Power Dissipation

The maximum power dissipation of the LM340 is given by:

$$P_{D\,MAX} = (V_{IN\,MAX} - V_{OUT})\, I_{OUT\,MAX} + V_{IN\,MAX}\, I_Q \text{ (W)} \qquad (1\text{-}6)$$

The maximum junction temperature (assuming that there is no thermal protection) is given by:

$$T_{JM} = \frac{36 - 13\, I_{OUT\,MAX} - (V_{IN} - V_{OUT})}{0.0855} + 25^\circ\text{C} \qquad (1\text{-}7)$$

Example:

$V_{IN\,MAX} = 23\text{V}$, $I_{OUT\,MAX} = 1.0\text{A}$, LM340T-15.

Equation (1-7) yields: $T_{JM} = 200^\circ\text{C}$. So the T_j max of 150°C specified in the data sheet should be the limiting temperature.

From (1-6) $P_D \cong 8.1\text{W}$. The thermal resistance of the heat sink can be estimated from:

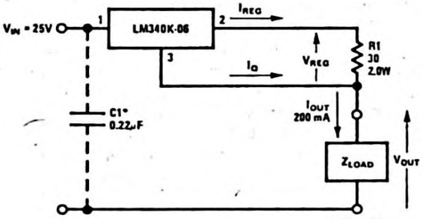
$$\theta_{s\text{-}a} = \frac{T_{JMAX} - T_A}{P_D} - (\theta_{j\text{-}c} + \theta_{c\text{-}s})(^\circ\text{C/W}) \qquad (1\text{-}8)$$

The thermal resistance $\theta_{j\text{-}c}$ (junction to case) of the TO-220 package is 6°C/W, and assuming a $\theta_{c\text{-}s}$ (case to heat sink) of 0.4, equation (1-8) yields:

$$\theta_{s\text{-}a} = 8.4^\circ\text{C/W}$$

2. CURRENT SOURCE

The circuit shown on Figure 5 provides a constant output current (equal to $V_{OUT}/R1$ or 200 mA) for a variable load impedance of 0 to 85Ω. Using the following definitions and the notation shown on Figure 5, Z_{OUT} and I_{OUT} are:



*Required if regulator is located far from power supply filter.

FIGURE 5. Current Source

Q_{CC}/V = Quiescent current change per volt of input/output (pin 1 to pin 2) voltage change of the LM340

L_r/V = Line regulation per volt: the change in the LM340 output voltage per volt of input/output voltage change at a given I_{OUT}.

$$\Delta I_{OUT} = (Q_{CC}/V)\,\Delta V_{OUT} + \frac{L_r/V}{R1}\,\Delta V_{OUT} \qquad (2\text{-}1)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \qquad (2\text{-}2)$$

$$Z_{OUT} = \frac{\Delta V_{OUT}}{(Q_{CC}/V)\,\Delta V_{OUT} + \dfrac{(L_r/V)}{R1}\,\Delta V_{OUT}} \qquad (2\text{-}3)$$

$$Z_{OUT} = \frac{1}{(Q_{CC}/V) + \dfrac{(L_r/V)}{R1}} \qquad (2\text{-}4)$$

The LM340-06 data sheet lists maximum quiescent current change of 1.3 mA for an 8.0V to 25V change in input voltage; and a line regulation (interpolated for I_{OUT} = 200 mA) of 75 mV maximum for an 8.0V to 25V change in input voltage:

$$Q_{CC}/V = \frac{1.3\text{ mA}}{17\text{V}} = 76\mu\text{A/V} \qquad (2\text{-}5)$$

$$L_r/V = \frac{75\text{ mV}}{17\text{V}} = 4.4\text{ mV/V} \qquad (2\text{-}6)$$

The worst case change in the 200 mA output current for a 1.0V change in output or input voltage using equation 2-1 is:

$$\frac{\Delta I_{OUT}}{1.0\text{V}} = 76\mu\text{A} + \frac{4.4\text{ mV}}{30\Omega} = 223\mu\text{A} \qquad (2\text{-}7)$$

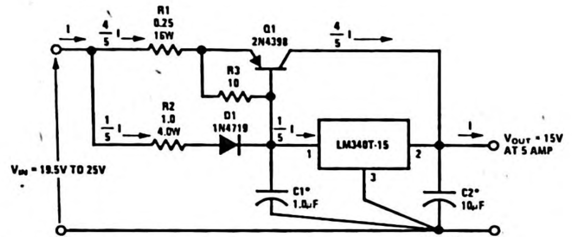
and the output impedance for a 0 to 85Ω change in Z_L using equation 2-4 is:

$$Z_{OUT} = \frac{1}{76\mu\text{A} + \dfrac{4.4\text{ mV}}{30\Omega}} = 4.5\text{ k}\Omega \qquad (2\text{-}8)$$

Typical measured values of Z_{OUT} varied from 10 – 12.3 kΩ, or 81 – 100μA/V change input or output (approximately 0.05%/V).

3. HIGH CURRENT REGULATOR WITH SHORT CIRCUIT CURRENT LIMIT

The 15V regulator circuit of Figure 6 includes an external boost transistor to increase output current capability to 5.0A. Unlike the normal boosting methods, it maintains the LM340's ability to provide short circuit current limiting and thermal shut-down without use of additional active components. The extension of these safety features to the external pass transistor Q1 is based on a current sharing scheme using R1, R2, and D1. Assuming



*Solid tantalum.

Note 1: Current sharing between the LM340 and Q1 allows the extension of short circuit current limit, safe operating area protection, and (assuming Q1's heat sink has four or more times the capacity of the LM340 head sink) thermal shutdown protection.

Note 2: $I_{SHORT\ CIRCUIT}$ is approximately 5.5 amp.

Note 3: $I_{OUT\ MAX}$ at V_{OUT} = 15V is approximately 9.5 amp.

FIGURE 6. 15V 5.0A Regulator with Short Circuit Current Limit

the base-to-emitter voltage of Q1 and the voltage drop across D1 are equal, the voltage drops across R1 and R2 are equal. The currents through R1 and R2 will then be inversely proportional to their resistances. For the example shown on Figure 6, resistor R1 will have four times the current flow of R2. For reasonable values of Q1 beta, the current through R1 is approximately equal to the collector current of Q1; and the current through R2 is equal to the current flowing through the LM340. Therefore, under overload or short circuit conditions the protection circuitry of the LM340 will limit its own output current and, because of the R1/R2 current sharing scheme, the output current of Q1 as well. Thermal overload protection also extends Q1 when its heat sink has four or more times the capacity of the LM340 heat sink. This follows from the fact that both devices have approximately the same input/output voltage and share the load current in a ratio of four to one.

The circuit shown on Figure 6 normally operates at up to 5.0A of output current. This means up to 1.0A of current flows through the LM340 and up to 4.0A flows through Q1. For short term overload conditions the curve of Figure 7 shows the maximum instantaneous output current versus temperature for the boosted regulator. This curve reflects the approximately 2.0A current limit of the LM340 causing an 8.0A current limit in the pass transistor, or 10A, total. Under continuous short circuit conditions the LM340 will heat up and limit to a steady total state short circuit current of 4.0A to 6.0A as shown in Figure 8. This curve was taken using a Wakefield 680-75 heat sink (approximately 7.5°C/W) at a 25°C ambient temperature.

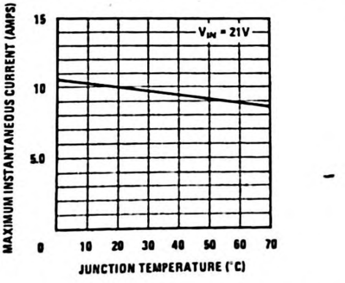


FIGURE 7. Maximum Instantaneous Current vs Junction Temperature

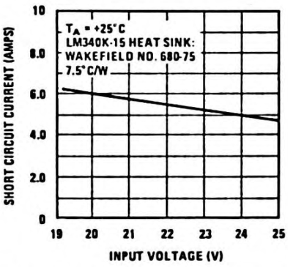


FIGURE 8. Continuous Short Circuit Current vs Input Voltage

For optimum current sharing over temperature between the LM340 and Q1, the diode D1 should be physically located close to the pass transistor on the heat sink in such a manner as to keep it at the same temperature as that of Q1. If the LM340 and Q1 are mounted on the same heat sink the LM340 should be electrically isolated from the heat sink since its case (pin 3) is at ground potential and the case of Q1 (its collector) is at the output potential of the regulator. Capacitors C1 and C2 are required to prevent oscillations and improve the output impedance respectively. Resistor R3 provides a path to unload excessive base charge from the base of Q1 when the regulator goes suddenly from full load to no load. The single point ground system shown on Figure 6 allows the sense pins (2 and 3) of the LM340 to monitor the voltage directly at the load rather than at some point along a (possibly) resistive ground return line carrying up to 5.0A of load current. Figure 9 shows the typical variation of load regulation versus load current for the boosted regulator. The insertion of the external pass transistor increases the input/output differential voltage from 2.0V to approximately 4.5V. For an output current less than 5.0A, the R2/R1 ratio can be set lower than 4:1. Therefore, a less expensive PNP transistor may be used.

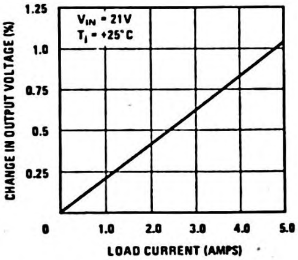


FIGURE 9. Load Regulation

4. 5.0V, 5.0A VOLTAGE REGULATOR FOR TTL

The high current 5.0V regulator for TTL shown in Figure 10 uses a relatively inexpensive NPN pass transistor with a lower power PNP device to replace the single, higher cost, power PNP shown in Figure 6. This circuit provides a 5.0V output at up to 5.0A of load current with a typical load regulation of 1.8% from no load to full load. The peak instantaneous output current observed was 10.4A at a 25°C junction temperature (pulsed load with a 1.0 ms ON and a 200 ms OFF period) and 8.4A for a continuous short circuit. The typical line regulation is 0.02% of input voltage change (I_{OUT} = 0).

One can easily add an overload indicator using the National's new NSL5027 LED. This is shown with dotted lines in Figure 10. With this configuration R2 is not only a current sharing resistor but also an overload sensor. R5 will determine the current through the LED; the diode D2 has been added to match the drop across D1. Once the load current exceeds 5.0A (1.0A through the LM340 assuming perfect current sharing and V_{D1} = V_{D2}) Q3 turns ON and the overload indicator lights up.

Example:

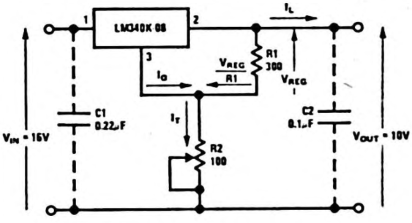
$I_{OVERLOAD}$ = 5.0A

I_{LED} = 40 mA (light intensity of 16 mcd)

$$V_{LED} = 1.75,\ R5 \simeq \frac{V_{IN} - 2.65}{I_{LED}} \qquad (4\text{-}1)$$

5. ADJUSTABLE OUTPUT VOLTAGE REGULATOR FOR INTERMEDIATE OUTPUT VOLTAGES

The addition of two resistors to an LM340 circuit allows a non-standard output voltage while maintaining the limiting features built into IC. The example shown in Figure 11 provides a 10V output using an LM340K-08 by raising the reference (pin number 3) of the regulator by 2.0V.

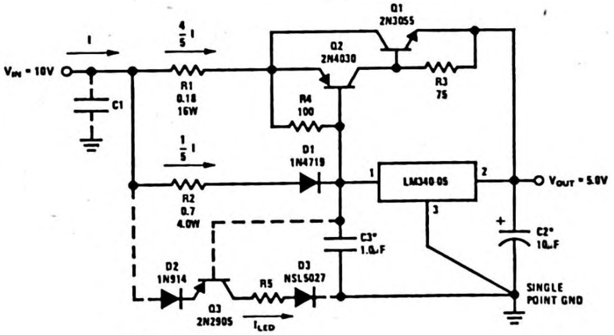


LM340K-08
1
2
3
I_L
R1
300
$\frac{V_{REG}}{R1}$
I_Q
V_{REG}
I_T
C1
0.22μF
C2
0.1μF
R2
100
V_{IN} = 16V
V_{OUT} = 10V

FIGURE 11. 10V Regulator

The 2.0V pedestal results from the sum of regulator quiescent current I_Q and a current equal to V_{REG}/R1, flowing through potenteniometer R2 to ground. R2 is made adjustable to compensate for differences in I_Q and V_{REG} output. The circuit is practical because the change in I_Q due to line voltage and load current changes is quite small.

The line regulation for the boosted regulator is the sum of the LM340 line regulation, its effects on the current through R2, and the effects of



V_{IN} = 10V
I
$\frac{4}{5}$ I
$\frac{1}{5}$ I
C1
R1
0.18
16W
R2
0.7
4.0W
R4
100
R3
75
Q1
2N3055
Q2
2N4030
D1
1N4719
LM340-05
1
2
3
V_{OUT} = 5.0V
C3*
1.0μF
C2*
10μF
+
D2
1N914
Q3
2N2905
R5
D3
NSL5027
I_{LED}
SINGLE POINT GND

*Solid tantalum.

FIGURE 10. 5.0V, 5.0A Regulator for TTL (with short circuit, thermal shutdown protection, and overload indicator)

ΔI_Q in response to input voltage changes. The change in output voltage is:

$$\Delta V_{OUT} = (L_r/V)\,\Delta V_{IN} + \frac{(L_r/V)\,\Delta V_{IN}\,R2}{R1} + (Q_{CC}/V)\,\Delta V_{IN}\,R2 \tag{5-1}$$

giving a total line regulation of:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = (L_r/V)\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/V)\,R2 \tag{5-2}$$

The LM340-08 data sheet lists $\Delta V_{OUT} < 160$ mV and $\Delta I_Q < 1.0$ mA for $\Delta V_{IN} = 14.5$V at $I_{OUT} = 500$ mA. This is:

$$L_r/V = \frac{160\text{ mV}}{14.5\text{V}} = 11\text{ mV/V} \tag{5-3}$$

$$Q_{CC}/V = \frac{1.0\text{ mA}}{14.5\text{V}} = 60\mu\text{A/V} \tag{5-4}$$

The worst case at line regulation for the circuit of Figure 12 calculated by equation 5-2, $I_{OUT} = 500$ mA and $R2 = 61\Omega$ is:

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 11\text{ mV/V}\left(1 + \frac{61\Omega}{300\Omega}\right) + (69\mu\text{A/V})\,61\Omega \tag{5-5}$$

$$\frac{\Delta V_{OUT}}{1.0\text{V}} = 13.2\text{ mV/V} + 4.2\text{ mV/V} = 17.4\text{ mV/V} \tag{5-6}$$

This represents a worst case line regulation value of 0.17%/V.

The load regulation is the sum of the LM340 voltage regulation, its effect on the current through R2, and the effect of ΔI_Q in response to changes in load current. Using the following definitions and the notation shown on Figure 11 ΔV_{OUT} is:

Z_{OUT} = Regulator output impedance: the change in output voltage per amp of load current change.

Z_{340} = LM340 output impedance

Q_{CC}/A = Quiescent current change per amp of load current change

$$\Delta V_{OUT} = (Z_{340})\,\Delta I_L + \frac{(Z_{340})}{R1}\,\Delta I_L\,R2 + (Q_{CC}/A)\,\Delta I_L\,R2 \tag{5-7}$$

and the total output impedance is:

$$Z_{OUT} = \frac{\Delta V_{OUT}}{\Delta I_L} = Z_{340}\left(1 + \frac{R2}{R1}\right) + (Q_{CC}/A)\,R2 \tag{5-8}$$

The LM340-08 data sheet gives a maximum load regulation $L_r = 160$ mV and $\Delta I_Q = 0.5$ mA for a 1.5A load change.

$$Z_{340} = \frac{160\text{ mV}}{1.5\text{A}} = 0.107\Omega \tag{5-9}$$

$$Q_{CC}/A = \frac{0.5\text{ mA}}{1.5\text{A}} = 333\mu\text{A/A} \tag{5-10}$$

This gives a worst case dc output impedance (ac output impedance being a function of C2) for the 10V regulator using equation 5-8 of:

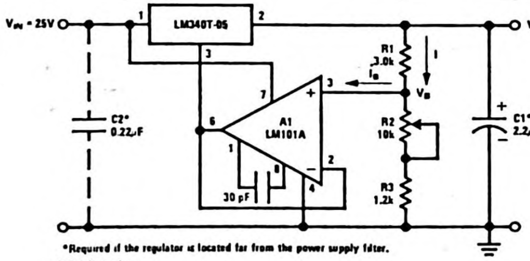
$$Z_{OUT} = 0.107\Omega\left(1 + \frac{61\Omega}{300\Omega}\right) + (333\mu\text{A/A})\,61\Omega \tag{5-11}$$

$$Z_{OUT} = 0.12\Omega + 0.020\Omega = 0.14\Omega$$

or a worst case change of approximately 1.5% for a 1.0A load change. Typical measured values are about 0.56% or one-third of the worst case value.

6. VARIABLE OUTPUT REGULATOR

In Figure 12 the ground terminal of the regulator is "lifted" by an amount equal to the voltage applied to the non-inverting input of the operational amplifier LM101A. The output voltage of the



*Required if the regulator is located far from the power supply filter.

**Solid tantalum.

FIGURE 12. Variable Output Regulator

regulator is therefore raised to a level set by the value of the resistive divider R1, R2, R3 and limited by the input voltage. With the resistor values shown in Figure 12, the output voltage is variable from 7.0V to 23V and the maximum output current (pulsed load) varies from 1.2A to 2.0A (T_j = 25°C) as shown in Figure 13.

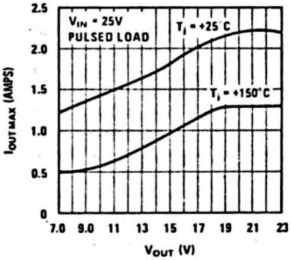


FIGURE 13. Maximum Output Current

Since the LM101A is operated with a single supply (the negative supply pin is grounded). The common mode voltage V_B must be at least at a 2.0 V_{BE} + V_{SAT} above ground. R3 has been added to insure this when R2 = 0. Furthermore the bias current I_B of the operational amplifier should be negligible compared to the current flowing through the resistive divider.

Example:

V_{IN} = 25V

V_{OUTMIN} = 5 + V_B, (R2 = 0),
V_B = R3 (I − I_B) = 2.0V
R1 = 2.5 R3

$V_{OUT\,MAX}$ = V_{IN} − dropout volt.
(R2 = $R2_{MAX}$)
$R2_{MAX}$ = 3.3 R1

So setting R3, the values of R1 and R2 can be determined.

If the LM324 is used instead of the LM101A, R3 can be omitted since its common mode voltage range includes the ground, and then the output will be adjustable from 5 to a certain upper value defined by the parameters of the system.

The circuit exhibits the short-circuit protection and thermal shutdown properties of the LM340 over the full output range.

The load regulation can be predicted as:

$$\Delta V_{OUT} = \frac{R1 + R2 + R3}{R1} \Delta V_{340} \qquad (6\text{-}1)$$

where ΔV_{340} is the load regulation of the device given in the data sheet. To insure that the regulator will start up under full load a reverse biased small signal germanium diode, 1N91, can be added between pins 2 and 3.

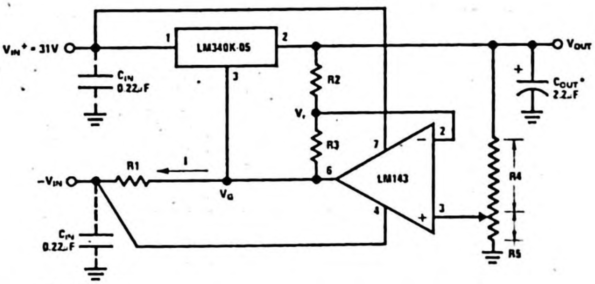
7. VARIABLE OUTPUT REGULATOR
0.5V − 29V

When a negative supply is available an approach equivalent to that outlined in section 6 may be used to lower the minimum output voltage of the regulator below the nominal voltage that of the LM340 regulator device. In Figure 14 the voltage V_G at the ground pin of the regulator is determined by the drop across R1 and the gain of the amplifier. The current I may be determined by the following relation:

$$I = \frac{V_{340}}{R1} \frac{R2\,R5 - R3\,R4}{R4\,(R2 + R3)} + \frac{V_{IN}^-}{R1} \qquad (7\text{-}1)$$

or if R2 + R3 = R4 + R5 = R

$$I = \frac{V_{340}\,R2}{R1\,R4} + \frac{1}{R1} (V_{IN}^- - V_{340}) \qquad (7\text{-}2)$$



*Solid tantalum.

FIGURE 14. Variable Output Voltage 0.5V − 30V

considering that the output is given by:

$$V_{OUT} = V_G + V_{340} \tag{7-3}$$

and

$$V_G = R1\,I - V_{IN}^{-} \tag{7-4}$$

combining 7-2, 7-3, 7-4 an expression for the output voltage is:

$$V_{OUT} = V_{340}\,\frac{R2}{R4} \tag{7-5}$$

Notice that the output voltage is inversely proportional to R4 so the output voltage may be adjusted very accurately for low values. A minimum output of 0.5V has been set. This implies that

$$\frac{R2}{R4} = 0.1 \quad \frac{R3}{R4} = 0.9 \quad \frac{R3}{R2} = 9 \tag{7-6}$$

An absolute zero output voltage will require R4 = ∞ or R2 = 0, neither being practical in this circuit. The maximum output voltage as shown in Figure 14 is 30V if the high voltage operational amplifier LM143 is used. If only low values of V_{OUT} are sought, then an LM101 may be used. R1 can be computed from:

$$R1 = \frac{V_{IN}^{-}}{I_{Q\,340}} \tag{7-7}$$

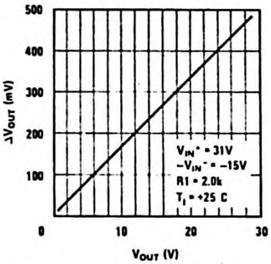


FIGURE 15. Typical Load Regulation for a 0.5V – 30V Regulator (ΔI_{OUT} = 1.0A)

Figure 15 illustrates the load regulation as a function of the output voltage.

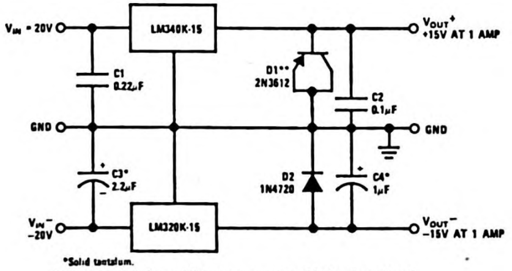
8. DUAL POWER SUPPLY

The plus and minus regulators shown in Figure 16 will exhibit line and load regulations consistant with their specifications as individual regulators. If fact, operation will be entirely normal until the problem of common loads occurs. A 30Ω load from the +15V output to the −15V output (representing a 0.5A starting load for the LM340K-15 if the LM320K-15 is already started) would allow start up of the LM340 in most cases. To insure LM340 startup over the full temperature range into a worst case 1.0A current sink load the germanium power "diode" D1 has been added to the circuit. Since the forward voltage drop of the germanium diode D1 is less than that of the silicon substrate diode of the LM340 the external diode will take any fault current and allow the LM340 to start up even into a negative voltage load. D1 and silicon diode D2 also protect the regulator outputs from inadvertant shorts between outputs and to ground. For shorts between outputs the voltage difference between either input and the opposite regulator output should not exceed the maximum rating of the device.

The example shown in Figure 16 is a symmetrical ±15V supply for linear circuits. The same principle applies to non-symmetrical supplies such as a +5.0V and −12V regulator for applications such as registers.

9. TRACKING DUAL REGULATORS

In Figure 17, a fraction of the negative output voltage "lifts" the ground pins of the negative LM320K-15 voltage regulator and the LM340K-15 through a voltage follower and an inverter respectively. The dual operational amplifier LM1558 is used for this application and since its supply voltage may go as high as ±22V the regulator outputs may be set between 5.0V and 20V. Because of the tighter output tolerance and the better drift of the LM320, the positive regulator

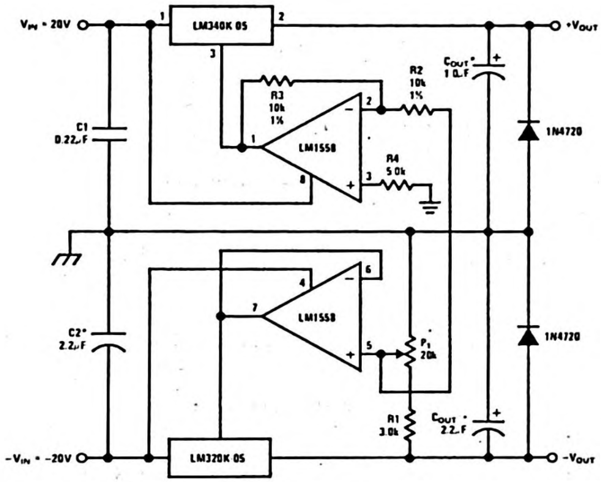


*Solid tantalum.

**Germanium diode (using a PNP germanium transistor with the collector shorted to the emitter).

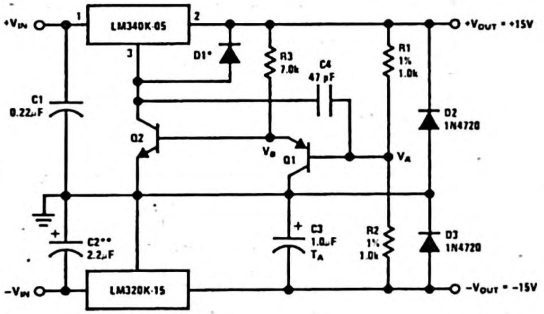
Note: C1 and C2 required if regulators are located far from power supply filter.

FIGURE 16. Dual Power Supply


V_IN = 20V
1
LM340K 05
2
+V_OUT
3
C_OUT*
1.0μF
R2
10k
1%
R3
10k
1%
C1
0.22μF
1
LM1558
R4
5.0k
8
3
1N4720
6
4
7
LM1558
C2*
2.2μF
5
P1
20k
1N4720
R1
3.0k
C_OUT*
2.2μF
−V_IN = −20V
LM320K 05
−V_OUT

*Solid tantalum.

FIGURE 17. Tracking Dual Supply ±5.0V — ±18V


+V_IN
1
LM340K-05
2
+V_OUT = +15V
3
D1*
R3
7.0k
C4
47 pF
R1
1%
1.0k
C1
0.22μF
D2
1N4720
Q2
V_B
Q1
V_A
C2**
2.2μF
C3
1.0μF
T_A
R2
1%
1.0k
D3
1N4720
−V_IN
LM320K-15
−V_OUT = −15V

*Germanium diode.
**Solid tantalum.

FIGURE 18. Tracking Dual Supply ±15V

is made to track the negative. The best tracking action is achieved by matching the gain of both operational amplifiers, that is, the resistors R2 and R3 must be matched as closely as possible.

Indeed, with R2 and R3 matched to better than 1%, the LM340 tracks the LM320 within 40 – 50 mV over the entire output range. The typical load regulation at V_{OUT} = ±15V for the positive regulator is 40 mV from a 0 to 1.0A pulsed load and 80 mV for the negative.

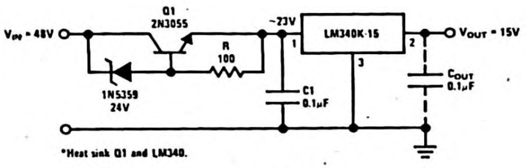
Figure 18 illustrates ±15V tracking regulator, where again the positive regulator tracks the negative. Under steady state conditions V_A is at a virtual ground and V_B at a V_{BE} above ground. Q2 then conducts the quiescent current of the LM340. If $-V_{OUT}$ becomes more negative the collector base junction of Q1 is forward biased thus lowering V_B and raising the collector voltage of Q2. As a result $+V_{OUT}$ rises and the voltage V_A again reaches ground potential.

Assuming Q1 and Q2 to be perfectly matched, the tracking action remains unchanged over the full operating temperature range.

With R1 and R2 matched to 1%, the positive regulator tracks the negative within 100 mV (less than 1%). The capacitor C4 has been added to improve stability. Typical load regulations for the positive and negative sides from a 0 to 1.0A pulsed load (t_{ON} = 1.0 ms, t_{OFF} = 200 ms) are 10 mV and 45 mV respectively.

10. HIGH INPUT VOLTAGE

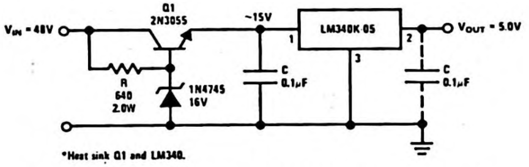
The input voltage of the LM340 must be kept within the limits specified in the data sheet. If



Q1
2N3055
V_{IN} = 48V
~23V
LM340K-15
V_{OUT} = 15V
R
100
1
2
3
1N5359
24V
C1
0.1µF
C_{OUT}
0.1µF

*Heat sink Q1 and LM340.

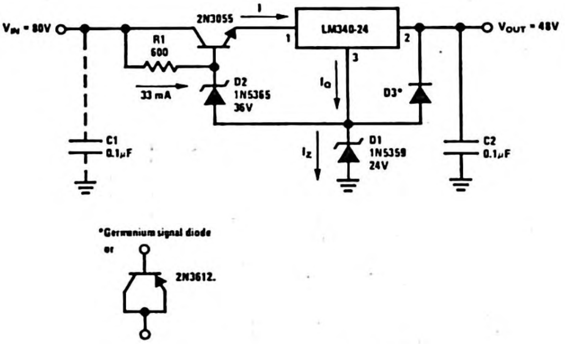
FIGURE 19. High Input Voltage



Q1
2N3055
V_{IN} = 48V
~15V
LM340K-05
V_{OUT} = 5.0V
R
640
2.0W
1N4745
16V
C
0.1µF
C
0.1µF
1
2
3

*Heat sink Q1 and LM340.

FIGURE 20. High Input Voltage



2N3055
I
V_{IN} = 80V
LM340-24
V_{OUT} = 48V
R1
600
1
2
3
33 mA
D2
1N5365
36V
I_Q
D3*
C1
0.1µF
I_Z
D1
1N5359
24V
C2
0.1µF
2N3612.

*Germanium signal diode or

FIGURE 21. High Voltage Regulator

the device is operated above the absolute maximum input voltage rating, two failure modes may occur. With the output shorted to ground, the series pass transistor Q16 (see Figure 4) will go to avalanche breakdown; or, even with the output not grounded, the transistor Q1 may fail since it is operated with a collector-emitter voltage approximately 4.0V below the input.

If the only available supply runs at a voltage higher than the maximum specified, one of the simplest ways to protect the regulator is to connect a zener diode in series with the input of the device to level shift the input voltage. The drawback to this approach is obvious. The zener must dissipate (V_{SUPPLY} − V_{INMAX} LM340). (I_{OUTMAX}) which may be several watts. Another way to overcome the over voltage problem is illustrated in Figure 19 where an inexpensive, NPN-zener-resistor, combination may be considered as an equivalent to the power zener. The typical load regulation of this circuit is 40 mV from 0 to 1.0A pulsed load (T_j = 25°C) and the line regulation is 2.0 mV for 1.0V variation in the input voltage (I_{OUT} = 0). A similar alternate approach is shown in Figure 20.

With an optional output capacitor the measured noise of the circuit was 700µVp-p.

11. HIGH VOLTAGE REGULATOR

In previous sections the principle of "lifting the ground terminal" of the LM340, using a resistor divider or an operational amplifier, has been illustrated. One can also raise the output voltage by using a zener diode connected to the ground pin as illustrated in the Figure 21 to obtain an output level increased by the breakdown voltage of the zener. Since the input voltage of the regulator has been allowed to go as high as 80V a level shifting transistor-zener (D2)—resistor combination has been added to keep the voltage across the LM340 under permissible values. The disadvantage of the system is the increased output noise and output voltage drift due to the added diodes.

Indeed it can be seen that, from no load to full load conditions, the ΔI_Z will be approximately the current through R1 (≃ 35 mA) and therefore the degraded regulation caused by D1 will be V_Z (at 35 mA + I_Q) − V_Z (at I_Q).

The measured load regulation was 60 mV for ΔI_{OUT} of 5.0 mA to 1.0A (pulsed load), and the line regulation is 0.01%/V of input voltage change (I_{OUT} = 500 mA) and the typical output noise 2.0 mVp-p (C2 = 0.1μF). The value of R1 is calculated as:

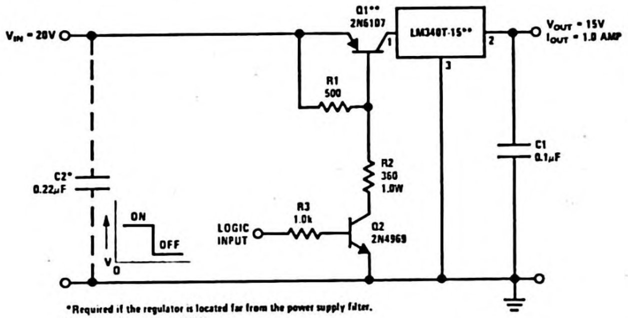
$$R1 \simeq \beta \left[\frac{V_{IN} - (V_{Z1} + V_{Z2})}{I \text{ full load}} \right] \qquad (11\text{-}1)$$

12. ELECTRONIC SHUTDOWN

Figure 22 shows a practical method of shutting down the LM340 under the control of a TTL or DTL logic gate. The pass transistor Q1 operates either as a saturated transistor or as an open switch. With the logic input high (2.4V specified minimum for TTL logic) transistor Q2 turns on and pulls 50 mA down through R2. This provides sufficient base drive to maintain Q1 in saturation during the ON condition of the switch. When the logic input is low (0.4V specified maximum for TTL logic) Q2 is held off, as is Q1; and the switch is in the OFF condition. The observed turn-on time was 7.0μs for resistive loads from 15Ω to infinity and the turn-off time varied from approximately 3.0μs for a 15Ω load to 3.0 ms for a no-load condition. Turn-off time is controlled primarily by the time constant of R_{LOAD} and C1.

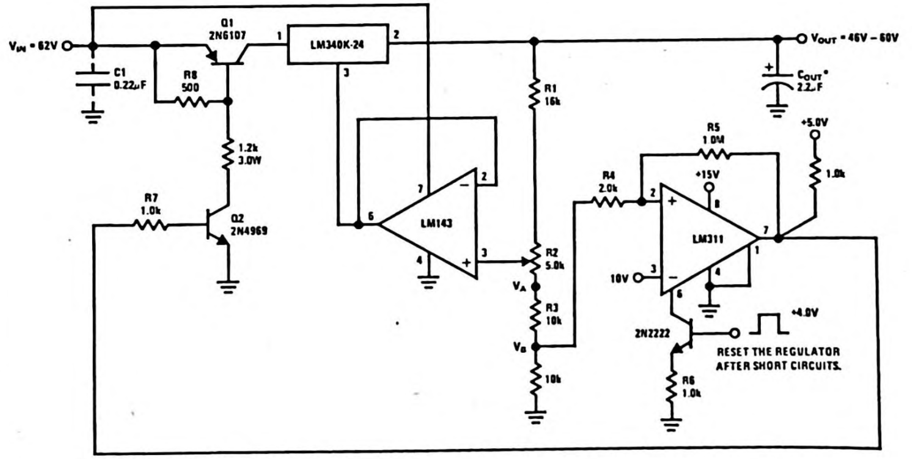
13. VARIABLE HIGH VOLTAGE REGULATOR WITH OVERVOLTAGE SHUTDOWN

A high voltage variable-output regulator may be constructed using the LM340 after the idea illustrated in section 7 and drawn in Figure 23. The principal inconvenience is that the voltage across the regulator must be limited to maximum rating of the device, the higher the applied input voltage the higher must be lifted the ground pin of the LM340. Therefore the range of the variable


Q1**
2N6107
LM340T-15**
V_{IN} = 20V
V_{OUT} = 15V
I_{OUT} = 1.0 AMP
1
2
3
R1
500
C1
0.1μF
R2
360
1.0W
C2*
0.22μF
ON
OFF
V_O
R3
1.0k
LOGIC INPUT
Q2
2N4969

*Required if the regulator is located far from the power supply filter.
**Head sink Q1 and the LM340.

FIGURE 22. Electronic Shutdown Circuit


V_{IN} = 62V
Q1
2N6107
LM340K-24
1
2
3
V_{OUT} = 46V – 60V
C1
0.22μF
R8
500
R1
16k
C_{OUT}*
2.2μF
1.2k
3.0W
R7
1.0k
Q2
2N4969
LM143
7
2
6
4
3
R2
5.0k
V_A
R3
10k
V_B
10k
R5
1.0M
+5.0V
1.0k
R4
2.0k
+15V
LM311
8
7
1
10V
4
6
+4.0V
2N2222
RESET THE REGULATOR AFTER SHORT CIRCUITS.
R6
1.0k

*Solid tantalum.

FIGURE 23. Variable High Voltage Regulator with Shortcircuit and Overvoltage Protection

output is limited by the supply voltage limit of the operational amplifier and the maximum voltage allowed across the regulator. An estimation of this range is given by:

$$V_{OUT\,MAX} - V_{OUT\,MIN} = V_{SUPPLY\,MAX\,340} - V_{NOMINAL\,340} - 2.0V \quad (13\text{-}1)$$

Examples:

$$\text{LM340-24: } V_{OUT\,MAX} - V_{OUT\,MIN} = 40 - 24 - 2 = 14V$$

Figure 23 illustrates the above considerations. Even though the LM340 is by itself short circuit protected, when the output drops, also V_A drops and the voltage difference across the device increases. If it exceeds 40V the pass transistor internal to the regulator will breakdown, as explained in section 11. To remedy this, an over-voltage shutdown is included in the circuit. When the output drops the comparator switches low, pulls down the base of Q2 thus opening the switch Q1, and shutting down the LM340. Once the short circuit has been removed the LM311 must be activated through the strobe to switch high and close Q1, which will start the regulator again. The additional voltages required to operate the comparator may be taken from the 62V since the LM311 has a certain ripple rejection and the reference voltage (pin 3) may have a superimposed small ac signal. The typical load regulation can be be computed from equation 6-1.

BIBLIOGRAPHY

1. AN-42: *"IC Provides on Card Regulation for Logic Circuits."*
2. Carl T. Nelson: *"Power distribution and regulation can be simple, cheap and rugged."* EDN, February 20, 1973.

Noise Specs Confusing?

National Semiconductor
Application Note 104
Jim Sherwin
May 1974

It's really all very simple—once you understand it. Then, here's the inside story on noise for those of us who haven't been designing low noise amplifiers for ten years.

You hear all sorts of terms like signal-to-noise ratio, noise figure, noise factor, noise voltage, noise current, noise power, noise spectral density, noise per root Hertz, broadband noise, spot noise, shot noise, flicker noise, excess noise, I/F noise, fluctuation noise, thermal noise, white noise, pink noise, popcorn noise, bipolar spike noise, low noise, no noise, and loud noise. No wonder not everyone understands noise specifications.

In a case like noise, it is probably best to sort it all out from the beginning. So, in the beginning, there was noise; and then there was signal. The whole idea is to have the noise very small compared to the signal; or, conversely, we desire a high signal-to-noise ratio S/N. Now it happens that S/N is related to noise figure NF, noise factor F, noise power, noise voltage $\bar{e}_n$, and noise current $\bar{i}_n$. To simplify matters, it also happens that any noisy channel or amplifier can be completely specified for noise in terms of two noise generators $\bar{e}_n$ and $\bar{i}_n$ as shown in Figure 1.

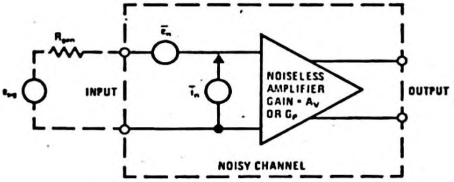


FIGURE 1. Noise Characterization of Amplifier

All we really need to understand are NF, $\bar{e}_n$, and $\bar{i}_n$. So here is a rundown on these three.

NOISE VOLTAGE, $\bar{e}_n$, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of the noiseless amplifier if the input terminals were shorted. It is expressed in nanovolts per root Hertz nV/$\sqrt{Hz}$ at a specified frequency, or in microvolts in a given frequency band. It is determined or measured by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$ if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in Figure 2. This increase is 1/f NOISE.

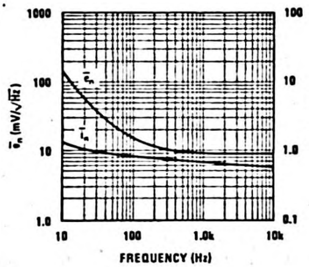


FIGURE 2. Noise Voltage and Current for an Op Amp

NOISE CURRENT, $\bar{i}_n$, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which occurs apparently at the input of the noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz pA/$\sqrt{Hz}$ at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is $\bar{i}_n \times R_{in}$ (or X_{cin}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the input, there is only $\bar{e}_n$ and $\bar{i}_n X_{cin}$. The $\bar{i}_n$ is measured with a bandpass filter and converted to pA/$\sqrt{Hz}$ if appropriate; typically it increases at lower frequencies for op amps and bipolar transistors, but increases at higher frequencies for field-effect transistors.

NOISE FIGURE, NF is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \log \frac{(S/N)_{in}}{(S/N)_{out}} \qquad (1)$$

where: S and N are power or $(\text{voltage})^2$ levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{gen} and any X_{gen} as well as frequency must be known to properly express NF in meaningful terms. This is because the amplifier $\bar{i}_n \times Z_{gen}$ as well as R_{gen} itself produces input noise. The signal source in Figure 1 contains some noise. However e_{sig} is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance R_{gen}. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen from Equation 2 that the $\overline{e_n^2}$ has the units V^2/Hz and that $(\bar{e}_n)$ has the units $V/\sqrt{Hz}$

$$\overline{e_R^2} = 4kTRB \qquad (2)$$

where: T is temperature in °K
R is resistor value in ohms
B is bandwidth in Hz
k is Boltzman's constant

Relation Between $\bar{e}_n$, $\bar{i}_n$, μF

Now we can examine the relationship between $\bar{e}_n$ and $\bar{i}_n$ at the amplifier input. When the signal source is connected, the $\bar{e}_n$ appears in series with the e_{sig} and $\bar{e}_R$. The $\bar{i}_n$ flows through R_{gen} thus producing another noise voltage of value $\bar{i}_n \times R_{gen}$. This noise voltage is clearly dependent upon the value of R_{gen}. All of these noise voltages add at the input in rms fashion; that is, as the square root of the sum of the squares. Thus, neglecting possible correlation between $\bar{e}_n$ and $\bar{i}_n$, the total input noise is

$$\overline{e_N^2} = \overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2 \qquad (3)$$

Further examination of the NF equation shows the relationship of $\bar{e}_N$, $\bar{i}_n$, and NF.

$$NF = 10 \log \frac{S_{in} \times N_{out}}{S_{out} \times N_{in}}$$

$$= 10 \log \frac{S_{in}\ G_p\ \overline{e_N^2}}{S_{in}\ G_p\ \overline{e_R^2}}$$

where: G_p = power gain

$$= 10 \log \frac{\overline{e_N^2}}{\overline{e_R^2}}$$

$$= 10 \log \frac{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}$$

$$NF = 10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2}\ R_{gen}^2}{\overline{e_R^2}}\right) \qquad (4)$$

Thus, for small R_{gen}, noise voltage dominates; and for large R_{gen}, noise current becomes important. A clear advantage accrues to FET input amplifiers, especially at high values of R_{gen}, as the FET has essentially zero $\bar{i}_n$. Note, that for an NF value to have meaning, it must be accompanied by a value for R_{gen} as well as frequency.

Calculating Total Noise, $\bar{e}_N$

We can generate a plot of $\bar{e}_N$ for various values of R_{gen} if noise voltage and current are known vs frequency. Such a graph is shown in Figure 3 drawn from Figure 2. To make this plot, the thermal noise $\bar{e}_R$ of the input resistance must be calculated from Equation 2 or taken from the graph of Figure 4. Remember that each term in Equation 3 must be squared prior to addition, so the data from Figure 4 and from Figure 2 is squared. A sample of this calculation follows.

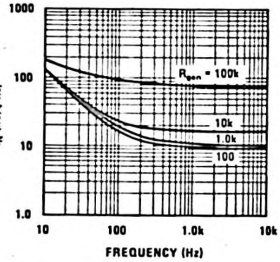


FIGURE 3. Total Noise for the Op Amp of Figure 2.

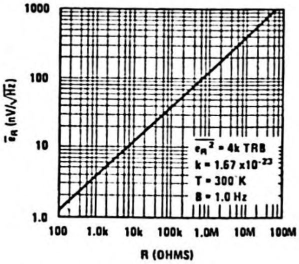


FIGURE 4. Thermal Noise of Resistor

Example 1: Determine total equivalent input noise per unit bandwidth for an amplifier operating at 1 kHz from a source resistance of 10 kohms. Use the data from Figures 2 and 4.

1. Read $\bar{e}_R$ from Figure 4 at 10 kohm; the value is 12 nV/√Hz.
2. Read $\bar{e}_n$ from Figure 2 at 1 kHz; the value is 9.5 nV/√Hz.
3. Read $\bar{i}_n$ from Figure 2 at 1 kHz; the value is 0.68 pA/√Hz. Multiply by 10 kohm to obtain 6.8 nV/√Hz.

4. Square each term individually, and enter into Equation 3.

$$\bar{e}_N = \sqrt{\overline{e_n^2} + \overline{e_R^2} + \overline{i_n^2}\, R_{gen}^2}$$

$$= \sqrt{9.5^2 + 12^2 + 6.8^2} = \sqrt{279}$$

$$\bar{e}_N = 16.7\ \text{nV}/\sqrt{\text{Hz}}$$

This is total rms noise at the input in one Hertz bandwidth at 1 kHz. If total noise in a given bandwidth is desired, one must integrate the noise over a bandwidth as specified. This is most easily done in a noise measurement set-up, but may be approximated as follows.

1. If the frequency range of interest is in the flat band; i.e., between 1 kHz and 10 kHz in Figure 2, it is simply a matter of multiplying $\bar{e}_N$ by the square root of the bandwidth. Then, in the 1 kHz-10 kHz band, total noise is

$$\bar{e}_N = 16.7\sqrt{9000}$$

$$= 1.59\mu\text{V}$$

2. If the frequency band of interest is not in the flat band of Figure 2, one must break the band into sections, calculating average noise in each section, squaring, multiplying by section bandwidth, summing all sections, and finally taking square root of the sum as follows:

$$\bar{e}_N = \sqrt{\overline{e_R^2}B + \sum_{1}^{i} (\overline{e_n^2} + \overline{i_n^2} R_{gen}^2)_i\, B_i} \qquad (5)$$

where: i is the total number of sub-blocks.

For most purposes a sub-block may be one or two octaves. Example 2 details such a calculation.

Example 2: Determine the rms noise level in the frequency band 50 Hz to 10 kHz for the amplifier of Figure 2 operating from R_{gen} = 2k.

1. Read $\bar{e}_R$ from Figure 4 at 2k, square the value, and multiply by the entire bandwidth. Easiest way is to construct a table as shown below.
2. Read the median value of $\bar{e}_n$ in a relatively small frequency band, say 50 Hz-100 Hz, from Figure 2, square it and enter into the table.
3. Read the median value of $\bar{i}_n$ in the 50 Hz-100 Hz band from Figure 2, multiply by R_{gen} = 2k, square the result and enter in the table.
4. Sum the squared results from steps 2 and 3, multiply the sum by Δf = 100–50 = 50 Hz, and enter in the table.
5. Repeat steps 2-4 for band sections of 100 Hz-300 Hz, 300 Hz-1000 Hz and 1 kHz-10 kHz. Enter results in the table.
6. Sum all entires in the last column, and finally take the square root of this sum for the total rms noise in the 50 Hz-10,000 Hz band.
7. Total $\bar{e}_n$ is 1.62μV in the 50 Hz-10,000 Hz band.

Calculating S/N and NF

Signal-to-noise ratio can be easily calculated from known signal levels once total rms noise in the band is determined. Example 3 shows this rather simple calculation from Equation 6 for the data of Example 2.

$$S/N = 20 \log \frac{e_{sig}}{\bar{e}_N} \qquad (6)$$

Example 3: Determine S/N for an rms e_{sig} = 4 mV at the input to the amplifier operated in Example 2.

1. RMS signal is e_{sig} = 4 mV
2. RMS noise from Example 2 is 1.62μV
3. Calculate S/N from Equation 6

$$S/N = 20 \log \frac{4\ \text{mV}}{1.62\mu\text{V}}$$

$$= 20 \log (2.47 \times 10^3)$$

$$= 20 (\log 10^3 + \log 2.47)$$

$$= 20 (3 + 0.393)$$

$$S/N = 68\ \text{dB}$$

TABLE I. Noise Calculations for Example 2

B (Hz)	Δf (Hz)	$\bar{e}_n^2$ (nV/Hz)	+	$\bar{i}_n^2 R_{gen}^2$			SUM x Δf	=	(nV^2)
50-100	50	$(20)^2 = 400$		$(8.7 \times 2.0k)^2$	=	302	702* x 50		35,000
100-300	200	$(13)^2 = 169$		$(8 \times 2.0k)^2$	=	256	425 x 200		85,000
300-1000	700	$(10)^2 = 100$		$(7 \times 2.0k)^2$	=	196	296 x 700		207,000
1.0k-10k	9000	$(9)^2 = 81$		$(6 \times 2.0k)^2$	=	144	225 x 9000		2,020,000
50-10,000	9950	$\bar{e}_R^2 = (5.3)^2 = 28$					28 x 9950		279,000
Total $\bar{e}_N = \sqrt{2{,}626{,}000} = 1620\ \text{nV} = 1.62\mu\text{V}$									

*The units are as follows: $(20\ \text{nV}/\sqrt{\text{Hz}})^2 = 400\ (\text{nV})^2/\text{Hz}$

$(8.7\ \text{pA}/\sqrt{\text{Hz}} \times 2.0\text{kohms})^2 = (17.4\ \text{nA}/\sqrt{\text{Hz}})^2 = 302\ (\text{nV})^2/\text{Hz}$

Sum $= 702\ (\text{nV})^2/\text{Hz} \times 50\ \text{Hz} = 35{,}000\ (\text{nV})^2$

It is also possible to plot NF vs frequency at various R_{gen} for any given plot of $\bar{e}_n$ and $\bar{i}_n$. However there is no specific all-purpose conversion plot relating NF, $\bar{e}_n$, $\bar{i}_n$, R_{gen} and f. If either $\bar{e}_n$ or $\bar{i}_n$ is neglected, a reference chart can be constructed. Figure 5 is such a plot when only $\bar{e}_n$ is considered. It is useful for most op amps when R_{gen} is less than about 200 ohms and for FETs at any R_{gen} (because there is no significant $\bar{i}_n$ for FETs), however actual NF for op amps with $R_{gen} > 200$ ohms is higher than indicated on the chart.

The graph of Figure 5 can be used to find spot NF if $\bar{e}_n$ and R_{gen} are known, or to find $\bar{e}_n$ if NF and R_{gen} are known. It can also be used to find max R_{gen} allowed for a given max NF when $\bar{e}_n$ is known. In any case, values are only valid if $\bar{i}_n$ is negligible and at the specific frequency of interest for NF and $\bar{e}_n$, and for 1 Hz bandwidth. If bandwidth increases, the plot is valid so long as $\bar{e}_n$ is multiplied by $\sqrt{B}$.

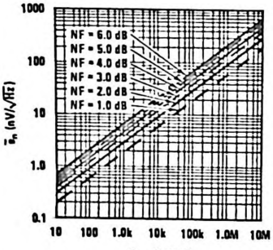


FIGURE 5. Spot NF vs R_{gen} when Considering *Only* $\bar{e}_n$ and $\bar{e}_R$ (not valid when $\bar{i}_n R_{gen}$ is significant)

The Noise Figure Myth

Noise figure is easy to calculate because the signal level need not be specified (note that e_{sig} drops out of Equation 4). Because NF is so easy to handle in calculations, many designers tend to lose sight of the fact that signal-to-noise ratio $(S/N)_{out}$ is what is important in the final analysis, be it an audio, video, or digital data system. One can, in fact, choose a high R_{gen} to reduce NF to near zero if $\bar{i}_n$ is very small. In this case $\bar{e}_R$ is the major source of noise, overshadowing $\bar{e}_n$ completely. The result is very low NF, but very low S/N as well because of very high noise. Don't be fooled into believing that low NF means low noise *per se!*

Another term is worth considering, that is optimum source resistance R_{OPT}. This is a value of R_{gen} which produces the lowest NF in a given system. It is calculated as

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n} \tag{7}$$

This has been arrived at by differentiating Equation 4 with respect to R_{gen} and equating it to zero (see Appendix). *Note that this does not mean lowest noise.*

For example, using Figure 2 to calculate R_{OPT} at say 600 Hz,

$$R_{OPT} = \frac{10\ \text{nV}}{0.7\ \text{pA}} = 14\ \text{kohms}$$

Then note in Figure 3, that $\bar{e}_N$ is in the neighborhood of 20 nV/$\sqrt{Hz}$ for R_{gen} of 14k. While $\bar{e}_N$ = 10 nV/$\sqrt{Hz}$ for R_{gen} = 0-100 ohms. STOP! Do not pass GO. Do not be fooled. Using $R_{gen} = R_{OPT}$ does not guarantee lowest noise UNLESS $e_{sig}^2 = kR_{gen}$ as in the case of transformer coupling. When $e_{sig}^2 > kR_{gen}$, as is the case where signal level is proportional to R_{gen} ($e_{sig} = kR_{gen}$), it makes sense to use the highest practical value of R_{gen}. When $e_{sig}^2 < kR_{gen}$, it makes sense to use a value of $R_{gen} < R_{OPT}$. These conclusions are verified in the Appendix.

This all means that it does not make sense to tamper with the R_{gen} of existing signal sources in an attempt to make $R_{gen} = R_{OPT}$. Especially, do not add series resistance to a source for this purpose. It does make sense to adjust R_{gen} in transformer coupled circuits by manipulating turns ratio or to design R_{gen} of a magnetic pick-up to operate with pre-amps where R_{OPT} is known. It does make sense to increase the design resistance of signal sources to match or exceed R_{OPT} so long as the signal voltage increases with R_{gen} in at least the ratio $e_{sig}^2 \propto R_{gen}$. It does not necessarily make sense to select an amplifier with R_{OPT} to match R_{gen} because one amplifier operating at $R_{gen} = R_{OPT}$ may produce lower S/N than another (quieter) amplifier operating with $R_{gen} \neq R_{OPT}$.

With some amplifiers it is possible to adjust R_{OPT} over a limited range by adjusting the first stage operating current (the National LM121 and LM381 for example). With these, one might increase operating current, varying R_{OPT}, to find a condition of minimum S/N. Increasing input stage current decreases R_{OPT} as $\bar{e}_n$ is decreased and $\bar{i}_n$ is simultaneously increased.

Let us consider one additional case of a fairly complex nature just as a practical example which will point up some factors often overlooked.

Example 4: Determine the S/N *apparent to the ear* of the amplifier of Figure 2 operating over 50-12, 800 Hz when driven by a phonograph cartridge exhibiting $R_{gen} = 1350\Omega$, $L_{gen} = 0.5H$, and average e_{sig} = 4.0 mVrms. The cartridge is to be loaded by 47k as in Figure 6. This is equivalent to using a Shure V15, Type 3 for average level recorded music.

1. Choose sectional bandwidths of 1 octave each, these are listed in the following table.
2. Read $\bar{e}_n$ from Figure 2 as average for each octave and enter in the table.
3. Read $\bar{i}_n$ from Figure 2 as average for each octave and enter in the table.
4. Read $\bar{e}_R$ for the $R_{gen} = 1350\Omega$ from Figure 4 and enter in the table.

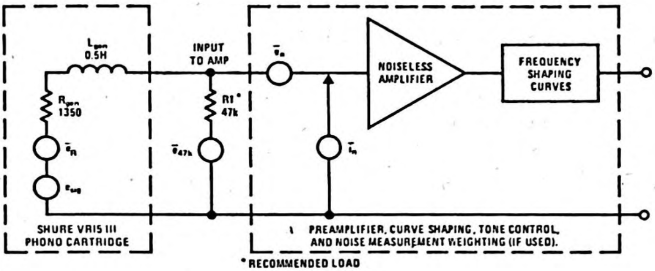

L_{gen}
0.5H
R_{gen}
1350
$\bar{e}_R$
e_{sig}
SHURE VRIS III
PHONO CARTRIDGE
INPUT
TO AMP
R1*
47k
$\bar{e}_{47k}$
$\bar{e}_n$
$\bar{i}_n$
NOISELESS
AMPLIFIER
FREQUENCY
SHAPING
CURVES
PREAMPLIFIER, CURVE SHAPING, TONE CONTROL,
AND NOISE MEASUREMENT WEIGHTING (IF USED).
*RECOMMENDED LOAD

FIGURE 6. Phono Preamp Noise Sources

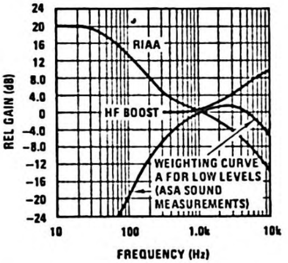


FIGURE 7. Relative Gain for RIAA, ASA Weighting A, and H-F Boost Curves

5. Determine the values of Z_{gen} at the midpoint of each octave and enter in the table.
6. Determine the amount of $\bar{e}_R$ which reaches the amplifier input; this is

$$\bar{e}_R \frac{R1}{R1 + Z_{gen}}$$

7. Read the noise contribution $\bar{e}_{47k}$ of R1 = 47k from Figure 4.
8. Determine the amount of $\bar{e}_{47K}$ which reaches the amplifier input; this is

$$\bar{e}_{47k} \frac{Z_{gen}}{R1 + Z_{gen}}$$

9. Determine the effective noise contributed by $\bar{i}_n$ flowing through the parallel combination of R1 and Z_{gen}. This is

$$\bar{i}_n \frac{Z_{gen} R1}{Z_{gen} + R1}$$

10. Square all noise voltage values resulting from steps 2, 6, 8 and 9; and sum the squares.
11. Determine the relative gain at the midpoint of each octave from the RIAA playback response curve of Figure 7.
12. Determine the relative gain at these same midpoints from the A weighted response curve of Figure 7 for sound level meters (this roughly accounts for variations in human hearing).
13. Assume a tone control high frequency boost of 10 dB at 10 kHz from Figure 7. Again determine relative response of octave midpoints.
14. Multiply all relative gain values of steps 11-13 and square the result.
15. Multiply the sum of the squared values from step 10 by the resultant relative gain of step 14 and by the bandwidth in each octave.
16. Sum all the values resultant from step 15, and find the square root of the sum. This is the total audible rms noise apparent in the band.
17. Divide e_{sig} = 4 mV by the total noise to find S/N = 69.5 dB.

Steps for Example

1	Frequency Band (Hz)	50-100	100-200	200-400	400-800	800-1600	1.6-3.2k	3.2-6.4k	6.4-12.8k
	Bandwidth, B (Hz)	50	100	200	400	800	1600	3200	6400
	Bandcenter, f (Hz)	75	150	300	600	1200	2400	4800	9600
5	Z_{gen} at f (ohms)	1355	1425	1665	2400	4220	8100	16k	32k
	Z_{gen} R1 (ohms)	1300	1360	1600	2270	3900	6900	11.9k	19k
	$Z_{gen}/(R1 + Z_{gen})$	0.028	0.030	0.034	0.485	0.082	0.145	0.255	0.400
	$R1/(R1 + Z_{gen})$	0.97	0.97	0.97	0.95	0.92	0.86	0.74	0.60
11	RIAA Gain, A_{RIAA}	5.6	3.1	2.0	1.4	1	0.7	0.45	0.316
12	Corr for Hearing, A_A	0.08	0.18	0.45	0.80	1	1.26	1	0.5
13	H-F Boost, A_{boost}	1	1	1	1	1.12	1.46	2.3	3.1
14	Product of Gains, A	0.45	0.55	0.9	1.12	1.12	1.28	1.03	0.49
	A^2	0.204	0.304	0.81	1.26	1.26	1.65	1.06	0.241
4	$\bar{e}_R$ $(nV/\sqrt{Hz})$	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
7	$\bar{e}_{47k}$ $(nV/\sqrt{Hz})$	29	29	29	29	29	29	29	29
3	$\bar{i}_n$ $(pA/\sqrt{Hz})$	0.85	0.80	0.77	0.72	0.65	0.62	0.60	0.60
2	$\bar{e}_n$ $(nV/\sqrt{Hz})$	19	14	11	10	9.5	9	9	9
9	$\bar{e}_1 = \bar{i}_n (Z_{gen} R1)$	1.1	1.09	1.23	1.63	2.55	4.3	7.1	11.4
6	$\bar{e}_2 = \bar{e}_R R1/(R1 + Z_{gen})$	4.35	4.35	4.35	4.25	4.15	3.86	3.33	2.7
8	$\bar{e}_3 = \bar{e}_{47k} Z_{gen}/(R1 + Z_{gen})$	0.81	0.87	0.98	1.4	2.4	4.2	7.4	11.6
10	$\overline{e_n^2}$	360	195	121	100	90	81	81	81
	$\overline{e_1^2}$ (from $\bar{i}_n$)	1.21	1.2	1.5	2.65	6.5	18.5	50	150
	$\overline{e_2^2}$ (from $\bar{e}_R$)	19	19	19	18	17	15	11	7.2
	$\overline{e_3^2}$ (from $\bar{e}_{47k}$)	0.65	0.76	0.96	2	5.8	18	55	135
	$\Sigma \overline{e_n^2}$ (nV^2/Hz)	381	216	142	122	120	133	147	373
15	BA^2 (Hz)	10.2	30.4	162	504	1010	2640	3400	1550
	$BA^2 \Sigma \overline{e^2}$ (nV^2)	3880	6550	23000	61500	121000	350000	670000	580000

16 $\Sigma(\overline{e_{n_i}^2} + \overline{e_{1_i}^2} + \overline{e_{2_i}^2} + \overline{e_{3_i}^2}) B_i A_i^2 = 1{,}815{,}930\ nV^2$

$\bar{e}_N = \sqrt{\Sigma} = 1.35 \mu V$

17 $S/N = 20 \log (4.0\ mV/1.35 \mu V) = 69.5\ dB$

Note the significant contributions of $\bar{i}_n$ and the 47k resistor, especially at high frequencies. Note also that there will be a difference between calculated noise and that noise measured on broadband meters because of the A curve employed in the example. If it were not for the A curve attenuation at low frequencies, the $\bar{e}_n$ would add a very important contribution below 200 Hz. This would be due to the RIAA boost at low frequency. As it stands, 97% of the 1.35µV would occur in the 800-12.8 kHz band alone, principally because of the high frequency boost and the A measurement curve. If the measurement were made without either the high frequency boost or the A curve, the $\bar{e}_n$ would be 1.25µV. In this case, 76% of the total noise would arise in the 50 Hz-400 Hz band alone. If the A curve were used, but the high-frequency boost were deleted, $\bar{e}_n$ would be 0.91µV; and 94% would arise in the 800-12, 800 Hz band alone.

The three different methods of measuring would only produce a difference of +3.5 dB in overall S/N, however the prime sources of the largest part of the noise and the frequency character of the noise can vary greatly with the test or measurement conditions. It is, then, quite important to know the method of measurement in order to know which individual noise sources in Figure 6 must be reduced in order to significantly improve S/N.

CONCLUSIONS

The main points in selecting low noise preamplifiers are:

1. Don't pad the signal source; live with the existing R_{gen}.
2. Select on the basis of low values of $\bar{e}_n$ and especially $\bar{i}_n$ if R_{gen} is over about a thousand ohms.
3. Don't select on the basis of NF or R_{OPT} in most cases. NF specs are all right so long as you know precisely how to use them and so long as they are valid over the frequency band for the R_{gen} or Z_{gen} with which you must work.
4. Be sure to (root) sum all the noise sources $\bar{e}_n$, $\bar{i}_n$ and $\bar{e}_R$ in your system over appropriate bandwidth.
5. The higher frequencies are often the most important unless there is low frequency boost or high frequency attenuation in the system.
6. Don't forget the filtering effect of the human ear in audio systems. Know the eventual frequency emphasis or filtering to be employed.

APPENDIX I

Derivation of R_{OPT}:

$$NF = 10 \log \frac{\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\, R_{gen}^2}{\overline{e_R^2}}$$

$$10 \log \left(1 + \frac{\overline{e_n^2} + \overline{i_n^2}\; R_{gen}^2}{\overline{e_R^2}}\right)$$

$$\frac{\partial NF}{\partial R} = \frac{0.435}{(4kTRB)^2}\; \frac{4\,kTRB\,(2R\,\overline{i_n^2}) - (\overline{e_n^2} + \overline{i_n^2}\, R^2)4kTB}{1 + (\overline{e_n^2} + \overline{i_n^2}\, R^2)/4kTRB}$$

where: $R = R_{gen}$

Set this = 0, and

$$4kTRB(2R\overline{i_n^2}) = 4kTB(\overline{e_n^2} + \overline{i_n^2}\, R^2)$$

$$2\overline{i_n^2}\, R^2 = \overline{e_n^2} + \overline{i_n^2}\, R^2$$

$$\overline{i_n^2}\, R^2 = \overline{e_n^2}$$

$$R^2 = \overline{e_n^2} \,/\, \overline{i_n^2}$$

$$R_{OPT} = \frac{\bar{e}_n}{\bar{i}_n}$$

APPENDIX II

Selecting R_{gen} for highest S/N.

$$S/N = \frac{e_{sig}^{\;2}}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\, R^2)}$$

For S/N to increase with R,

$$\frac{\partial S/N}{\partial R} > 0$$

$$\frac{\partial S/N}{\partial R} = \frac{2e_{sig}(\partial e_{sig}/\partial R)\,(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\, R^2) - e_{sig}^{\;2}\,(4kT + 2\overline{i_n^2}R)}{B(\overline{e_R^2} + \overline{e_n^2} + \overline{i_n^2}\, R^2)^2}$$

APPENDIX II (Con't)

If we set >0, then

$$2\,(\partial\, e_{sig}/\partial\, R)\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\, R^2) > e_{sig}\,(4kT + 2\overline{i_n{}^2}\, R)$$

For $e_{sig} = k_1\sqrt{R}$, $\quad \partial e_{sig}/\partial R = \dfrac{k_1}{2\sqrt{R}}$

$$(2k_1/2\sqrt{R})\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\, R^2) > k_1\sqrt{R}\,(4kT + 2\overline{i_n{}^2}\, R)$$

$$\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\, R^2 > 4kTR + 2\overline{i_n{}^2}\, R^2$$

$$\overline{e_n{}^2} > \overline{i_n{}^2}\, R^2$$

$$R < \bar{e}_n/\bar{i}_n$$

Therefore S/N increases with R_{gen} so long as $R_{gen} \leq R_{OPT}$

For $e_{sig} = k_1 R$, $\partial e_{sig}/\partial R = k_1$

$$2k_1\,(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\, R^2) > k_1 R\,(4kT + 2\overline{i_n{}^2} R)$$

$$2\overline{e_R{}^2} + 2\overline{e_n{}^2} + 2\overline{i_n{}^2}\, R^2 > 4kTR + 2\overline{i_n{}^2}\, R^2$$

$$\overline{e_R{}^2} + 2\overline{e_n{}^2} > 0$$

Then S/N increases with R_{gen} for any amplifier.

For any $e_{sig} < k_1\sqrt{R}$, an optimum R_{gen} may be determined. Take, for example, $e_{sig} = k_1\, R^{0.4}$, $\partial e_{sig}/\partial R = 0.4k_1\, R^{-0.6}$

$$(0.8k_1/R^{0.6})(\overline{e_R{}^2} + \overline{e_n{}^2} + \overline{i_n{}^2}\, R^2) > k_1\, R^{0.4}\,(4kT + 2\overline{i_n{}^2} R)$$

$$0.8\,\overline{e_R{}^2} + 0.8\,\overline{e_n{}^2} + 0.8\,\overline{i_n{}^2}\, R^2 > 4kTR + 2\,\overline{i_n{}^2}\, R^2$$

$$0.8\,\overline{e_n{}^2} > 0.2\,\overline{e_R{}^2} + 1.2\,\overline{i_n{}^2}\, R^2$$

Then S/N increases with R_{gen} until

$$0.25\,\overline{e_R{}^2} + 1.5\,\overline{i_n{}^2}\, R^2 = \overline{e_n{}^2}$$

Fast IC Power Transistor with Thermal Protection

National Semiconductor
Application Note 110
Robert C. Dobkin
May 1974

INTRODUCTION

Overload protection is perhaps most necessary in power circuitry. This is shown by recent trends in power transistor technology. Safe-area, voltage and current handling capability have been increased to limits far in excess of package power dissipation. In RF transistors, devices are now available and able to withstand badly mismatched loads without destruction. However, for anyone working with power transistors, they are still easily destroyed.

Since power circuitry, in many cases, drives other low level circuitry—such as a voltage regulator—protection is doubly important. Overloads that cause power transistor failure can result in the destruction of the entire circuit. This is because the common failure mode for power transistors is a short from collector to emitter—applying full voltage to the load. In the case of a voltage regulator, the raw supply voltage would be applied to the low level circuitry.

A new monolithic power transistor provides virtually absolute protection against any type of overload. Included on the chip are current limiting, safe area protection and thermal limiting. Current limiting controls the peak current through the chip to a safe level below the fuzing current of the aluminum metalization. At high collector to emitter voltage the safe area limiting reduces the peak current to further protect the power transistor. If, under prolonged overload, power dissipation causes chip temperature to rise toward destructive levels, thermal limiting turns off the device keeping the devices at a safe temperature. The inclusion of thermal limiting, a feature not easily available in discrete circuitry makes this device especially attractive in applications where normal protective schemes are ineffective.

The device's high gain and fast response further reduce requirements of surrounding circuitry. As well as being used in linear applications, the IC can interface transistor-transistor logic or complementary-MOS logic to power loads without external devices. In fact, the input-current requirement of 3 microamperes is small enough for one CMOS gate to drive over 400 LM195's.

Besides high dc current gain, the IC has low input capacitance so it can be easily driven from high impedance sources—even at high frequencies. In a standard TO-3 power package, the monolithic structure ties the emitter, rather than the collector, to the case effectively bootstrapping the base-to-package capacitance. Additionally, connecting the emitter to the package is especially convenient for grounded emitter circuits.

The device is fully protected against any overload condition when it is used below the maximum voltage rating. The current-limiting circuitry restricts the power dissipation to 35 watts, 1.8 amperes are available at collector-to-emitter voltage of 17V decreasing to about 0.8 amperes at 40V. In reality, however, like standard transistors, power dissipation in actual use is limited by the size of the external heat sink.

Switching time is fast also. At 40V 25 Ohm load can be switched on or off in a relatively fast 500 ns. The internal planar double diffused monolithic transistors have an f_t of 200 MHz to 400 MHz. The limiting factor on overall speed is the protective and biasing circuitry around the output transistors. An important performance point is that no more than the normal 3μA base current is needed for fast switching.

To the designer, the LM195 acts like an ordinary power transistor, and its operation is almost identical to that of a standard power device. However, it provides almost absolute protection against any type of overload. And, since it is manufactured with standard seven-mask IC technology, the device is produceable in large quantities at reasonable cost.

CIRCUIT DESIGN

Besides the protective features, the monolithic power transistor should function as closely to a discrete transistor as possible. Of course, due to the circuitry on the chip, there will be some differences.

Figure 1 shows a simplified schematic of the power transistor. A power NPN Darlington is driven by an input PNP. The PNP and output NPN's are biased by internal current source I_1. The composite three transistors yield a total current gain in excess of 10^6 making it easy to drive the power transistors from high impedance sources. Unlike normal power transistors, the base current is negative, flowing out of the PNP. However, in most cases this is not a problem.

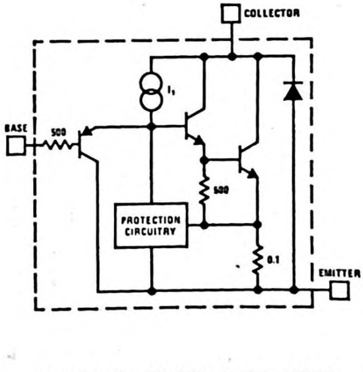


FIGURE 1. Simplified Circuit of the LM195

The input PNP transistor is made with standard IC processing and has a reverse base-emitter breakdown voltage in excess of 40V. This allows the power transistor to be driven from a stiff voltage source without damage due to excessive base current. At input voltages in excess of about 1V the input PNP becomes reverse biased and no current is drawn from the base lead. In fact it is possible for the base of the monolithic transistor to be driven with up to 40V even though the collector to emitter voltage is low. Further, the input PNP isolates the base drive from the protective circuitry insuring that even with high base drive the device will be protected. When the device is turned off current I_1 is shunted from the base of the NPN transistor by the PNP and appears at the emitter terminal. This sets the minimum load current to about 2 mA, not a severe restriction for a power transistor. Because of the PNP and I_1, the power transistor turns "on" rather than "off" if the base is opened; however, most power circuits already include a base-emitter resistor to absorb leakage currents in present power transistors.

A schematic of the LM195 is shown in *Figure 2*. The circuitry is biased by four current sources comprised of Q4, Q7, Q8 and Q9. The operating current is set by Q5 and Q6 and is relatively independent of supply voltage. FET Q1 and R2 insure reliable starting of the bias circuitry while D1 clamps the output of the FET limiting the starting current at high supply voltage.

The output transistors Q19 and Q20 are driven from input PNP Q14. Current limiting independent of temperature changes is provided by Q21, Q16, and Q15. At high collector to emitter voltages the current limit decreases due to the voltage across R21 from D3, D4 and R20. The double emitter structure used on Q21 allows the power limiting to more closely approximate constant power curve rather than a straight line decrease in output current as input voltage increases.

Transistor Q13 thermally limits the device by removing the base drive at high temperature. The actual temperature sensing is done by Q11 and Q12 with Q10 regulating the voltage across the sensors so thermal limit temperature remains independent of supply. As temperature increases, the collector current of Q11 increases while the V_{BE} of Q12 decreases. At about 170°C the Q12 turns on Q13 removing the base drive from the output transistors. Finally, C1, Q2 and Q3 boost operating currents during switching to obtain faster response time and Q17 and Q18 compensate for h_{fe} variations in the power devices.

PERFORMANCE

The new power transistor is packaged in a standard TO-3 transistor package making it compatible with standard power transistors. An added advantage of the monolithic structure is that the emitter is tied to the case rather than the collector. This allows the device to be connected directly to ground in collector output applications.

A photomicrograph of the LM195 is shown in *Figure 3*. More than half of the die area is needed for the output power transistor (Q20). Actually, the power transistor is many individual small transistors connected in parallel with a common collector. Partitioning the power device into small discrete areas improves power handling over a single large device. Firstly, the power device has ten base sections spread across the chip. Between the base diffusion are N+ collector contacts. Each section has its own emitter ballasting resistor to insure current sharing between sections. One of these resistors is used to sense the output current for current limiting.

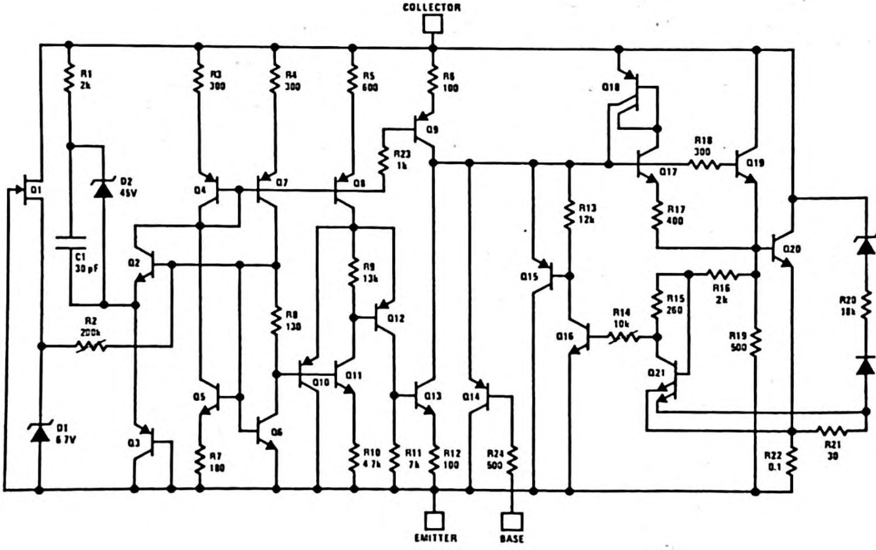


FIGURE 2. Schematic Diagram of the LM195

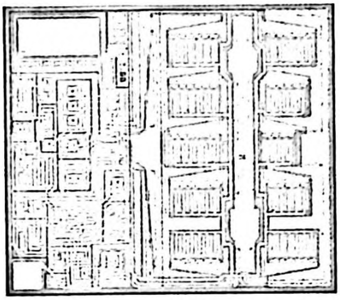


FIGURE 3. LM195 Chip

TABLE I. Typical Performance

Collector to Emitter Voltage	42V
Base to Emitter Voltage (max.)	42V
Peak Collector Current (internally limited)	1.8 amps
Reverse Base Emitter Voltage	20V
Base to Emitter Voltage (I_C = 1.0 amp)	0.9V
Base Current	3μA
Saturation Voltage	2V
Switching Time (turn on or turn off)	500 ns
Power Dissipation (internally limited)	35 watts
Thermal Limit Temperature	165°C
Maximum Operating Temperature	150°C
Thermal Resistance (Junction to Case)	2.3°C/W

A detail of one of the base sections is shown in *Figure 4.* An interdigitated structure is used with alternating base contacts and emitter stripes. Integrated into each emitter is an individual emitter ballasting resistor to insure equal current sharing between emitters in each section. Aluminum metalization runs the length of the emitter stripe to prevent lateral voltage drop from debiasing a section of the stripe at high operating currents. All current in the stripe flows out through the small ballasting resistor where it is summed with the currents from the other stripes in the section. The partitioning in conjunction with the emitter resistor gives a power transistor with large safe-area and good power handling capability.

APPLICATIONS

With the full protection and high gain offered by this monolithic power transistor, circuit design is considerably simplified. The inclusion of thermal limiting, not normally available in discrete design allows the use of smaller heat sinks than with conventional protection circuitry. Further, circuits where protection of the power device is difficult–if not impossible–now cause no problems.

For example, with only current limiting, the power transistor heat sink must be designed to dissipate worst case overload power dissipation at maximum ambient temperature. Wheh the power transistor is thermally limited, only normal power need be dissipated by the heat sink. During overload, the device is allowed to heat up and thermally limit, drastically reducing the size of the heat sink needed.

Switching circuits such as lamp drivers, [illegible]d drivers or switching regulators do not dissipate much power during normal operation and usually no heat sink is necessary. However, during overload, the full supply voltage times the maximum output current must be dissipated. Without a large heat sink standard power transistors are quickly destroyed.

Using this new device is easier than standard power transistors but a few precautions should be observed. About the only way the device can be destroyed is excessive collector to emitter voltage or improper power supply polarity. Sometimes when used as an emitter follower, low level high frequency oscillations can occur. These are easily cured inserting a 5k-10k resistor in series with the base lead. The resistor will eliminate the oscillation without effecting speed or performance. Good power supply bypassing should also be used since this is a high frequency device.

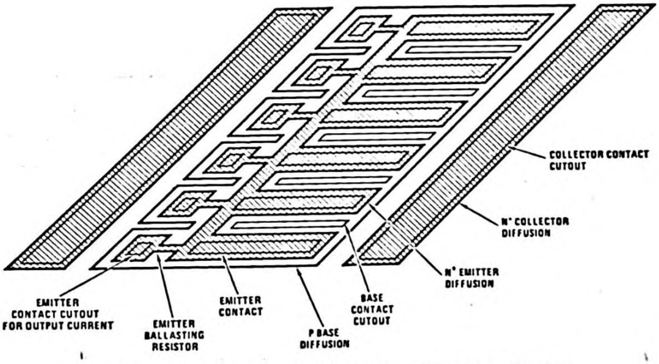
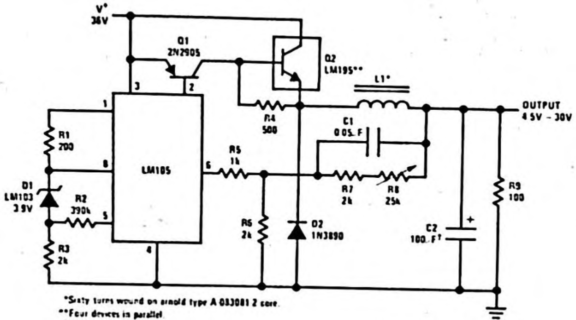


FIGURE 4. Detailed Structure of one Section of the Power Transistor



*Sixty turns wound on arnold type A 083081 2 core.
**Four devices in parallel.
†Solid tantalum.

FIGURE 5. 6 Amp Variable Output Switching Regulator

Figure 5 shows a 6 amp, variable output switching regulator for general purpose applications. An LM105 positive regulator is used as the amplifier-reference for the switching regulator. Positive feedback to induce switching is obtained from the LM105 at pin 1 through an LM103 diode. The positive feedback is applied to the internal amplifier at pin 5 and is independent of supply voltage. This forces the LM105 to drive the pass devices either "on" or "off," rather than linearly controlling their conduction. Negative feedback, delayed by L1 and the output capacitor, C2, causes the regulator to switch with the duty cycle automatically adjusting to provide a constant output. Four LM195's are used in parallel to obtain a 6 amp output since each device can only supply about 2 amps. Note that no ballasting resistors are needed for current sharing. When Q1 turns "on" all bases are pulled up to V$^+$ and no base current flows in the LM195 transistors since the input PNP's are reverse biased.

A two terminal current/power limiter is shown in *Figure 6*. The base and collector are shorted—turning the power transistor on. If the load current exceeds 2 amps, the device current limits protecting the load. If the overload remains on, the device will thermal limit, further protecting itself and the load. In normal operation, only 2V appear across the device so high efficiency is realized and no heat sink is needed. Another method of protection would be to place the monolithic power transistor on a common heat sink with the devices to be protected. Overheating will then cause the LM195 to thermal limit protecting the rest of the circuitry.

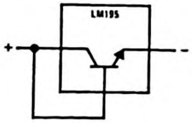


FIGURE 6. Two Terminal Current Limiter

The low base current make this power device suitable for many unique applications. *Figure 7* shows a time delay circuit. Upon application of power or S1 closing, the load is energized. Capacitor C1 slowly charges toward V$^-$ through R1. When the voltage across R1 decreases below about 0.8 volts the load is de-energized. Long delays can be obtained with small capacitor values since a high resistance can be used.

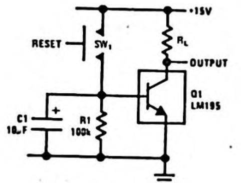
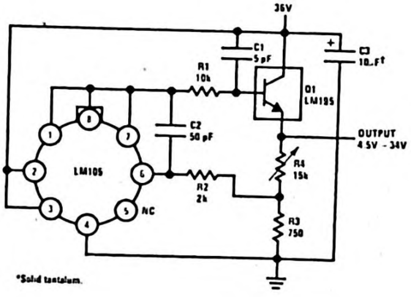


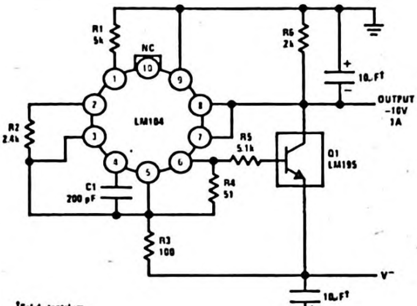
FIGURE 7. Time Delay Circuit

Figure 8 and 9 show how the LM195 can be used with standard IC's to make positive or negative voltage regulators. Since the current gain of the LM195 is so high, both regulators have better than 2 mV load regulation. They are both fully overload protected and will operate with only 2V input-to-output voltage differential.



*Solid tantalum.

FIGURE 8. 1 Amp Positive Voltage Regulator



†Solid tantalum.

FIGURE 9. 1 Amp Negative Regulator

An optically isolated power transistor is shown in *Figure 10.* D1 and D2 are almost any standard optical isolator. With no drive, R1 absorbs the base current of Q1 holding it off. When power is applied to the LED, D2 allows current to flow from the collector to base. Less than 20μA from the diode is needed to turn the LM195 fully on.

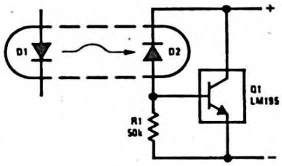


FIGURE 10. Optically Isolated Power Transistor

An alternate connection for better ac response is to return the cathode of D2 to separate positive supply rather than the collector of Q1, as shown in *Figure 11,* eliminating the added collector to base capacitance of the diode. With this circuit a 40V 1 amp load can be switched in 500 ns. Of course, any photosensitive diode can be used instead of the opto-isolator to make a light activated switch.

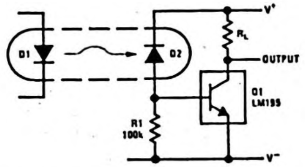


FIGURE 11. Fast Optically Isolated Switch

A power lamp flasher is shown in *Figure 12.* It is designed to flash a 12V bulb at about a once-per-second rate. The reverse base current of Q2 provides biasing for Q1 eliminating the need for a resistor. Typically, a cold bulb can draw 8 times its normal operating current. Since the LM195 is current limited, high peak currents to the bulb are not experienced during turn-on. This prolongs bulb life as well as easing the load on the power supply.

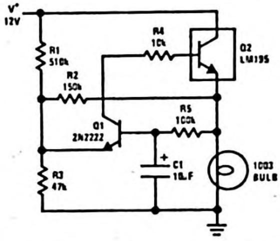
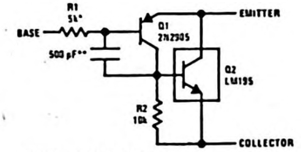


FIGURE 12. 1 Amp Lamp Flasher

Since no PNP equivalent of this device is available, it is advantageous to use the LM195 in a quasi-complementary configuration to simulate a power PNP. *Figure 13* shows a quasi PNP made with an LM195. A low current PNP is used to drive the LM195 as the power output device. Resistor R1 protects against overdrive destroying the PNP and, in conjunction with C1, frequency compensates the loop against oscillations. Resistor R2 sets the operating current for the PNP and limits the collector current.



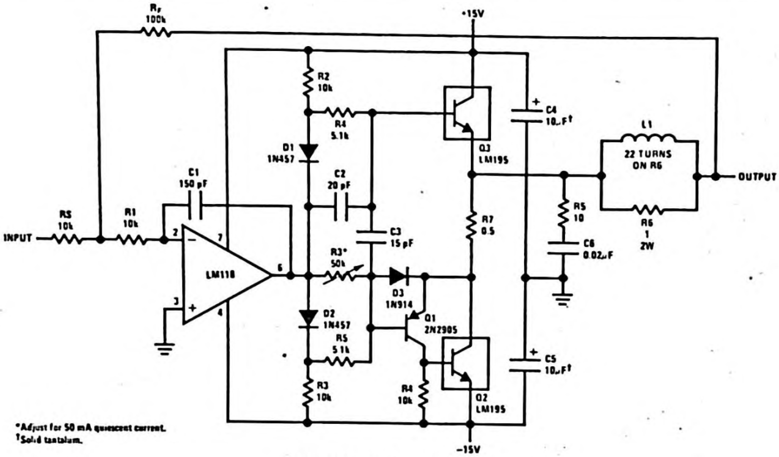
*Protects against excessive base drive.
**Needed for stability.

FIGURE 13. PNP Configuration for LM195

Figure 14 shows a power op amp with a quasi-complementary power output stage. Q1 and Q2 form the equivalent of a power PNP. The circuit is simply an op amp with a power output stage. As shown, the circuit is stable for almost any load. Better bandwidth can be obtained by decreasing C1 to 15 pF (to obtain 150 kHz full output response), but capacitive loads can cause oscillation. If due to layout, the quasi-complimentary loop oscillates, collector to base capacitance on Q1 will stabilize it. A simpler power op amp for up to 300 Hz operation is shown in *Figure 15.*

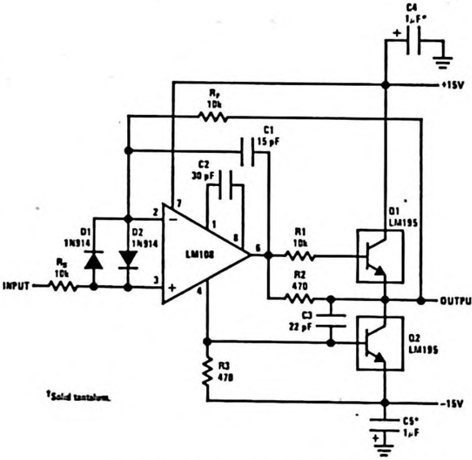
One of the more difficult circuit types to protect is a current regulator. Since the current is already fixed, normal protection doesn't work. Circuits to limit the voltage across the current regulator may allow excessive current to flow through the load. About the only protection method that protects both the regulator and the driven circuit is thermal limiting.

A 100 mA, two terminal regulator is shown in *Figure 16.* The circuit has low temperature coefficient and operates


R$_F$
100k
+15V
R2
10k
R4
5.1k
D1
1N457
C1
150 pF
C2
20 pF
C3
15 pF
R3*
50k
RS
10k
R1
10k
INPUT
2
7
LM118
6
3
4
D3
1N914
Q1
2N2905
D2
1N457
R5
5.1k
R3
10k
R4
10k
Q3
LM195
Q2
LM195
R7
0.5
C4
10μF†
C5
10μF†
L1
22 TURNS
ON R6
R5
10
C6
0.02μF
R6
1
2W
OUTPUT
−15V

*Adjust for 50 mA quiescent current.
†Solid tantalum.

FIGURE 14. Power Op Amp


C4
1μF*
+15V
R$_F$
10k
C1
15 pF
C2
30 pF
D1
1N914
D2
1N914
R$_S$
10k
INPUT
2
3
7
1
8
6
4
LM108
R1
10k
R2
470
C3
22 pF
Q1
LM195
Q2
LM195
OUTPUT
R3
470
−15V
C5*
1μF

†Solid tantalum.

FIGURE 15. 1 Amp Voltage Follower

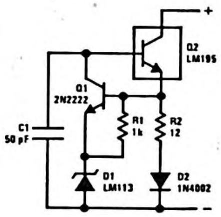

+
Q2
LM195
Q1
2N2222
R1
1k
R2
12
C1
50 pF
D1
LM113
D2
1N4002
−

FIGURE 16. Two Terminal 100 mA Current Regulator

down to 3V. Once again, the reverse base current of the LM195 to bias the operating circuitry.

A 2N2222 is used to control the voltage across a current sensing resistor, R2 and diode D1, and therefore the current through it. The voltage across the sense network is the V_{BE} of the 2N2222 plus 1.2V from the LM113. In the sense network R2 sets the current while D1 compensates for the V_{BE} of the transistor. Resistor R1 sets the current through the LM113 to 0.6 mA.

CONCLUSIONS

A new IC power transistor has been developed that significantly improves power circuitry reliability. The device is virtually impossible to destroy through abuse. Further it has high gain and fast response. It is manufactured with standard seven mask IC technology making it produceable in large quantities at reasonable prices. Finally, in addition to the protection features, it has high gain simplifying surrounding circuitry.

Wide Range Function Generator

National Semiconductor
Application Note 115
Robert C. Dobkin
July 1974

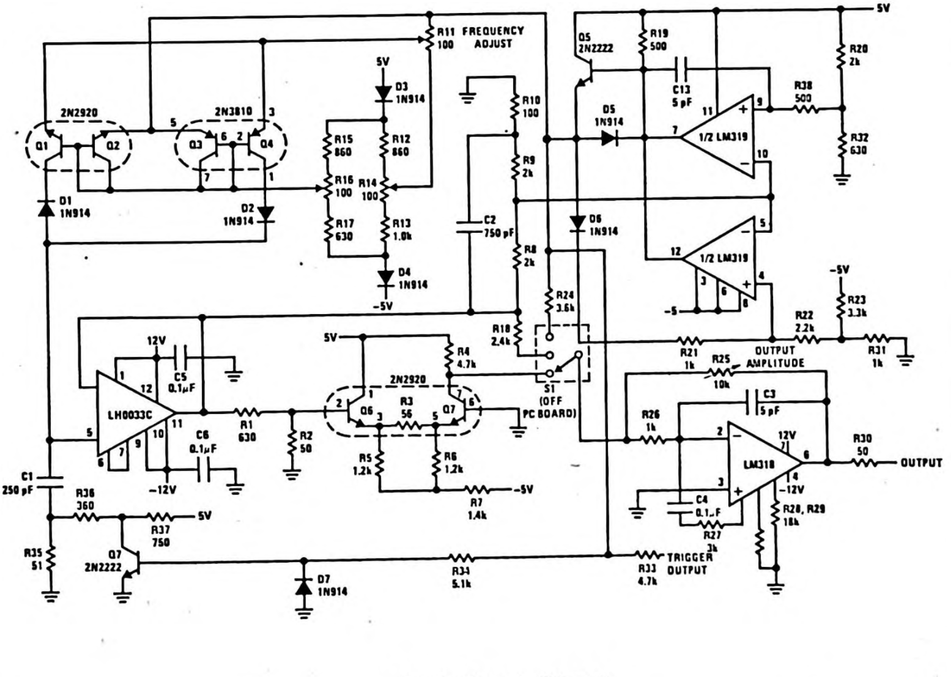
The sine, square, triangle function generator has proven to be exceptionally useful. Various IC circuits have been published for generating square and triangle waveforms in an attempt to duplicate the general purpose function generator. However, these simple circuits are usually limited to about 10 kHz and have no sine wave output. The function generator shown here provides all three waveforms and operates from below 10 Hz to 1 MHz with usable output to about 2 MHz.

DESIGN

As with most function generators, an integrator-comparator generates the square and triangle waveforms with a shaping circuit forming the triangle wave into a sine wave.

Obtaining six decades of operating with a single control plus 2 MHz operation requires some unusual circuit design techniques as well as good high frequency IC's. The triangle wave is generated by switching current-source transistors to alternately charge and discharge the timing capacitor. This generates a linear tri-wave without the use of an op amp integrator. A FET voltage follower buffers the tri-wave and drives the comparator, output amplifier and sine converter.

A precision dual comparator is used to set the peak-to-peak amplitude of the tri-wave. It is necessary to accurately control the tri-wave since the sine converter requires close amplitude control to produce a low distortion output. An accurate divider across the 5V supply regulators sets the threshold at the inputs of the LM319 comparator. The tri-wave is applied to the other comparator inputs through another divider—R8, R9, R10 and C2. The comparator switches when the amplitude of the tri-wave is ±2.5V. Capacitor C2 compensates for delays in the comparator at high frequencies.


R11 FREQUENCY ADJUST 100
2N2920
2N3810
Q1
Q2
Q3
Q4
D1 1N914
D2 1N914
D3 1N914
D4 1N914
5V
-5V
R15 860
R12 860
R16 100
R14 100
R17 630
R13 1.0k
R10 100
R9 2k
R8 2k
C2 750 pF
R18 2.4k
R24 3.6k
D6 1N914
S1 (OFF PC BOARD)
Q5 2N2222
R19 500
C13 5 pF
D5 1N914
1/2 LM319
R38 500
R20 2k
R32 630
R23 3.3k
R22 2.2k
R21 1k
R31 1k
R25 10k OUTPUT AMPLITUDE
C3 5 pF
R26 1k
LM318
12V
-12V
R30 50
OUTPUT
C4 0.1 µF
R27 3k
R28, R29 10k
R33 4.7k
TRIGGER OUTPUT
LH0033C
C5 0.1 µF
C6 0.1 µF
R1 630
R2 50
R4 4.7k
Q6
Q7
R3 56
R5 1.2k
R6 1.2k
R7 1.4k
C1 250 pF
R36 360
R37 750
R35 51
Q7 2N2222
D7 1N914
R34 5.1k

Function Generator Schematic

PARTS LIST

R1	630Ω	1%
R2	50Ω	1%
R3	56Ω	5%
R4	4.7k	5%
R5	1.2k	1%
R6	1.2k	1%
R7	1.4k	1%
R8	2k	5%
R9	2k	5%
R10	100Ω	5%
R11	100Ω potentiometer	
R12	860Ω	5%
R13	1k	5%
R14	100Ω PC mount trimpot	
R15	860Ω	5%
R16	100Ω PC mount trimpot	
R17	630Ω	5%
R18	2.4k	5%
R19	500Ω	5%
R20	2k	5%
R21	1k	5%
R22	2.2k	5%
R23	3.3k	5%
R24	3.6k	5%
R25	10k potentiometer	
R26	1k	5%
R27	3k	5%
R28	18k	5%
R29	18k	5%
R30	50Ω	5%
R31	1k	5%
R32	630Ω	5%
R33	4.7k	5%
R34	5.1k	5%
R35	51Ω	5%
R36	360Ω	5%
R37	750Ω	5%
R38	500Ω	5%

C1	250 pF		
C2	750 pF		
C3	5 pF		
C4	0.1μF		
C5	0.1μF		
C6	0.1μF		
C7	500μF	25V	
C8	500μF	25V	
C9	4.7μF		Solid Tantalum
C10	4.7μF		Solid Tantalum
C11	4.7μF		Solid Tantalum
C12	4.7μF		Solid Tantalum
C13	5 pF		

Q1–Q2	2N2920	Dual NPN
Q3–Q4	2N3810	Dual PNP
Q5	2N2222	
Q6–Q7	2N2920	Dual NPN
Q8	2N2222	

D1–D7 1N914
1–Varo VE27 Full Wave Bridge

1–LM318H Operational Amplifier
1–LM319N Dual Comparator
1–LH0033C Fast Buffer
1–LM340K 12V Positive Voltage Regulator
1–LM320K −12V Negative Voltage Regulator
1–LM309H 5V Positive Voltage Regulator
1–LM320H −5V Negative Voltage Regulator

TI = Triad F90X

S_1–3 Position ST Switch
S_2–SPST Switch

1/4 Amp Fuse and Holder–PC Board, Mounting Hardware, etc.

A square wave output from the comparator is obtained at the emitter of Q5 and is used to drive both the current switches and output amplifier. The current switches–Q1, Q2, Q3, Q4–provide a 5 nA to 5 mA current to timing capacitor, C1. The exponential relationship between emitter-base voltage and collector current allows a six decade current range to be obtained with a single potentiometer. The maximum output current is set by the current through R15 or R17 (depending on polarity) and appears when the arm of the frequency control, R11, ties all four emitters together. As R11 is rotated, a voltage is developed between the emitters of Q1–Q4 and Q2–Q3. This voltage decreases the emitter base voltage of Q1 and Q4 decreasing their operating current. About 380 mV is developed across R11 and corresponds to over a 10^6 reduction in charging current.

Converting the tri-wave to a sine wave also uses the non-linear relationship between emitter-base voltage and collector current of a transistor pair.

Transistors Q6 and Q7 form a differential amplifier with emitter degeneration. The tri-wave is attenuated by R1 and R2 to about 450 mV and applied to one half of the pair–Q6. This drives the transistors non-linearly producing a sine wave output current at the collector of Q7 to drive the output amplifier.

The output amp, an LM318, uses feedforward compensation to maximize bandwidth and slew rate. It is used for adjustable scaling of all three waveforms to ±10V. Even with the feedforward, there is not quite enough bandwidth for good reproduction of the triangle or square wave at frequencies over 1 MHz. Therefore, if the higher frequencies are of major interest, a faster output amplifier is necessary.

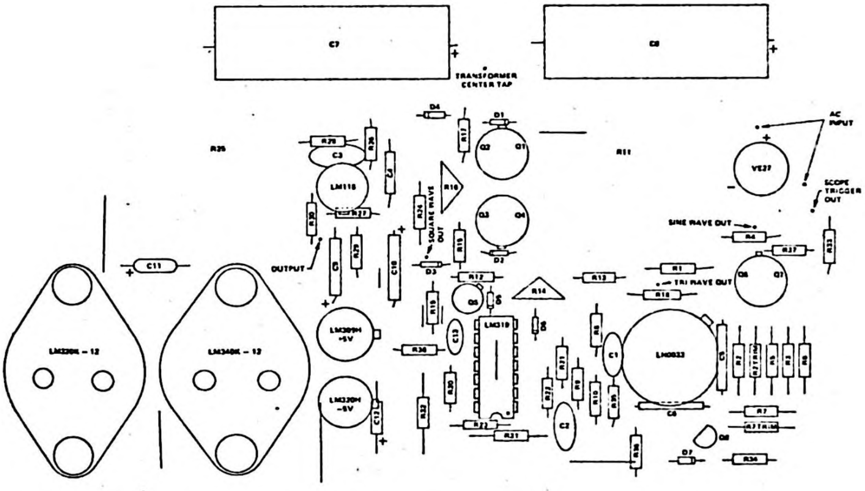
CONSTRUCTION AND SET UP

It is important to observe good construction practices for proper operation. All four power supplies should be bypassed with 4.7μF solid tantalum capacitors on the circuit board. Since the circuit operates at relatively high frequencies, short leads and a compact layout is a good idea. The wiring to the function selector switch should be made with shielded wire to minimize spikes from the fast square wave. At low frequencies, charging currents to the timing capacitor are quite low, so 60 Hz pickup can modulate the operating frequency. Shielding the current sources and C1 from the power transformer is in order.

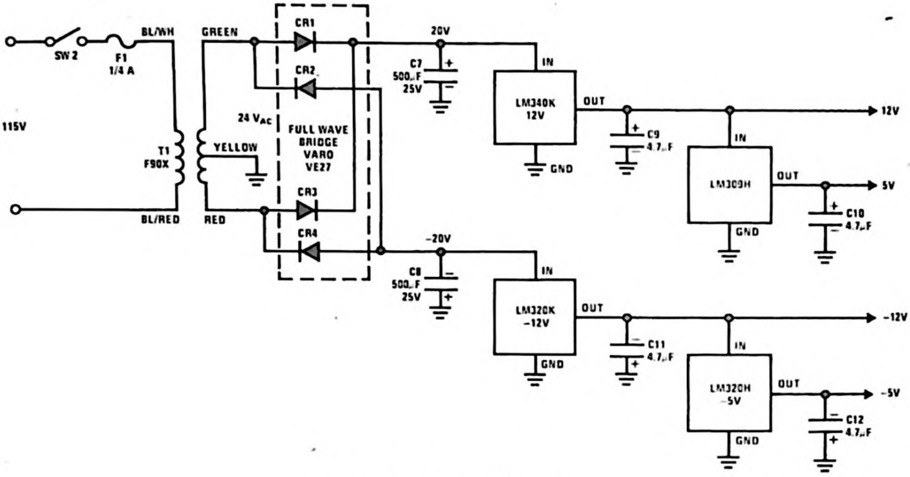
All transistors used to set the timing currents must track with temperature changes. Of course, the individual pairs will track but the NPN pair must also track the PNP pair as well. There are many small heat sinks for transistors which can be used to thermally couple Q1, Q2, to Q3, Q4. Temperature differences between the pair will cause the symmetry to change.

Set up is not difficult either. Firstly, R11 is set for a 1 MHz output. Then R16 is used to adjust the output symmetry. Secondly, R11 is set to provide a 10 Hz output and the symmetry is again adjusted by R14.

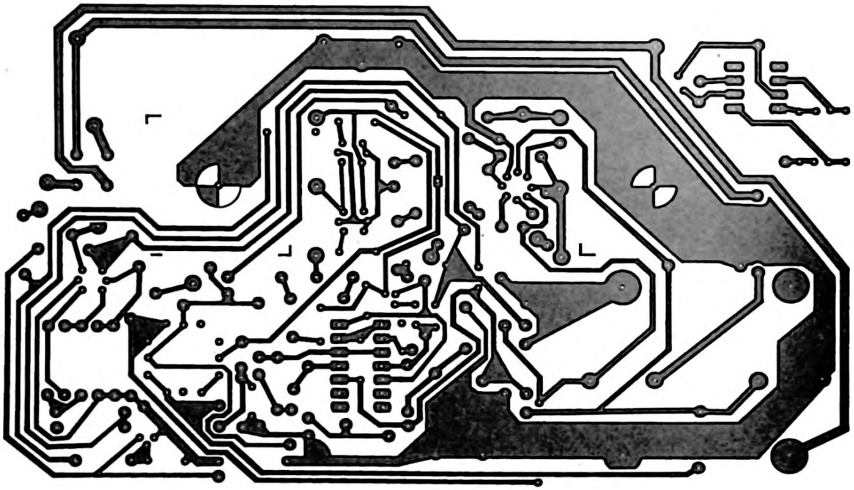
Other possible adjustments that may be necessary are in the sine converter. R7 can be trimmed if the sine output (from the LM318) has a dc offset. Also, it may be necessary to adjust R2 to minimize distortion. (It should be mentioned that there can be considerable distortion if the symmetry of the tri-wave is not 50%.)


C7
C8
TRANSFORMER CENTER TAP
AC INPUT
R25
R28
C3
R26
LM118
R30
R27
R29
C9
C10
OUTPUT
SQUARE WAVE OUT
R24
R16
D4
R17
D1
Q2
Q1
Q3
Q4
D2
D3
R11
VE27
SCOPE TRIGGER OUT
SINE WAVE OUT
R4
R37
R33
C11
LM320K – 12
LM340K – 12
LM309H +5V
LM320H –5V
C12
R36
C13
R19
R32
R20
R12
Q5
D5
R14
R13
R1
TRI WAVE OUT
R18
Q6
Q7
LM319
D6
R8
R21
R22
R9
R10
R35
C1
LM0033
C5
R2
R2 TRIM
R5
R3
R6
C6
R7
R7 TRIM
Q8
C2
R31
R38
D7
R34

Component Location, Top View


SW 2
F1
1/4 A
BL/WH
GREEN
CR1
CR2
20V
C7
500μF
25V
IN
LM340K
12V
OUT
12V
115V
24 V$_{AC}$
FULL WAVE
BRIDGE
VARO
VE27
T1
F90X
YELLOW
C9
4.7μF
GND
IN
LM309H
OUT
5V
C10
4.7μF
GND
CR3
BL/RED
RED
CR4
−20V
C8
500μF
25V
IN
LM320K
−12V
OUT
−12V
C11
4.7μF
GND
IN
LM320H
−5V
OUT
−5V
C12
4.7μF
GND

Power Supply Section Schematic



Circuit Board Layout
(This PC layout must be enlarged approximately 120% in order to be usable.)

Use the LM158/LM258/LM358 Dual, Single Supply Op Amp

National Semiconductor
Application Note 116
Jim Sherwin
May 1974

INTRODUCTION

Use the LM158/LM258/LM358 dual op amp with a single supply in place of the MC1458/MC1558/MC1558C with split supply and reap the profits in terms of:

- a. Input and output voltage range down to the negative (ground) rail
- b. Single supply operation
- c. Lower standby power dissipation
- d. Higher output voltage swing
- e. Lower input offset current
- f. Generally similar performance otherwise.

The main advantage, of course, is that you can eliminate the negative supply in many applications and still retain equivalent op amp performance. Additionally, and in some cases more importantly, the input and output levels are permitted to swing down to ground (negative rail) potential. Table I shows the relative performance of the two in terms of guaranteed and/or typical specifications.

In many applications the LM158/LM258/LM358 can also be used directly in place of LM1558 for split supply operation.

SINGLE SUPPLY OPERATION

The MC1458/MC1558 or similar op amps exhibit several important limitations when operated from a single positive (or negative) supply. Chief among these is that input and output signal swing is severely limited for a given supply as shown in *Figure 1*. For linear operation, the input voltage must not reach within 3 volts of ground or of the supply, and output range is similarly limited to within 3–5 volts of ground or supply. This means that operation with a +12V supply could be limited as low as 2 Vp-p output swing. The LM358 however, allows a 10.5 Vp-p output swing for the same 12V supply. Admittedly these are worst case specification limits, but they serve to illustrate the problem.

TABLE I. Comparison of Dual Op Amps, MC1458 and LM358

CHARACTERISTIC	MC1458	LM358
V_{IO}	6 mV Max	7 mV Max
CM V_I	24 Vp-p*	0 – 28.5V*
I_{IO}	200 nA	50 nA
I_{OB}	500 nA	−500 nA
CMRR	60 dB Min @ 100 Hz 90 dB Typ	85 dB Typ @ DC
$\overline{e}_n$ @ 1 kHz, R_{GEN} 10 kΩ	45 $nV/\sqrt{Hz}$ Typ	40 $nV/\sqrt{Hz}$ Typ**
Z_{IN}	200 MΩ Typ	Typ 100 MΩ
A_{VOL}	20k Min 100k Typ	100k Typ
f_c	1.1 MHz Typ	1 MHz Typ**
P_{BW}	14 kHz Typ	11 kHz Typ**
dV_o/dt	0.8V/μs Typ	0.5V/μs Typ**
V_o @ R_L = 10k/2k	24/20 Vp-p*	28.5 Vp-p
I_{SC}	20 mA Typ	Source 20 mA Min (40 Typ) Sink 10 mA Min (20 Typ)
PSRR @ DC	37 dB Min 90 dB Typ	100 dB Typ
I_D (R_L = ∞)	8 mA Max	2 mA Max

‡From laboratory measurement
*Based on V_S = 30V on LM358 only, or V_S = ±15V
**From data sheet typical curves

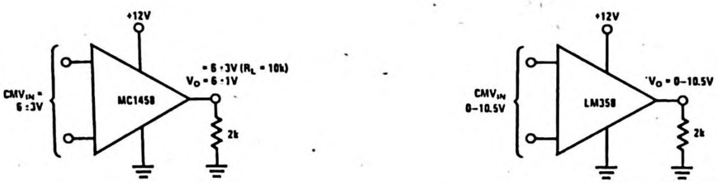


FIGURE 1. Worst Case Signal Levels with +12V Supply

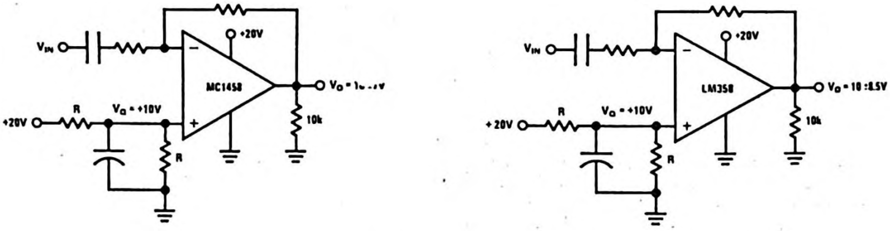


FIGURE 2. Operating with AC Signals

AC GAIN

For ac signals the input can be capacitor coupled. The input common mode and quiescent output voltages are fixed at one-half the supply voltage by a resistive divider at the non-inverting input as shown in *Figure 2*. This quiescent output could be set at a lower voltage to minimize power dissipation in the LM358, if desired, so long as $V_Q \geq V_{IN}$ pk. For the MC1458 the quiescent output must be higher, $V_Q \geq 3V + V_{IN}$ pk thus, for small signals, power dissipation is much greater with the MC1458. Example: Required $V_O = V_Q \pm 1V$ pk into 2k, V_{SUPPLY} = as required. Find quiescent dissipation in load and amplifier for MC1458 and LM358.

LM358	MC1458
$V_Q = +1V$	$V_Q = 4V$
$V_{SUPPLY} = +3.5V$	$V_{SUPPLY} = 8V$
$P_{LOAD} = \frac{E_L^2}{R_L} = \frac{1}{2k} = 0.5\ mW$	$P_{LOAD} = \frac{4^2}{2k} = 8\ mW$
$P_D = V_S I_S^* + (V_S - V_Q) I_L$	$P_D = P_D^* + (V_S - V_Q) I_L$
$= 3.5V \times 0.7\ mA + (3.5 - 1) \frac{1V}{2k}$	$= 22\ mW + (8 - 4) \frac{4V}{2k}$
$P_D = 2.45 + 1.25 = 3.7\ mW$	$P_D = 22 + 8 = 30\ mW$
$P_{TOTAL} = 3.7 + 0.5 = 4.2\ mW$	$P_{TOTAL} = 30 + 8 = 38\ mW$
*From typical characteristics	*From typical characteristics

The MC1458 requires over twice the supply voltage and nearly 10 times the supply power of the LM358 in this application.

INVERTING DC GAIN

Connections and biasing for dc inverting gain are essentially the same as for the ac coupled case. Note, of course, that the output cannot swing negative when operated from a single positive supply. *Figure 3* shows the connections and signal limitations.

NON-INVERTING DC GAIN

The non-inverting gain connection does not require the V_Q biasing as before; the inverting input can be returned to ground in the usual manner for gains greater than unity, (see *Figure 4*). A tremendous advantage of the LM358 in this connection is that input signals and output may extend all the way to ground; therefore dc signals in the low-millivolt range can be handled. The MC1458 still requires that V_{IN} = 3–17V. Therefore maximum gain is limited to $A_V = (V_O - 3)/3$, or A_V max = 5.4 for a 20V supply.

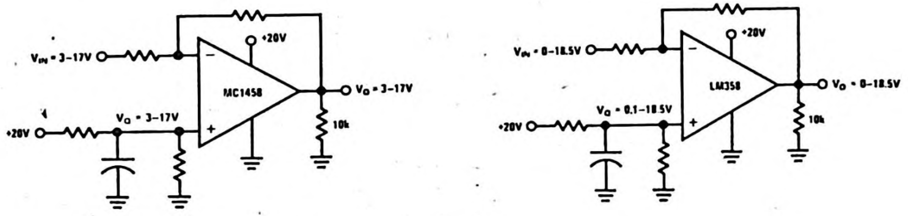
There is no similar limitation for the LM358.

ZERO T.C. INPUT BIAS CURRENT

An interesting and unusual characteristic is that I_{IN} has a zero temperature coefficient. This means that matched resistance is not required at the input, allowing omission of one resistor per op amp from the circuit in most cases.

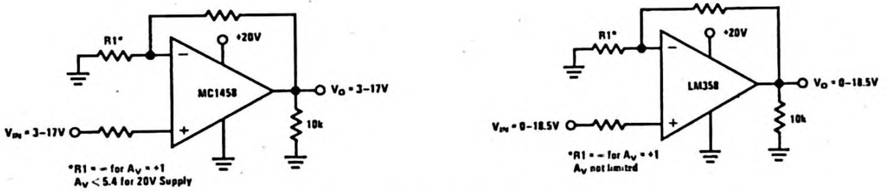
BALANCED SUPPLY OPERATION

The LM358 will operate satisfactorily in balanced supply operation so long as a load is maintained from output to the negative supply.



V_{IN} = 3–17V
+20V
MC1458
V_O = 3–17V
+20V
V_O = 3–17V
10k
V_{IN} = 0–18.5V
+20V
LM358
V_O = 0.1–18.5V
+20V
V_O = 0–18.5V
10k

FIGURE 3. Typical DC Coupled Inverting Gain

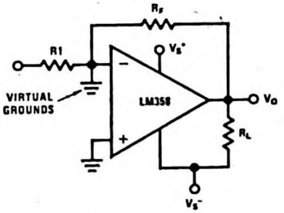


R1*
+20V
MC1458
V_O = 3–17V
10k
V_{IN} = 3–17V
R1*
+20V
LM358
V_O = 0–18.5V
10k
V_{IN} = 0–18.5V

*R1 = ∞ for A_V = +1
A_V < 5.4 for 20V Supply

*R1 = ∞ for A_V = +1
A_V not limited

FIGURE 4. Typical DC Coupled Non-Inverting Gain



R_F
R1
V_S^+
VIRTUAL GROUNDS
LM358
V_O
R_L
V_S^-

Crossover (distortion) occurs at $V_O = V_S^- \frac{R_F}{R_L + R_F}$

FIGURE 5. Split Supply Operation of LM358

The output load to negative supply forces the amplifier to source some minimum current at all times, thus eliminating crossover distortion. Crossover distortion without this load would be more severe than that expected with the normal op amp. Since the single supply design took notice of this normal load connection to ground, a class AB output stage was not included. Where ground referenced feedback resistors are used as in *Figure 5*, the required load to the negative supply depends upon the peak negative output signal level desired without exhibiting crossover distortion. R_L to the negative rail should be chosen small enough that the voltage divider formed by R_F and R_L will permit V_o to swing negative to the desired point according to the equation

$$R_L = R_F \frac{V_S^- - V_o}{V_o}$$

R_L could also be returned to the positive supply with the advantage that V_o max would never exceed (V_S^+ − 1.5V). Then with ±15V supplies $R_{L\ MIN}$ would be 0.12 R_F. The disadvantage would be that the LM358 can source twice as much current as it can sink, therefore R_L to negative supply can be one-half the value of R_L to positive supply.

The need for single or split supply is based on system requirements which may be other than op amp oriented. However if the only need for balanced supplies is to simplify the biasing of op amps, there are many systems which can find a cost effective benefit in operating LM358's from single supplies rather than standard op amps from balanced supplies. Of the usual op amp circuits, Table II shows those few which have limited function with single supply operation. Most are based on the premise that to operate from a single supply, a reference V_Q at about one-half the supply be available for bias or (zero) signal reference. The basic circuits are those listed in AN-20.

TABLE II. Conventional Op Amp Circuits Suitable for Single Supply Operation

APPLICATION	LIMITATIONS
AC Coupled amp‡	V_Q*
Inverting amp	V_Q
Non-inverting amp	OK*
Unity gain buffer	OK
Summing amp	V_Q
Difference amp	V_Q
Differentiator	V_Q
Integrator	V_Q
LP Filter	V_Q
I-V Connector	V_Q
PE Cell Amp	OK
I Source	$I_{O\ MIN} = \frac{1.5}{R1}$
I sink	OK
Volt Ref	OK
FW Rectifier	V_Q or modified circuit
Sine wave osc	V_Q
Triangle generator	V_Q
Threshold detector	OK
Tracking, regulator PS	Not practical
Programmable PS	OK
Peak Detector	OK to $V_{IN} = 0$

‡See AN20 for conventional circuits

*V_Q denotes need for a reference voltage, usually at about $\frac{V_S}{2}$

OK means no reference voltage required

LM377, LM378 and LM379 Dual Two, Four and Six Watt Power Amplifiers

National Semiconductor
Application Note 125
Jim Sherwin
January 1975

INTRODUCTION

The LM377, LM378 and LM379 are two-channel power amplifiers capable of delivering 2, 4, and 6 watts respectively into 8 or 16Ω loads. They feature on-chip frequency compensation, output current limiting, thermal shut-down protection, fast turn-on and turn-off without "pops" or pulses of active gain, an output which is self-entering at $V_{CC}/2$, and a 5 to 20 MHz gain-bandwidth product. Applications include stereo or multi-channel audio power output for phono, tape or radio use over a supply range of 10 to 35V, as well as servo amplifier, power oscillator and various instrument system circuits. Normal supply is single-ended, however, split supplies may be used without difficulty or degradation in power supply rejection.

CIRCUIT DESCRIPTION

The simplified schematic of *Figure 1* shows the important design features of the amplifier. The differential input stage made up of Q1–Q4 uses a double (split) collector PNP Darlington pair having several advantages. The high base-emitter breakdown of the lateral PNP transistor is about 60V which affords significant input over-voltage protection. The double collector allows operation at high emitter current to achieve good first stage f_t and minimum phase shift while simultaneously operating at low transconductance to allow internal compensation with a physically small capacitor C1. (Unity gain bandwidth of an amplifier with pole-splitting compensation occurs where the first stage transconductance equals ω C1.) Further decrease of transconductance is provided by degeneration caused by resistors at Q2 and Q3 emitters which also allow better large signal slew rate. The second collector provides bias current to the input emitter follower for increased frequency response and slew rate. Full differential input stage gain is provided by the "turnaround" differential to single-ended current source loads Q5 and Q6. The input common-mode voltage does not extend below about 0.5V above ground as might otherwise be expected from initial examination of the input circuit. This is because Q7 is actually preceeded by an emitter follower transistor not shown in the simplified circuit.

The second stage Q7 operates common-emitter with a current source load for high gain. Pole splitting compensation is provided by C1 to achieve unity gain bandwidth of about 10 MHz. Internal compensation is sufficient with closed-loop gain down to about $A_V = 25$.

The output stage is a complementary common-collector class AB composite. The upper, or current sourcing section, is a Darlington emitter follower Q12 and Q13. The lower, or current sinking, section is a composite PNP made up of Q14, Q15, and Q9. Normally, this type of PNP composite has low f_t and excessive delay caused by the lateral PNP transistor Q9. The usual result is poor unity gain bandwidth and probable oscillation on the negative half of the output waveform. The traditional fix has been to add an external series

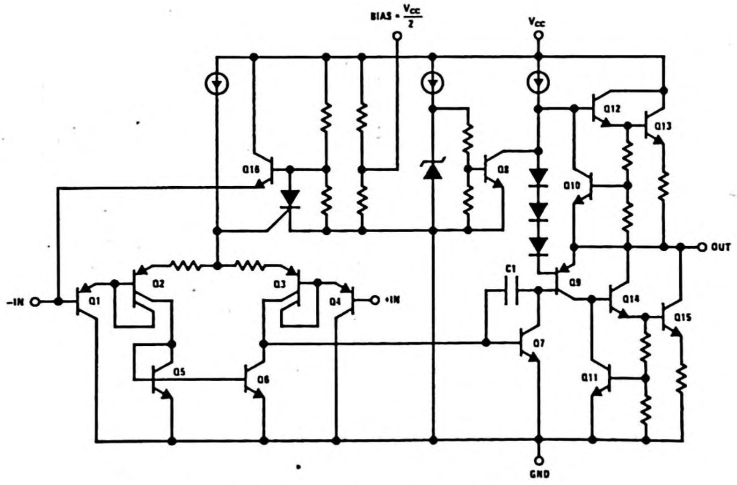


FIGURE 1. Simplified Schematic Diagram

RC network from output to ground to reduce loop gain of the composite PNP and so prevent the oscillation. In the LM377 series amplifiers, Q9 is made a field-aided lateral PNP to overcome these performance limitations and so reduce external parts count. There is no need for the external RC network, no oscillation is present on the negative half cycle, and bandwidth is better with this output stage. Q10 and Q11 provide output current limiting at about 1.3A, and there is internal thermal limiting protection at 150°C junction temperature. The output may be ac shorted without problem; and, although not guaranteed performance, dc shorts to ground are acceptable. A dc short to supply is destructive due to the thermal protection circuit which pulls the output to ground.

To achieve a stable dc operating point, it is desirable to close the feedback loop with unity dc gain. To achieve this simultaneously with a high ac gain normally requires a fairly large bypass capacitor, C1, in *Figure 2.*

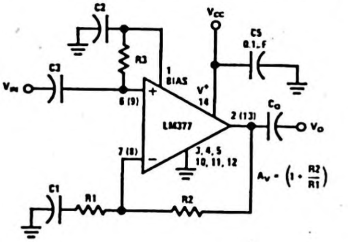


FIGURE 2. Non-Inverting Amplifier Connection

Establishing the initial charge on this capacitor results in a turn-on delay. An additional capacitor, C2, is normally required to supply a ripple-free reference to set the dc operating point. To achieve good supply rejection X_{C2} is normally made much smaller than a series resistor from the bias divider circuit (R_S in *Figure 3*). Where a supply rejection of 40 dB is required with 40 dB closed-loop gain, 80 dB ripple attenuation is required of R_S C2. The turn-on time can be calculated as follows:

$$\text{PSRR} = \frac{R_S - jX_{C2}}{X_{C2}} \approx \frac{R_S}{X_{C2}} = \omega\,RC = \omega T$$

$$T = \frac{\text{PSRR}}{\omega} = \frac{80\text{ dB}}{2\pi\ 120\text{ Hz}} = \frac{10^4}{754} = 13.3\text{ sec}$$

$$t_{ON} \approx \frac{T}{3} = 4.5\text{ seconds to small signal operation}$$

$$t_{ON} \approx 3T = 40\text{ seconds to full output voltage swing}$$

The 3T delay might normally be considered excessive! The LM377 series amplifiers incorporate active turn-on circuitry to eliminate the long turn-on time. This circuitry appeared in *Figure 1* as Q16 and an accompanying SCR; it is repeated and elaborated in *Figure 3.* In operation, the turn-on circuitry charges the external capacitors, bringing output and input levels to $V_{CC}/2$, and then disconnects itself leaving only the $V_{CC}/2$ divider R_B/R_B in the circuit.

The turn-on circuit operation is as follows. When power is applied, approximately $V_{CC}/2$ appears at the base of Q16, rapidly charging C1 and C2 via a low emitter-follower output impedance and series resistors of 3k and 1k. This causes the emitters of the differential input pair to rise to $V_{CC}/2$, bringing the differential amp Q3 and Q4 into balance. This, in turn, drives Q3 into conduction. Transistors Q2 and Q3 form an SCR latch which then triggers and clamps the base of Q16 to

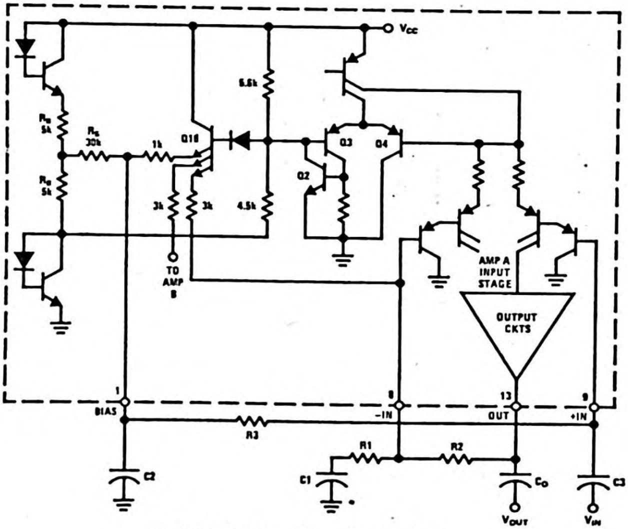


FIGURE 3. Internal Turn-On Circuitry

ground, thus disabling the charging circuit. Once the capacitors are charged, the internal voltage divider R_B/R_B maintains the operating point at $V_{CC}/2$. Using C2 = 250µF, the t_{ON} = 3T ≈ 0.3 seconds and PSRR ≈ 75 dB at 120 Hz due to the 30k resistor R_S. Using C2 = 1000µF, PSRR would be 86 dB. The internal turn-on circuit prevents the usual "pop" from the speaker at turn-on. The turn-off period is also pop-free as there is no series of pulses of active gain often seen in other similar amplifiers.

Note that the base of Q4 is tied to the emitters of only one of the two input circuits. Should only one amplifier be in use, it is important that it be that with input at pins 8 and 9.

EXTERNAL BIASING CONNECTION

The internal biasing is complete for the inverting gain connection of *Figure 4* except for the external C2 which provides power supply rejection. The bias terminal 1 may be connected directly to C2 and the non-inverting input terminals 6 and 9. Normal gain-set feedback connections to the inverting inputs plus input and output coupling capacitors complete the circuitry. The output will Q up to $V_{CC}/2$ in a fraction of one second.

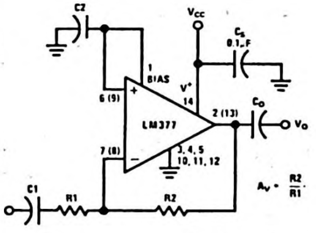


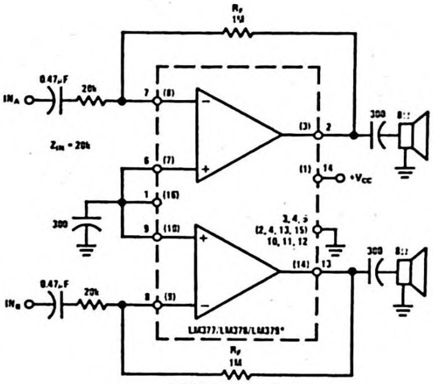
FIGURE 4. Inverting Amplifier Connection

The non-inverting circuit of *Figure 2* is only slightly more complex, requiring the input return resistor R3 from input to the bias terminal and additional input capacitor C3. C1 must remain in the circuit at the same or larger value than in *Figure 4*.

AUDIO AMPLIFIER APPLICATIONS

2/4/6 Watt Stereo Amplifier

The obvious and primary intended application is as an audio frequency power amplifier for stereo or quadraphonic music systems. The amplifier may be operated in either the non-inverting or the inverting modes of *Figures 2 and 4*. The inverting circuit has the lowest parts count so is most economical when driven by relatively low-impedance circuitry. *Figure 5* shows the total parts count for such a stereo amplifier. The feedback resistor value of 1 meg in *Figure 5* is about the largest practical value due to an input bias current max of approximately 1/2µA (100 nA typ). This will cause a −0.1 to 0.5V shift in dc output level, thus limiting peak negative signal



*(LM379 pin nos. in parenthesis)

	LM377	LM377/LM378	LM379
P_O =	2W/CH	3W/CH	4W/CH
e_{in} =	80 mV max	98 mV max	113 mV max
A_V =	50	50	50
V_{CC} =	18V	24V	28V

FIGURE 5. Inverting Stereo Amplifier

swing. This output voltage shift can be corrected by the addition of series resistors (equal to the R_F in value) in the + input lines. However, when this is done, a potential exists for high frequency instability due to capacitive coupling of the output signal to the + input. Bypass capacitors could be added at + inputs to prevent such instability, but this increases the parts count equal to that of the non-inverting circuit of *Figure 6* which has a superior input impedance. For applications utilizing high impedance tone and volume controls, the non-inverting connection will most surely be used.

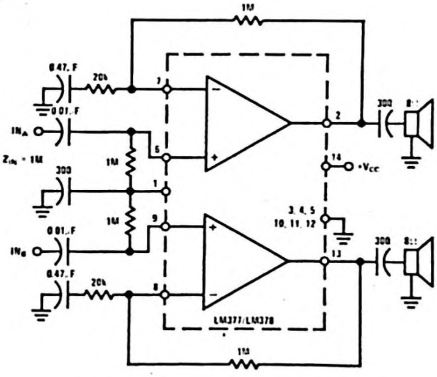
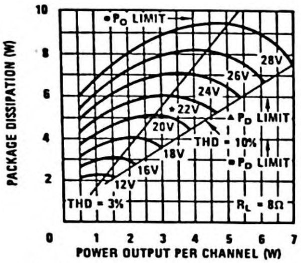


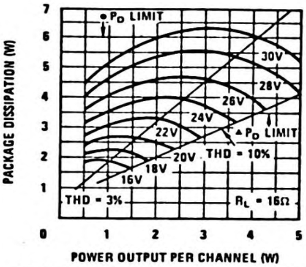
FIGURE 6. Non-Inverting Stereo Amplifier

The prime limitations on output power of the LM377 and LM378 will be the type of heat sink employed, supply voltage, and load resistance. Reference to the data sheet curves will indicate the most efficient supply voltages to use for specific power output levels with 8 or 16Ω loads. The pertinent curves are reproduced in *Figures 7 through 10*. For other conditions $P_D = V_{CC}^2/20\ R_L$. At high power out, efficiency exceeds 50%



- ● Approx. P_O limit acc't. 0.7A rms internal current limit at oper. die temp.
- ▲ P_D limit for LM377/LM378 on PC board w/Staver V7-1 heat sink.
- ■ P_D limit for LM377/LM378 on PC board (2.5 sq. in. Cu)
- ★ Safe limit for LM377.

FIGURE 7. Device Dissipation for 8Ω Load



- ● P_D limit LM377/LM378 on PC board w/Staver V7-1.
- ▲ P_D limit LM377/LM378 on PC board.

FIGURE 8. Device Dissipation for 16Ω Load

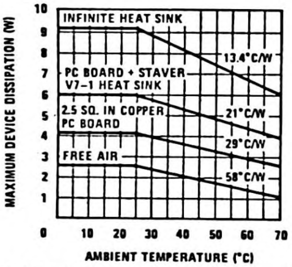


FIGURE 9. LM377/LM378 Power Derating

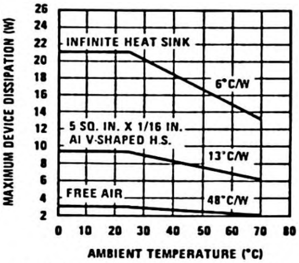


FIGURE 10. LM379 Power Derating

and dissipation drops below output power. A dual 2W amplifier must then dissipate about 4.0W with an 18V supply or 4.9W with a 20V supply when $R_L = 8\Omega$. Normally, one would choose the 18V supply for lower dissipation; however, the 20V supply allows reduced distortion levels or considerably higher powers. A dual 4W amplifier will dissipate about 8W with a 26V supply. This is above the dissipation limit for an LM378 with normal heat sink. Accordingly, a fairly efficient heat sink must be employed in order to allow full 8W continuous output from the LM378 *(Figure 9)*. The recommended heat sinks are listed in Table I with measured power output levels at $V_S = 18$ to 29V for LM377 and LM378 (observe voltage limits on LM377) with 8 or 16Ω load.

POWER OUTPUT PER CHANNEL (BOTH CHANNELS DRIVEN) BEFORE CLIPPING

Power dissipation vs power output/channel (both channels driven) is indicated in *Figures 7 and 8* for load resistances of 8 and 16Ω.

Limiting points to keep in mind, noted on *Figures 7 and 8,* are 4W package dissipation limit for LM377/LM378 when soldered to PC board with 2.5 sq. in. copper, 6W limit when a Staver V7-1 heat sink is added, and internal current limit at about 1.5A peak at 25°C die temperature reducing to about 1A peak at operating die temperature. This results in an approximate P_O = 4W/channel limit for $R_L = 8\Omega$. The onset of clipping occurs just to left of the THD = 3% line in *Figures 7 and 8.*

The overall result is that the LM377 and LM378 with practical heat sinks, are limited to operation below package dissipation of 6W and below P_O = 4W/channel when $R_L = 8\Omega$. Thus maximum P_O = 3W/channel before clipping or 4W/channel at about 6% THD with either device at $V_{CC} = 22V$. With a 16Ω load the LM378 can deliver 4W/channel with 3–4% THD when V_{CC} = 29–30V. The LM379 is limited to P_O = 4–5W/channel before clipping at V_{CC} = 26–28V, $R_L = 8\Omega$, or 4W/channel at $V_{CC} = 30V$, $R_L = 16\Omega$. P_O = 6W occurs at 8–10% THD with V_{CC} = 28–30V and $R_L = 8\Omega$.

TABLE I. Continuous Power Out (Both Channels)

HEAT SINK	LM377 $R_L = 8\Omega$			LM378 $R_L = 16\Omega$		
	$V_S = 18V$	$V_S = 20V$	$V_S = 22V$	$V_S = 24V$	$V_S = 26V$	$V_S = 29V$
PC Board, 40°C/W	2.2W	0.8W	0.3W	2.2W	1W	0.3W
PC Board and Staver V7-1, 12°C/W	2.2W	2.7W	3.1W	2.2W	2.5W	3.3W

Note that the P_O = 6W rating on LM379 is at 10% THD where peak current is similar to that at P_O = 4W, V_{CC} = 26V, R_L = 8Ω.

What really exists then are power out before clipping of 2W/channel at V_{CC} = 18V with PC board mounting, 3W/channel at V_{CC} = 22V with maximum practical heat sinking on either LM377 or LM378, and 4W/channel at $V_{CC} \geq$ 26V for LM379.

Device dissipation vs ambient temperature with several heat sink types is indicated in *Figures 9 and 10* for convenience of matching heat sink capacity to the circuit needs. In those cases where heat sink capacity is inadequate for device dissipation requirements, the internal thermal limit circuitry will automatically limit device dissipation on signal peaks. The result is similar to peak clipping in its effect and causes severe distortion. The device can provide momentary peak power output in excess of the maximum heat sink limited steady-state levels for a second or so depending upon the margin between maximum steady-state level and the actual average power level prior to the peak demand. Once in thermal limiting, clipping occurs on each positive and/or negative half cycle of a steady waveform.

In the majority of audio amplifier applications, the heat sinking can be considerably smaller due to the approximately 30 dB ratio between rms and peak power levels in music and speech. If we assume willingness to accept clipping at peak levels 20 dB above average level, then average power levels will be 0.2–0.3W/channel in LM377 and LM378. Heat sink requirements are thus significantly reduced as these peak levels occur less than 10% of time periods of several seconds duration. Thus the circuit does not go into thermal overload even though the heat sink is designed for 3W dissipation (LM377 operating at 0.3W/channel, V_{CC} = 18V).

STABILIZATION

The LM377 series amplifiers are internally stabilized so external compensation capacitors are not required. The high Gain x BW provides a bandwidth greater than 50 kHz as seen in *Figure 11.* These amplifiers are, however, not intended for closed loop gain below 25. The typical Bode plot of *Figure 12* shows a phase margin of 70° for gain of 5.6 (15 dB) which is stable. At unity gain the phase margin is less than 30° or marginally stable. This margin may vary considerably from device to device due to variation in Gain x BW.

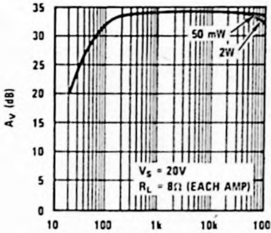


FIGURE 11. Frequency Response of the Stereo Amp of Figure 5

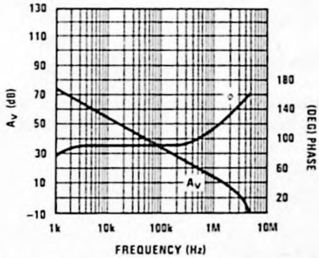


FIGURE 12. Open Loop Bode Plot (Approximately Worst Case)

As with any amplifier of high Gain x BW, careful circuit layout is important to insure unconditional stability. Specifically, coupling to the non-inverting inputs from output and feedback elements should be minimized. The supply should also be bypassed with an 0.05–0.1μF ceramic or 0.47μF mylar capacitor within 2 inches of the IC terminals. One layout which accomplishes this is illustrated in *Figure 13.* The signal circuits are symmetrically arranged on either side of the IC package.

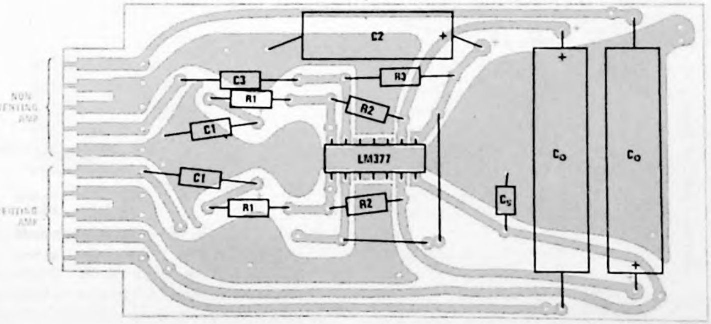


FIGURE 13. Parts Layout for LM377/LM378 Dual Amplifier

Operation may be either inverting or non-inverting, therefore, one side is shown connected each way. Normally both sides would be connected in the same sense. The PC board art-work is shown in *Figure 14.* The edge connector could, of course, be omitted and wire connections made to appropriate contacts at either end. This layout is satisfactory for gain as low as 10. Below $A_V = 10$, instability may occur.

Ground and power connections must be adequate to handle the 1 to 2A peak supply and load currents. Ground loops can be especially troublesome because of these high currents. The load return line should be connected directly to the ground pins of the package on one side and/or the input and feedback ground lines should be connected directly to the ground pins (possibly on the other side of the package). Note that the layout in *Figure 14* has a connection at center of the card edge connector for signal ground and two separate, flanking, terminals for the load and power grounds. The signal ground should not be connected so as to intercept any output signal voltage drop due to resistance between IC ground and load ground.

10–12 Watt Channel Boosted Amplifier

Where more power output is desired, the simple booster circuit of *Figure 15* allows power output of 10W/channel when driven from the LM378. The circuit is exceptionally simple, and the output exhibits lower levels of crossover distortion than does the LM378 alone. This is due to the inclusion of the booster transistors within the feedback loop. At signal levels below 20 mW, the LM378 supplies the load directly through the 5Ω resistor to about 100 mA peak current. Above this level, the booster transistors are biased ON by the load current through the same 5Ω resistor.

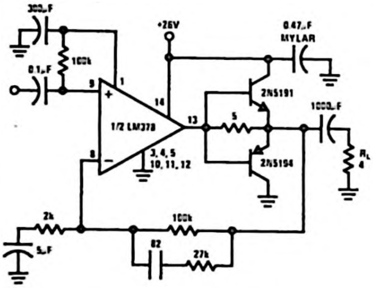


FIGURE 15. 10 Watt Power Amplifier

The response of the 10W boosted amplifier is indicated in *Figure 16* for power levels below clipping. Distortion is below 2% from about 50 Hz to 30 Hz. Fifteen watts rms power is available at 10% distortion; however, this represents extreme clipping. Although the LM378 delivers little power, its heat sink must be adequate for about 3W package dissipation. The output transistors must also have an adequate heat sink.

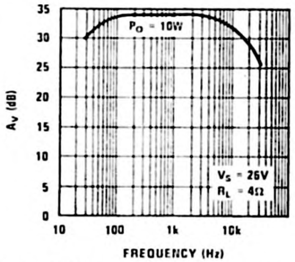


FIGURE 16. 10 Watt Bosted Amplifier, Frequency Response

The circuit of *Figure 17* achieves about 12W/channel output prior to clipping. Power output is increased because there is no power loss due to effective series resistance and capacitive reactance of the output coupling capacitor required in the single supply circuit. At power up to 10W/channel, the output is extremely clean, containing less than 0.2% THD midband at 10W. The bandwidth is also improved due to absence of the output coupling capacitor. The frequency response and distortion are plotted in *Figures 18 and 19* for low and high power levels. Note that the input coupling capacitor is still required, even though the input may be ground

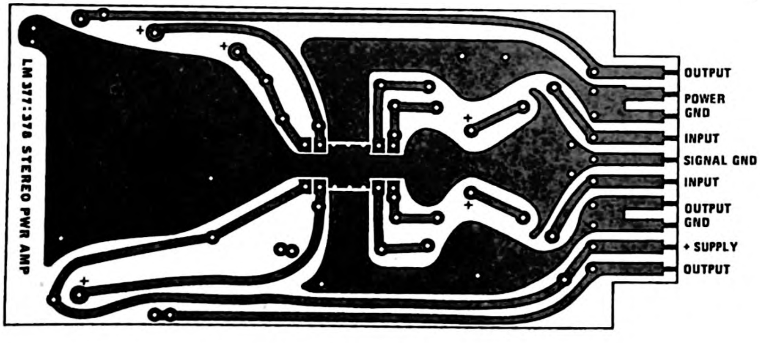


FIGURE 14. PC Board for LM377/LM378 Dual Amplifier

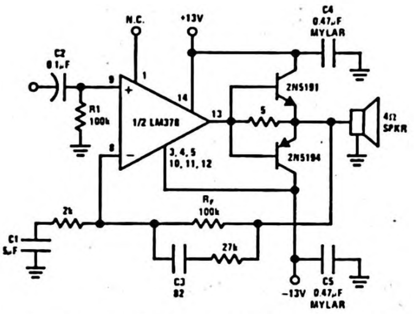


FIGURE 17. 12 Watt Low-Distortion Power Amplifier

referenced, in order to isolate and balance the dc input offset due to input bias current. The feedback coupling capacitor, C1, maintains dc loop gain at unity to insure zero dc output voltage and zero dc load current. Capacitors C1 and C2 both contribute to decreasing gain at low frequencies. Either or both may be increased for better low frequency bandwidth. C3 and the 27k resistor provide increased high frequency feedback for improved high frequency distortion characteristics. C4 and C5 are low inductance mylar capacitors connected within 2 inches of the IC terminals to ensure high frequency stability. R1 and R_f are made equal to maintain $V_{OUT\ DC} = 0$. The output should be within 10 to 20 mV of zero volts dc. The internal bias is unused; pin 1 should be open circuit. When experimenting with this circuit, use the amplifier connected to terminals 8, 9 and 13. If using only the amplifier on terminals 6, 7 and 2, connect terminals 8 and 9 to ground (split supply) to cause the internal bias circuits to disconnect.

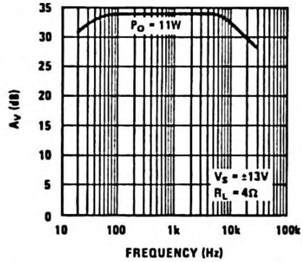


FIGURE 18. Response for Amplifier of Figure 17

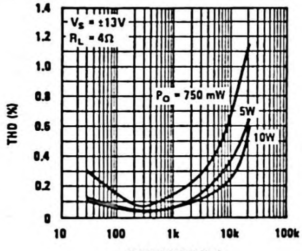


FIGURE 19. Distortion for Amplifier of Figure 17

Bridge Amplifier

The LM377 series amplifiers are equally useful in the bridge configuration to drive floating loads, which may be loudspeakers, servo motors or whatever. Double the power output can be obtained in this connection, and output coupling capacitors are not required. Load impedance may be either 8 or 16Ω in the bridge circuit of *Figure 20.* Response of this circuit is 20 Hz to 160 kHz as shown in *Figure 21* and distortion is 0.1% midband at 4W rising to 0.5% at 10 kHz and 50 mW output *Figure 22.* The higher distortion at low power is due to a small amount of crossover notch distortion which becomes more apparent at low powers and high frequencies. The circuit of *Figure 23* is similar except for higher input impedance. In *Figure 23,* the signal drive for the inverting amplifier is derived from the feedback voltage of the non-inverting amplifier. Resistors R1 and R3 are the input and feedback resistors for A_2, whereas R1 and R2 are the feedback network for A_1. So far as A_1 is concerned, R2 sees a virtual ground at the (−) input to A_2; therefore, the gain of A_1 is (1 + R2/R1). So far as A_2 is concerned, its input signal is the voltage appearing at the (−) input to A_1. This equals that at the (+) input to A_1. The driving point impedance at the (−) input to A_1 is very low even though R2 is 100k. A_1 can be considered a unity gain amplifier with internal R = R2 = 100k and R_L = R1 = 2k. Then the effective output resistance of the unity gain amplifier is:

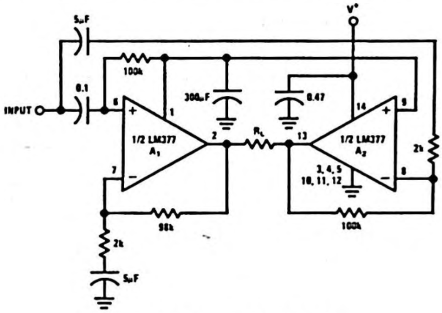


FIGURE 20. 4-Watt Bridge Amplifier

$$R_{OUT} = \frac{R_{INTERNAL}}{A_{OL}/A_{\beta}} = \frac{100k}{600/1} = 167\Omega$$

Layout is critical if output oscillation is to be avoided. Even with careful layout, capacitors C1 and C2 may be required to prevent oscillation. With the values shown, the amplifier will drive a 16Ω load to 4W with less than 0.2% distortion midband, rising to 1% at 20 kHz *(Figure 24).* Frequency response is 27 Hz to 60 kHz as shown in *Figure 25.* The low frequency roll off is due to the double poles C3 R3 and C4 R1.

Power Oscillator

One half of an LM377 may be connected as an oscillator to deliver up to 2W to a load. *Figure 26* shows a Wein bridge type of oscillator with FET amplitude stabilization in the negative feedback path. The circuit employs

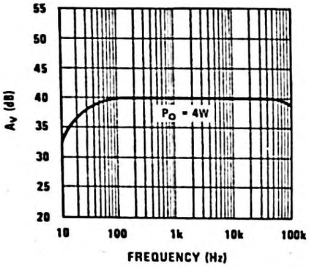


FIGURE 21. Frequency Response, Bridge Amp of Figure 20

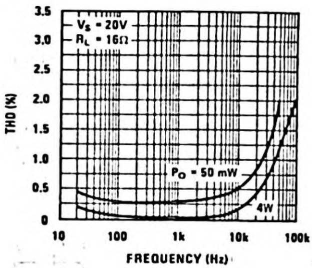


FIGURE 22. Distortion for Bridge Amp of Figure 20

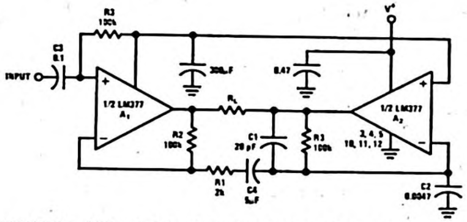


FIGURE 23. 4-Watt Bridge Amplifier with High Input Impedance

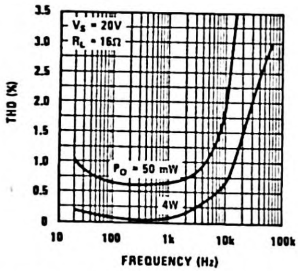


FIGURE 24. Distortion for Bridge Amp of Figure 23

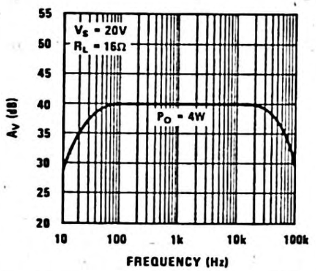


FIGURE 25. Frequency Response, Bridge Amp of Figure 23

internal biasing and operates from a single supply. C3 and C6 allow unity gain dc feedback and isolate the bias from ground. Total harmonic distortion is under 1% to 10 kHz, and could possibly be improved with careful adjustment of R5. The FET acts as the variable element in the feedback attenuator R4 to R6. Minimum negative feedback gain is set by the resistors R4 to R6, while the FET shunts R6 to increase gain in the absence of adequate output signal. The peak detector D2 and C8 senses output level to apply control bias to the FET. Zener diode D1 sets the output level although adjustment could be made if R9 were a potentiometer with R8 connected to the slider. Maximum output level with the values shown is 5.3V rms at 60 Hz. C7 and the attenuator R7 and R8 couple 1/2 the signal of the FET drain to the gate for improved FET linearity and low distortion. The amplitude control loop could be replaced by an incandescant lamp in non-critical circuits *(Figure 27)* although dc offset will suffer by a factor of about 3 (dc gain of the oscillator). R10 matches R3 for improved dc stability; and the network R11, C9 increases high frequency gain for improved stability. Without this RC, oscillation may occur on the negative half cycle of output waveform. A low inductance capacitor, C5, located directly at the supply leads on the package is important to maintain stability and prevent high frequency oscillation on negative half cycle of the output waveform. C5 may be 0.1μF ceramic, or 0.47μF mylar. Layout is important; especially take care to avoid ground loops as discussed in the section on amplifiers. If high frequency instability still occurs, add the R12, C10 network to the output.

Figure 27 shows the use of the LM377 to drive a small 60 Hz two phase servo motor up to 3W per phase. Applications such as a constant (or selectable) speed phonograph turntable drive are adequately met by this circuit. A split supply is used to simplify the circuit, reduce parts count, and eliminate several large bypass capacitors. An incandescent lamp is used in a simple amplitude stabilization loop. Input dc is minimized by balancing dc resistance at + and − amplifier inputs (R1 = R3 and R6 = R8). High frequency stability is assured by increasing closed-loop gain from approximately 3 at 60 Hz to about 30 above 40 kHz with the network consisting of R3, R4 and C3. The interstage

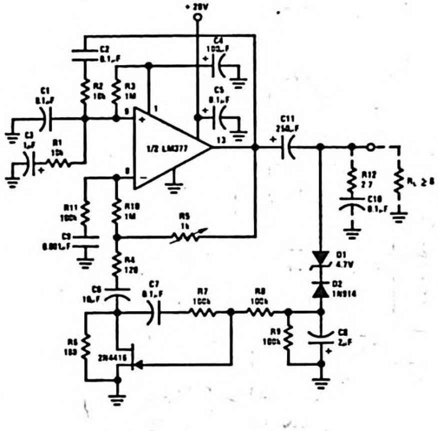


FIGURE 26. Wein Bridge Power Oscillator

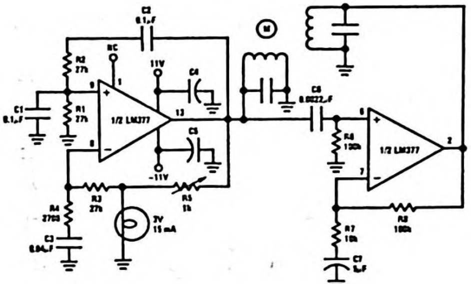
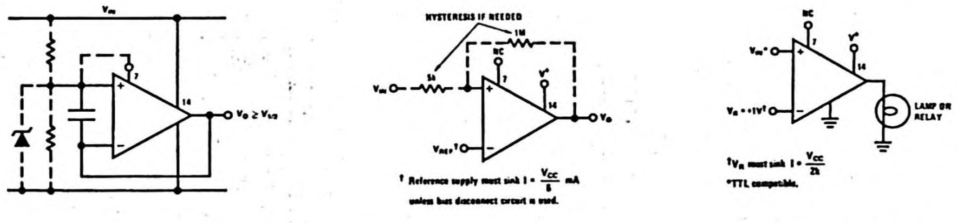


FIGURE 27. Two-Phase Motor Drive



† Reference supply must sink $I = \frac{V_{CC}}{5}$ mA unless bias disconnect circuit is used.

†V_R must sink $I = \frac{V_{CC}}{2k}$

*TTL compatible.

Supply Regulator

Power Comparator

Lamp or Relay Driver

FIGURE 28. Miscellaneous Applications

coupling C6 R6 network shifts phase by 85° at 60 Hz to provide the necessary two phase motor drive signal. The gain of the phase shift network is purposely low so that the buffer amplifier will operate at a gain of 10 for adequate high frequency stability. As in other circuits, the importance of supply bypassing, careful layout, and prevention of output ground loops is to be stressed. The motor windings are tuned to 60 Hz with shunt capacitors. This circuit will drive 8Ω loads to 3W each.

MISCELLANEOUS APPLICATIONS

A number of non-audio applications come to mind, such as a dual power supply regulator, power comparator, and relay or lamp driver as shown in *Figure 28.* The degree of practicality of any of these will be limited by the special characteristics of the LM377/LM378/LM379 chip. Limitations are a higher than usual input-offset voltage and temperature drift (not troublesome in the intended capacitor coupled applications). As the devices are not unity-gain stable, a shunt capacitor across the inputs is needed in low gain applications such as the supply regulator. The output saturation voltage is 2 to 3V, thus internal power dissipation is non-negligible in relay or lamp driver applications.

As a lamp driver, the LM377 is limited to those applications where its dissipation is outweighed by the advantage of the internal current limiting. The real advantage of this current limiting is that the lamp driver cannot be destroyed by a shorted lamp *if* the lamp common terminal is ground (the LM377 will not survive an output short to supply).

In any of these applications, recall that the internal turn-on circuit will supply current out the (−) input until inputs are raised to $V_{CC}/2$.

COMPLETE SYSTEMS

The LM377 to LM379 dual power amplifiers are useful in table or console radios, phonographs, tape players, intercoms, or any low to medium power music systems. Several examples of complete audio systems are described. One is a 2-channel audio system for radio, phono, and tape playback. The other is rear channel amplifier pair for extracting "ambience" information from stereo signals and amplifying for 4-channel sound.

Figures 29 to 30 describe the complete electronic section of a 2-channel sound system with inputs for AM

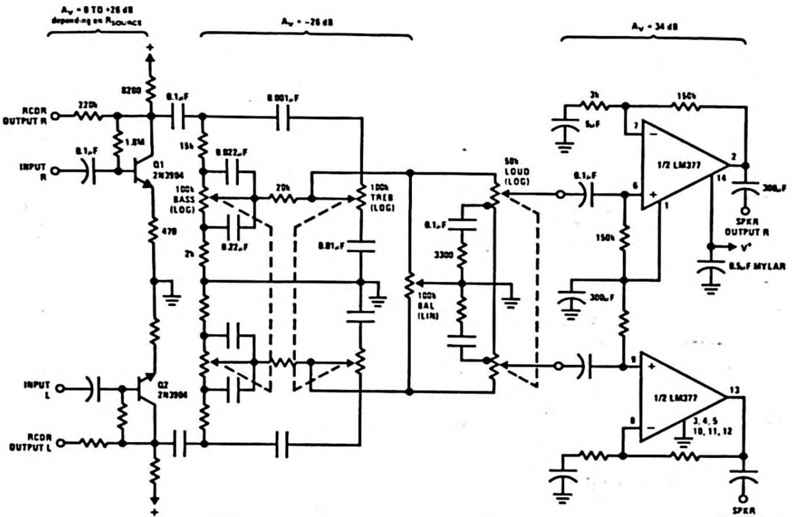

A_V = 0 TO +26 dB depending on R_SOURCE
A_V = −26 dB
A_V = 34 dB
+
8200
RCDR OUTPUT R
220k
1.8M
0.1μF
INPUT R
Q1 2N3904
0.1μF
0.001μF
15k
0.022μF
100k BASS (LOG)
20k
100k TREB (LOG)
470
2k
0.22μF
0.01μF
0.1μF
3300
100k BAL (LIN)
50k LOUD (LOG)
0.1μF
3k
5μF
150k
7
1/2 LM377
2
14
6
1
300μF
SPKR OUTPUT R
150k
V+
0.5μF MYLAR
300μF
9
1/2 LM377
13
8
3, 4, 5 10, 11, 12
INPUT L
Q2 2N3904
RCDR OUTPUT L
+
SPKR OUTPUT L

FIGURE 29. Two-Channel Power Amplifier and Control Circuits

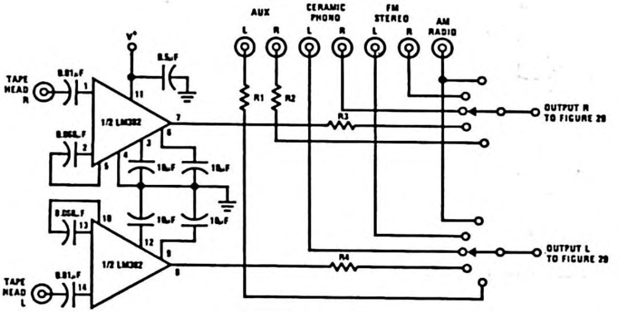

AUX
CERAMIC PHONO
FM STEREO
AM RADIO
L
R
L
R
L
R
V+
0.5μF
TAPE HEAD R
0.01μF
1
11
1/2 LM382
7
0.068μF
2
6
3
4
5
10μF
10μF
R1
R2
R3
OUTPUT R TO FIGURE 29
0.068μF
10
13
10μF
10μF
12
9
1/2 LM382
8
R4
OUTPUT L TO FIGURE 29
TAPE HEAD L
0.01μF
14

FIGURE 30. Two-Channel Tape-Playback Amplifier and Signal Switching

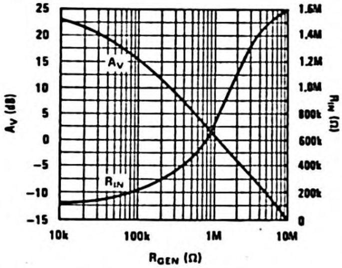


FIGURE 31. A_V and R_{IN} for Input Stage of Figure 28.

radio, stereo FM radio, phono, and tape playback. *Figure 29* combines the power amplifier pair with loudness, balance, and tone controls. The tone controls allow boost or cut of bass and/or treble. Transistors Q1 and Q2 act as input line amplifiers with the triple function of (1) presenting a high input impedance to the inputs, especially ceramic phono; (2) providing an amplified output signal to a tape recorder; and (3) providing gain to make up for the loss in the tone controls. Feedback tone controls of the Baxandall type employing transistor gain could be used; but then, with the same transistor count, the first two listed functions of Q1 Q2 would be lost. It is believed that this circuit represents the lowest parts count for the complete system. *Figure 30* is the additional circuitry for input switching and tape playback amplifiers. The LM382 with capacitors as shown provides for NAB tape playback compensation. For further information on the LM382 or the similar LM381 and LM387, refer to the data sheets.

Figure 31 shows the relationship between signal source impedance and gain or input impedance for the amplifier stage Q1 Q2. Stage gain may be set at a desired value by choice of either the source impedance or insertion of resistors in series with the inputs (as R1 to R4 in *Figure 30*). Gain is variable from −15 to +24 dB by choice of series R from 0 to 10 meg. Gain required for e_{IN} = 100 to 200 mV (approximate value of recovered audio from FM stereo or AM radio) is about 18 to 21 dB overall for 2W into an 8Ω speaker at 1 kHz or 21 to 24 dB for 4W.

The rear channel "ambience" circuit of *Figures 32 and 33* can be added to an existing stereo system to extract a difference signal (R − L or L − R) which, when combined with some direct signal (R or L), adds some fullness, or "concert hall realism" to reproduction of recorded music. Very little power is required at the rear channels, hence an LM377 will suffice for most "ambience" applications. The inputs are merely connected to the existing speaker output terminals of a stereo set, and two more speakers are connected to the ambience circuit outputs. Note that the rear speakers should be connected in opposite phase to those of the front speakers, as indicated by the +/− signs on the diagram of *Figure 32*.

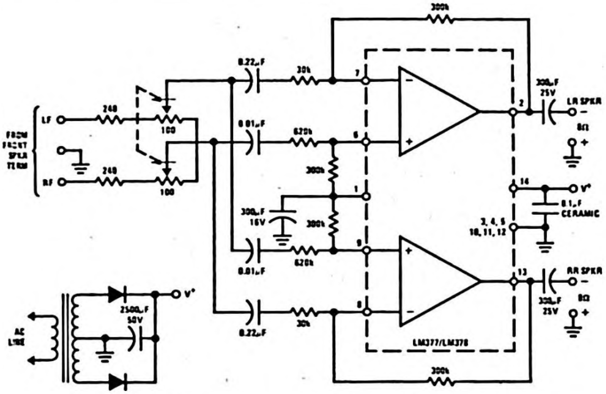

300k
0.22µF
30k
7
2
300µF
25V
LR SPKR
8Ω
LF
240
100
FROM FRONT SPKR TERM
RF
240
100
0.01µF
620k
6
300k
1
14
V+
0.1µF CERAMIC
300µF 16V
300k
3, 4, 5
10, 11, 12
9
0.01µF
620k
13
RR SPKR
8Ω
300µF 25V
8
0.22µF
30k
V+
2500µF 50V
AC LINE
LM377/LM378
300k

FIGURE 32. Rear Speaker Ambience (4-Channel) Amplifier

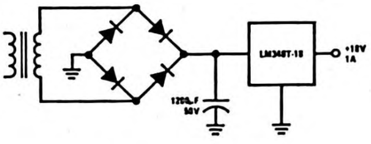

LM340T-18
+18V 1A
1200µF 50V

FIGURE 33. Alternate Power Supply for Ambience Circuit

APPENDIX: INTERPRETATION OF P_O vs P_D CURVES

The angled straight lines on the curves of *Figures A-1* and *A-2* indicate the loci of operating points where clipping occurs. When THD = 3%, the output waveform has noticeable clipping. The THD = 10% line is an operating area of severe clipping. Clipping begins just to the left of the THD = 3% line so this discussion deals only with operation up to, but not quite at, the 3% line.

The three circles on *Figure A-1* are the data sheet spec limits for LM377/LM378/LM379; that is, 2, 4 and 6W/channel with 20, 24 and 28V supplies respectively. Observe that the 2W point is well to the left of the THD = 3% line, or well under clipping. The 4 and 6W points march progressively further toward the THD = 10% line, or deeper into clipping. Also note the dissipation limits in *Figure A-3* for LM377/LM378 on PC board and on PC board with addition of Staver V7-1 heat sink are 4.1 and 6W respectively. These represent the limits for commonly available heat sinks for the DIP package. No doubt a special heat sink fabricated "just-so" could extend the 6W limit to 6 1/2 or 7W, but we'll stop at 6W. Data have been added to *Figure A-4* showing LM379

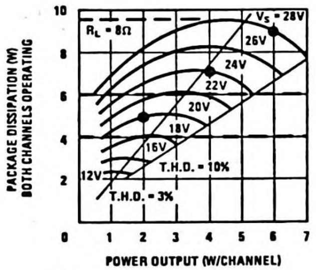


FIGURE A-1. Power Dissipation vs Power Output

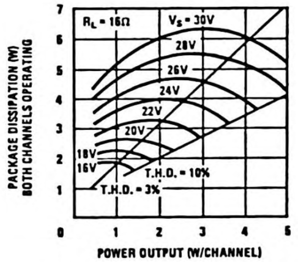


FIGURE A-2. Power Dissipation vs Power Output

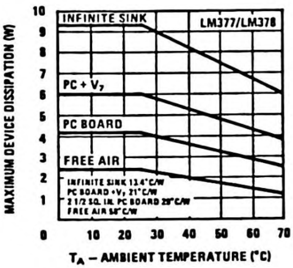


FIGURE A-3. Maximum Dissipation vs Ambient Temperature

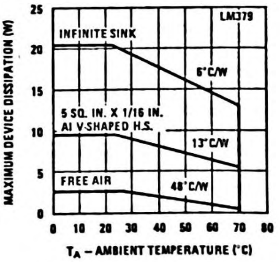


FIGURE A-4. Maximum Dissipation vs Ambient Temperature dissipation with a simple small heat sink. This heat sink is 5 square inches of 1/16" aluminum in a modified V shape which is clamped to the sink side of the LM379.

These practical limits are transferred to *Figure A-1* as horizontal dashed lines across the P_O vs P_D curves at 4.1, 6 and 9.6W. We see that the reference points, 2W at 20V and 4W at 24V, are above the practical P_D limits for PC board alone and for PC board with Staver V7-1 heat sink. The third point, 6W at 28V is OK so far. What this means is that, in bench testing, the LM377 must have better than PC mounting to meet data sheet specified operation; and the LM378 will likely not meet data sheet specified operation with any practical heat sink. The LM377 will meet specs with the PC board plus Staver heat sink. The LM378 will meet specs with a 7W heat sink, but not with normally available heat sinks. The LM379 will meet specs with the 5 square inch sink described above. What may be most important, however, is performance short of clipping. For that reason, the remainder of this section will deal only with rms power at levels below clipping.

Returning to *Figure A-1*, it appears that the LM377 or LM378 with only PC board heat sinking will be able to deliver 2.2W/channel into 8Ω with an 18V supply. But, if the supply is raised to 20V, the P_D limit is exceeded at 1W. With PC board plus a Staver heat sink, the LM377/LM378 will deliver 3.2W/channel with 22V supply, yet raising the supply to 24V limits us to P_O = 1.9W/channel.

So why use a LM378 if the supply limit is 22V? The reason is that few supplies are regulated in the consumer world. This means that if the supply is 22V under full load, the no-signal supply may rise 10% or more; and the variations in line voltage may add another 10% for a total supply maximum of at least 26.5V. Therefore the LM377 is only recommended for full-load operating supplies of less than 20V. But remember, it can deliver over 2W/channel with an 18V supply on a PC board, or 2 1/2W/channel with 20V supply and Staver heat sink. The LM378 will provide 3.2W/channel with 22V supply and PC board plus Staver heat sinking. With poorly regulated supplies over 20V or with 16Ω load, the LM378 is the obvious choice as higher supply voltages are required to obtain high powers with 16Ω loads. Although no greater power is available than with 8Ω loads.

There is no reasonable P_D limit on the LM379 as we can dissipate nearly 20W with adequate practical heat sinking and 9.6W with minimal sink. Then V_{CC} is the limit, say 30V. That would put us off the graph on *Figure A-1* at about 5.5W/channel or at 3W/channel with 16Ω load. Even at 8Ω and 30V, package dissipation is only 11W, or 9.6W with 28V. The kicker is in the data sheet electrical characteristics under current limit; 1.5A typ when T_{TAB} = 25°C. The tab is above 25°C when package dissipation is 9–11W. Still, this is a realistic test for high speed machine testing. In actual use, the current limit moves down to maybe 1.25A or even less. What does this mean? Consider an 8Ω load in power equation, and that 1–1.25A pk is 0.7–0.88A rms.

$$P = I^2 R$$

$$= (0.7)^2\ 8 = (0.5)\ 8 \quad \text{or} \quad = (0.88)^2\ 8 = (0.77)\ 8$$

$$= 4W \qquad\qquad\qquad\qquad = 6.2W$$

Now we have the actual limits at $P_{O(MAX)}$ = 4–6.2W at 8Ω or 8W at 16Ω. Trouble is we are limited to 5W at 28V, 8Ω or 5.5W at 30V, 8Ω and 4W at 16Ω by a 30V operating limit. Current limits could run higher than data sheet typicals; many do, in fact. Then we can get more than 4W/channel as a limit. Since this is a typical spec, there is no guarantee either way.

Note with interest that an LM377 with Staver V7-1 heat sink will deliver 3.2W/channel with 22V supply (but hold it close to 22V or use a LM378) and the LM379 will deliver 5W/channel with a 28V supply. The LM379 is the practical choice because it is easier and probably cheaper to heat sink, and there is more P_D headroom to allow for variations in supply voltage (very important). Also, the better the heat sink on the LM379, the lower the tab temperature, and the higher the operating current limit.

Beyond the limits discussed, the temperature or current limits operate, the peaks are clipped, the waveform remains at peak value for a longer portion of the input cycle, the rms P_O increases, P_D decreases, and rms power approaches peak power.

Here is a summary of the performance the customer may encounter.

TABLE A-1. Max P_O Before Clipping (8Ω Load)

Heat Sink =		PC BOARD (29°C/W)			PC BOARD + V7-1 (21°C/W)				13°C/W SINK		
V_{CC}	=	16	18	19	18	20	22	23	26	28	30
P_O/CH	=	1.5	2.2	1.4	2.2	2.5	3.2	1.9	4.3	5.0	5.5
		├──	──	LM377	──	──┤					
		├──	──	──	LM378	──	──	──┤			
		├──	──	──	──	LM379	──	──	──	──	──┤

LM143 Monolithic High Voltage Operational Amplifier Applications

National Semiconductor
Application Note 127
Sam Ochi
John Flink
April 1976

AN-127 LM143 Monolithic High Voltage Operational Amplifier Applications

INTRODUCTION

The LM143 is a general purpose, high voltage operational amplifier featuring ±40V maximum supply voltage operation, output swing to ±37V, ±38V input common-mode range, input overvoltage protection up to ±40V and slew rate greater than 2V/µs*. Offset null capability plus low input bias and offset currents (8 nA and 1 nA respectively) minimize errors in both high and low source impedance applications. Due to isothermal symmetry of the chip layout, gain is constant for loads $\geq$ 2 kΩ at output levels to ±37V. Because of these features, the LM143 offers advantages not found in other general purpose op amps. The LM143 may, in fact, be used as an improved performance, plug-in replacement for the LM741 in most applications.

This paper describes the operation of the LM143 and presents applications which take advantage of its unique, high voltage capabilities. Obviously, other applications exist where the low input current and high slew rate of the LM143 are useful. (See AN-29 on the LM108). Application tips are included in the appendix to guide the user toward reliable, trouble-free operation.

CIRCUIT DESCRIPTION

A simplified schematic of the LM143, shown in *Figure 1*, illustrates the basic circuit operation. The super-β input transistors(1), Q1 and Q2, are used as emitter followers to achieve low input bias currents. Although these devices exhibit β = 2000–5000, they inherently have a low collector-base breakdown voltage of about 4V. Therefore, active voltage clamps Q3 and Q4 protect Q1 and Q2 under all input conditions including common-mode and differential overvoltage. Other NPNs in the circuit are representative of those found in standard IC op amps, ($\beta \approx 200$, LV_{CEO} = 50–70V).

The input stage differential amplifier Q7 and Q8 with large base width exhibit LV_{CEO} = 90V to 110V and high BV_{EBO} so readily withstand input overvoltages. The total input stage collector current (I_1 = 80µA) is made higher than in most op amps to improve slew rate. Emitter degeneration resistors, R10 and R11, reduce transconductance(2) to limit small signal bandwidth at 1 MHz for a phase margin of 75°. Q16 and Q17 function as active collector loads for Q7 and Q8 and provide differential to single-ended current conversion with full differential gain.

One of the highest breakdown voltages available in standard planar NPN processing is the collector-base, BV_{CBO} which is typically 90V to 120V. To make use of this high voltage capability in the active region, the second stage consists of a cascode (common emitter—common base pair) connection of Q21 and Q23. The internal voltage bias V_{B1}, shunts avalanche-induced leakage current away from the base of Q21, avoiding β multiplication as found in the LV_{CEO} mode. Q23 and emitter follower Q22 are internally biased at a low voltage so the BV_{CEO} mode is impossible. Frequency compensation is achieved with an internal, high voltage capacitor, C_C.

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*An externally compensated version of the LM143, the LM144, offers even higher slew rate in most applications. The LM144 is pin-for-pin compatible with the LM101A.

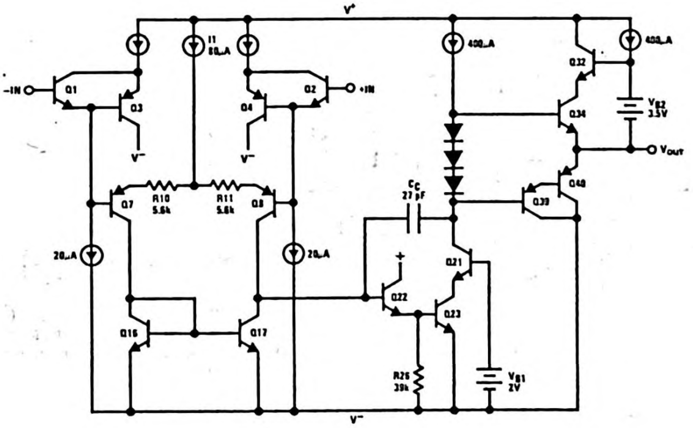


FIGURE 1. LM143 Simplified Schematic

The second stage drives a complementary class AB output stage. A cascode connection of Q32 and Q34 is again employed for high breakdown voltage. The associated voltage bias, V_{B2}, is internally derived. A Darlington PNP pair, Q39 and Q40 with BV_{CEO} = 100V, provides the active pull-down.

HIGH VOLTAGE APPLICATIONS

The following applications make use of the high voltage capabilities of the LM143. As with most general purpose op amps, the power supplies should be adequately bypassed to ground with 0.1µF capacitors.

130 Vp-p Drive to a Floating Load

A circuit diagram using two LM143's to drive up to 130V peak-to-peak is given in *Figure 2.*

A non-inverting voltage amplifier, with a gain of $A_V = 1 + (R2/R1)$, is followed by a unity gain inverter. The load is applied across the outputs of A1 and A2. Therefore, $V_{OUT} = V1 - V2 = V1 - (-V1) = 2V1$. If V1 = 65 Vp-p, then 2V1 = 130 Vp-p.

The above circuit was breadboarded and the results are as follows:

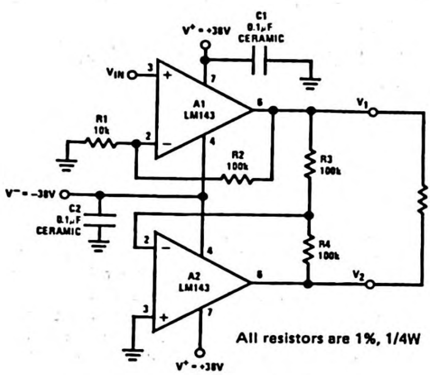
i) Maximum output voltage: 138 Vp-p unclipped into 10 kΩ load

ii) Slew rate: 6V/µs

±34V Common-Mode Range Instrumentation Amplifier

An instrumentation amplifier with ±34V common-mode range, high input impedance and a gain of X1000 is shown in *Figure 3.*

For a differential input signal, V_{IN}, A1 and A2 act as non-inverting amplifiers of gain $A_{V1} = 1 + (2R1/R2)$, where R1 = R3. However, the gain is unity for common-mode signals since voltages V1 and V2 are in phase, and no current flow is developed through R1, R2 and R3. The second stage is simply an op amp connected as a simple differential amplifier of gain, $A_{V2} = (R5/R4)$, where R5 = R7 and R4 = R6. The total gain of the instrumentation amplifier is


V+ = +38V
C1
0.1µF
CERAMIC
VIN
3
+
7
A1
LM143
6
V1
R1
10k
2
−
4
R2
100k
R3
100k
V− = −38V
C2
0.1µF
CERAMIC
RL
2
−
4
R4
100k
A2
LM143
6
V2
3
+
7
V+ = +38V

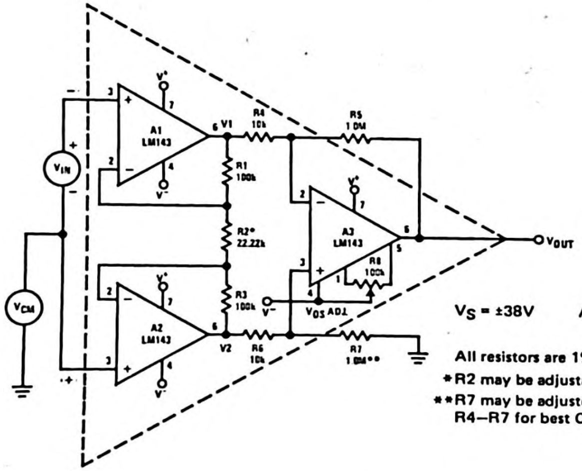
All resistors are 1%, 1/4W

FIGURE 2. 130V Drive Across a Floating Load

$$A_V = \left(1 + \frac{2R1}{R2}\right)\left(\frac{R5}{R4}\right) = \left(1 + \frac{2X100k}{22.22k}\right)\left(\frac{1.0M}{10k}\right)$$

$$= 1000$$

R7 may be adjusted to take up the resistance tolerances of R4, R5 and R6 for best common-mode rejection (CMR). Also, R2 may be made adjustable to vary the gain of the instrumentation amplifier without degrading the CMR.


V+
3
+
7
A1
LM143
6
V1
R4
10k
R5
1.0M
−
+
VIN
2
−
4
V−
R1
100k
R2*
22.22k
2
V+
7
A3
LM143
6
5
3
+
R8
100k
1
4
R3
100k
V−
VOS ADJ
2
−
7
V+
A2
LM143
VCM
3
+
4
V−
6
V2
R6
10k
R7
1.0M**
VOUT

$V_S = \pm 38V$ $\quad A_V = \left(1 + \frac{2\,R1}{R2}\right)\frac{R5}{R4}$ $\quad$ Where: R4 = R6, R5 = R7

All resistors are 1%, 1/4W

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4–R7 for best CMR.

FIGURE 3. Wide Common-Mode Range Instrumentation Amplifier

Laboratory evaluation of this circuit revealed noise and CMR data as follows:

i) Frequency response with 10k load and $A_V = 1000$: −3.0 dB at 8.9 kHz

ii) CMR measurements (common-mode signal of ±34 Vp-p) in *Figure 4*

iii) Noise measurements in *Figure 5*

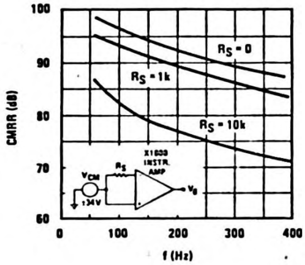


FIGURE 4. Common-Mode Rejection Measurements

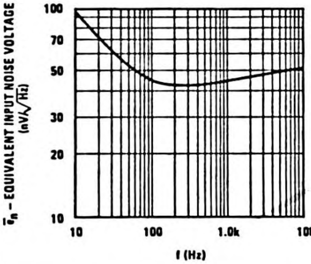
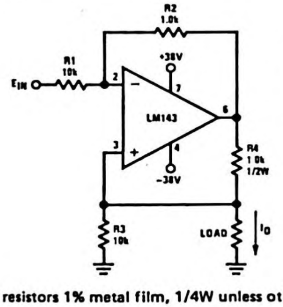


FIGURE 5. Noise Measurements

High Compliance Current Source

A current source with a compliance of ±28V is shown in *Figure 6.*



All resistors 1% metal film, 1/4W unless otherwise specified.

FIGURE 6. High-Compliance Current Source

The non-inverting input of the op amp senses the current through R4 to establish an output current, I_O proportional to the input voltage. The expression for I_O is

$$I_O = -\frac{E_{IN}\,R2}{R1\,R4} = -\frac{0.1\text{ mA}}{\text{V}}\,E_{IN}.$$

R3 keeps the circuit stable under any value of load resistance. Measured circuit performance is as follows:

$$I_{OMAX} = \pm 3.5\text{ mA at } E_{IN} = \mp 35\text{V}$$

$$R_{OUT} = 2\text{ M}\Omega \text{ at } I_{OUT} = \pm 2.0\text{ mA}$$

CURRENT BOOSTED APPLICATIONS

Because of the high voltage capability of the LM143, some thought must be given for the selection of the minimum load resistance. At an ambient temperature of 25°C, the LM143 can dissipate 680 mW. Worst case dissipation arises when the load resistance R_L is connected to one supply and $V_O = 0$. Then the amplifier sources $I_O = (38V/R_L)$ with 38V internal voltage drop. During this condition,

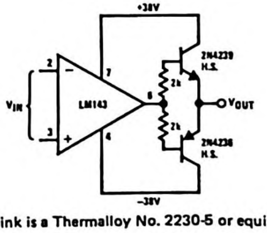
$$P_{MAX} = 680\text{ mW} = \frac{E_L^2}{R_L} = \frac{(38V)^2}{R_L}$$

$$\text{or } R_L = \frac{1444V^2}{680\text{ mW}} \approx 2.1\text{ k}\Omega$$

Hence, load resistances less than 2k will cause excessive power dissipation.

Simple Power Boost Circuit

For loads less than 2 kΩ, a power boost circuit should be added. The simple booster shown in *Figure 7* has the advantage of minimal parts count, but crossover distortion is noticeable and there is no short circuit protection; hence, either the LM143 or the boost transistors may fail under short circuit conditions.



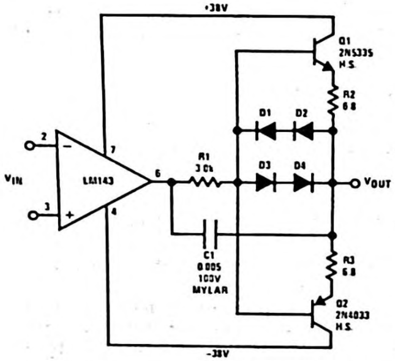
Heat sink is a Thermalloy No. 2230-5 or equivalent.
All resistors are 10%, 1W.

FIGURE 7. Simple Power Boost Circuit

100 mA Current Boost Circuit

With the addition of 4 diodes, a resistor and a capacitor, the booster circuit can be short circuit protected at 100 mA as shown in *Figure 8*.

R1 protects the LM143 by limiting the maximum drive current to (38V/3.0k) ≅ 12.5 mA, thereby keeping safely within the device dissipation limit of 680 mW. D1–D4 in conjunction with R2 and R3 protect the output transistors Q1 and Q2 by shunting the output drive current if the voltage drop across R2 or R3 exceeds 0.7V.



+38V
Q1
2N5335
H.S.
R2
6.8
D1
D2
2
7
R1
3.0k
D3
D4
VIN
LM143
6
VOUT
3
4
C1
0.005
100V
MYLAR
R3
6.8
Q2
2N4033
H.S.
-38V

Heat sink is a Thermalloy No. 2230-5 or equivalent.

All diodes are 1N914.

All resistors are 1/2W, 10%.

FIGURE 8. 100 mA Current Boost Circuit

Breadboard Data:

i) Frequency Response: Limited by LM143 frequency response and slew rate.

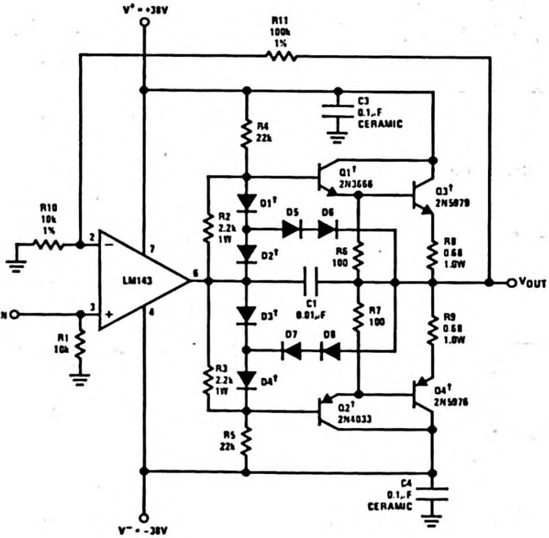
ii) Step response for unity gain, voltage follower configuration: Less than 10% overshoot for 1.0V step with 0.01μF capacitive load, 50% overshoot with 0.47μF capacitive load. The circuit is unconditionally stable for capacitive loads.

iii) Output Voltage: ±33 Vp-p into 400Ω load

1.0 Amp Class AB Current Booster

If crossover distortion is objectionable and currents of up to 1.0A are needed, the circuit in *Figure 9* should be used.

The output of the LM143 drives a class AB complementary output stage. The quiescent current for the output stage is set by the current flow through R4, R5 and diodes D1–D4. The diodes D1–D4 are on a common heat sink with the output transistors Q3 and Q4 so that the voltage drops across the diodes and base-



V⁺ = +38V
R11
100k
1%
C3
0.1μF
CERAMIC
R4
22k
Q1†
2N3666
Q3†
2N5979
R10
10k
1%
D1†
D5
D6
R2
2.2k
1W
2
7
D2†
R6
100
R8
0.68
1.0W
LM143
6
VOUT
VIN
3
C1
0.01μF
4
D3†
R7
100
R9
0.68
1.0W
R1
10k
D7
D8
R3
2.2k
1W
D4†
Q4†
2N5976
Q2†
2N4033
R5
22k
C4
0.1μF
CERAMIC
V⁻ = -38V

†Put on common heat sink, Thermalloy 6006B or equivalent.

All diodes are 1N3193.

All resistors are 10%, 1/4W except as noted.

FIGURE 9. 1 Amp Class AB Current Booster with Short Circuit Protection emitter junctions of the output transistors will track with temperature, Normally, R4 and R5 supply the current drive for the output Darlingtons, Q1, Q3 and Q2, Q4, but if additional drive is needed, the LM143 supplies the remainder through R2 and R3. For short circuited load, the drive current is bypassed around the output transistors through D1, D5 and D6 during the positive half cycle and through D4, D7 and D8 during the negative half cycle. Drive current bypassing, or output current limiting, occurs whenever R8 or R9 sees more than one diode drop (≅0.7V). An expression for the maximum output current is

$$I_{MAX} \cong \frac{0.7V}{0.68\Omega}$$

$$I_{MAX} \cong 1.0A.$$

Capacitor C1 stabilizes the circuit under most feedback and load conditions and C3 and C4 bypass the power supply. Measured performance is as follows:

i) Maximum output voltage with R_L = 40Ω: +29.6V, −28V with V_S = ±38 V_{DC}.

ii) Harmonic distortion measurements of *Figure 10* were measured with a closed loop gain of 10.

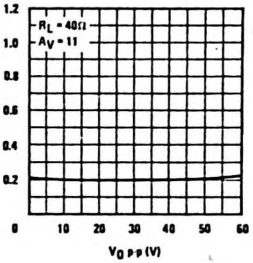
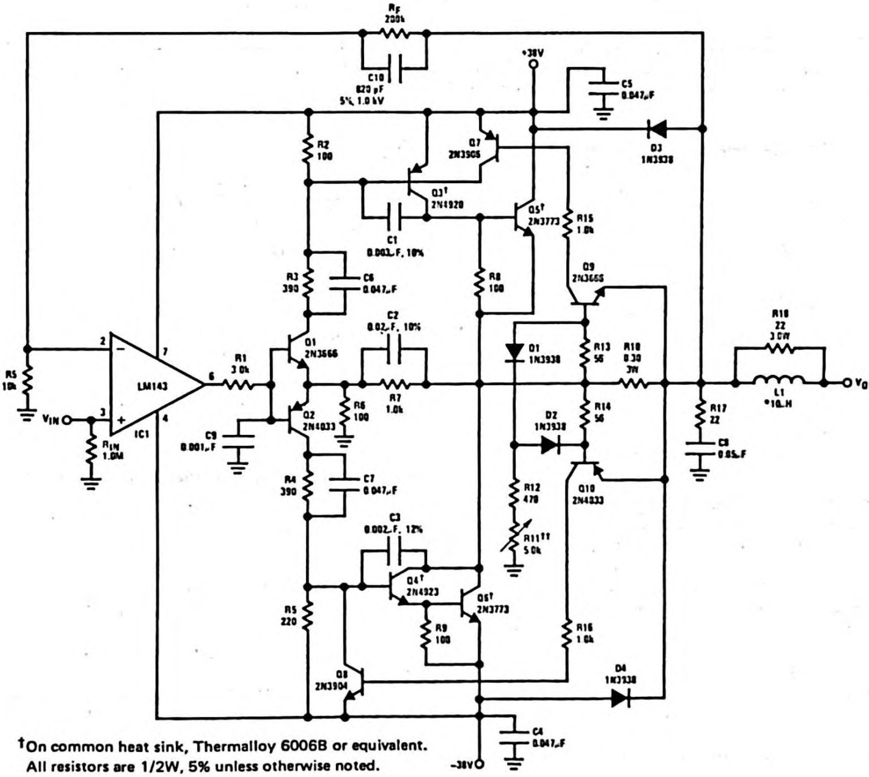


FIGURE 10. Harmonic Distortion Measurements

Very High Current Booster with High Compliance

If very high peak drive current is required in addition to a capability for the output swing to within 4.0V of the supplies under full load, the circuit in *Figure 11* should be used.


R_F
200k
C10
820 pF
5%, 1.0 kV
+38V
C5
0.047μF
R2
100
Q7
2N3905
D3
1N3938
Q3†
2N4920
Q5†
2N3773
R15
1.0k
C1
0.003μF, 10%
R3
390
C6
0.047μF
R8
100
Q9
2N3055
C2
0.02μF, 10%
R18
22
3.0W
2
7
Q1
2N3666
D1
1N3938
R13
56
R10
0.30
3W
R5
10k
LM143
6
R1
3.0k
L1
*10μH
V_{OUT}
V_{IN}
3
4
IC1
R_{IN}
1.0M
Q2
2N4033
R6
100
R7
1.0k
R14
56
D2
1N3938
R17
22
C8
0.05μF
C9
0.001μF
R4
390
C7
0.047μF
R12
470
Q10
2N4033
C3
0.002μF, 12%
R11††
5.0k
Q4†
2N4923
R5
220
Q6†
2N3773
R9
100
R16
1.0k
D4
1N3938
Q8
2N3904
C4
0.047μF
−38V

†On common heat sink, Thermalloy 6006B or equivalent.
All resistors are 1/2W, 5% unless otherwise noted.
All capacitors are 20%, 100V, ceramic disc unless otherwise noted.
††Output current limit adjust.

FIGURE 11. Very High Current Booster with High Compliance

Excluding the LM143, the current booster has three stages. The first stage is made up of Q1 and Q2 which level shifts and boosts the current output of the LM143 to about 100 mA. Q3 and Q4 further boost the output of Q1 and Q2 to about 1.0A. Q5 and Q6 then have adequate drive to source and sink at least 10A. There is no quiescent current path when the output voltage is zero since Q1 and Q2 are biased off.

The short circuit protection circuit is made up of Q7 and Q9 on the positive side and Q8 and Q10 on the negative side. Q9 or Q10 turns on as soon as $V_{BE} \cong 0.7V$ appears across R10 when the output terminal is shorted to ground. Then Q7 or Q8 bypass the drive to the output devices, Q5 and Q6. Since R10 is 0.3Ω, current limiting under short circuited output occurs at 2.3A and is relatively independent of the current limit adjustment resistor, R11. An expression for the maximum output current, $I_{OUT\ MAX}$, with V_{OUT} and R11 as variables is

$$|I_{OUTMAX}| \cong \frac{\dfrac{(|V_{OUT}| - V_{D1})\,R13}{R11 + R12 + R13} + V_{BE9}}{R10}$$

$$\cong \frac{\dfrac{(|V_{OUT}| - 0.7)\,56\Omega}{R11 + 526\Omega} + 0.7V}{0.3\Omega}$$

The equation is valid for both output polarities. The plot in *Figure 12* superimposes the above equation on the maximum operating area curve for the 2N3773 and illustrates the safe area protection feature.

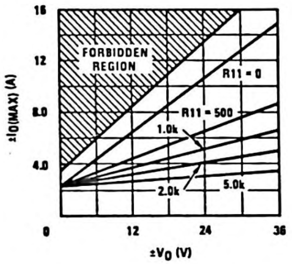


FIGURE 12. Maximum Output Current as a Function of R11 and V_{OUT}

The diodes, D1 and D2, are in the circuit to keep the base-emitter junctions of Q9 and Q10 from being reversed biased during the opposite polarity output voltage swings. C1, C2, C3, C6, C7 and C9 are judiciously inserted in the circuit to prevent oscillation. R17, R18, C8 and L1 are used in the circuit to maintain stability under all load conditions. Diodes D3 and D4 provide protection for inductive loads.

All measurements taken with a 4Ω load and ±38V supplies unless otherwise stated:

i) Maximum power out: 144 Wrms
ii) Frequency response:
  a) −3.0 dB at 10 kHz at full power
  b) −3.0 dB at 11.5 kHz at 10 Vp-p out
iii) Maximum output voltage: ±34V
iv) Maximum capacitive load: 10μF with 10% overshoot for a small signal step response
v) DC deadband: 20μV
vi) Quiescent current: 12.7 mA (positive supply), 2.1 mA (negative supply)
vii) Input impedance: 1 MΩ
viii) Voltage gain: 21

HIGH POWER APPLICATIONS

90 Wrms Audio Power Amplifier

A circuit diagram of an audio power amplifier which is capable of 90 Wrms into a 4Ω speaker or 70 Wrms into an 8Ω speaker is given in *Figure 13.* The circuit features safe area, short circuit and overload protection, harmonic distortion less than 0.1% at 1.0 kHz, and an all NPN output stage.

The output of the LM143 drives a quasi-complementary output stage made up of Q1, Q2, Q3 and Q4. This quasi-complementary circuit, which makes possible an all NPN output, was chosen over the complementary output circuit due to the lack of low cost high voltage power PNP transistors.

Safe area current limiting occurs whenever the output current is

$$|I_{OUTMAX}| = \frac{\dfrac{(|V_{OUT}| - V_{D3})\,R11}{R11 + R13} + V_{BE5}}{R12}$$

where R11 = R15 = 330Ω,

R13 = R14 = 3.9k,
R12 = R16 = 0.25Ω and

$V_{BE5} \cong V_{BE6} \cong V_{D3} \cong V_{D4} \cong 0.7V.$

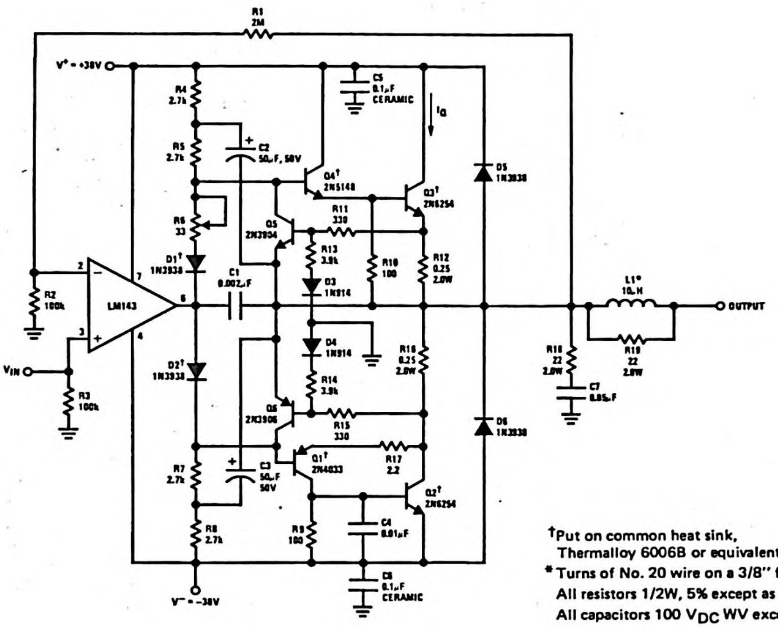
If the output is shorted, the above equation simplifies to

$$I_{OUT\ MAX} = \frac{V_{BE5}}{R12} \cong \frac{0.7V}{0.25\Omega} = 2.8A$$

If the output voltage is 30V,

$$I_{OUT\ MAX} = \frac{\dfrac{(30V - 0.7V)\,330}{4.23k} + 0.7V}{0.25\Omega}$$

$$\cong \frac{2.3 + 0.7V}{0.25} = 12A$$


R1
2M
V⁺ = +38V
R4
2.7k
C5
0.1µF
CERAMIC
I_Q
R5
2.7k
C2
50µF, 50V
Q4†
2N5148
Q3†
2N6254
D5
1N3880
R6
33
Q5
2N3904
R11
330
R13
3.9k
R10
100
R12
0.25
2.0W
D1†
1N3880
C1
0.002µF
D3
1N914
L1*
10µH
OUTPUT
2
7
6
3
4
R2
100k
LM143
D4
1N914
R16
0.25
2.0W
R18
22
2.0W
R19
22
2.0W
V_{IN}
D2†
1N3880
C7
0.05µF
R3
100k
R14
3.9k
Q6
2N3906
R15
330
D6
1N3880
R7
2.7k
C3
50µF
50V
Q1†
2N4033
R17
2.2
Q2†
2N6254
R8
2.7k
R9
100
C4
0.01µF
C6
0.1µF
CERAMIC
V⁻ = −38V

†Put on common heat sink,
Thermalloy 6006B or equivalent.
*Turns of No. 20 wire on a 3/8" form.
All resistors 1/2W, 5% except as noted.
All capacitors 100 V_{DC} WV except as noted.

FIGURE 13. 90W Audio Power Amplifier

The maximum output current, $I_{O(MAX)}$, versus V_O is plotted in *Figure 14*. D4 and D3 are in the circuit to keep Q5 off during the negative half of the output voltage cycle and Q6 off during the positive half cycle.

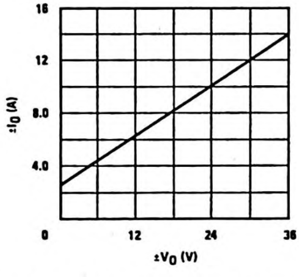


FIGURE 14. Output Current Limiting as a Function of Output Voltage

The output stage is biased into class AB operation by using the resistor string R4, R5, R7 and R8 to set the voltage drops across R6, D1 and D2, which then determine the quiescent current through the output transistors. These diodes are thermally coupled to the output devices to track their base-emitter junction voltages with temperature. Low distortion at low power levels is achieved by adjusting R6 to set the quiescent current through Q3 and Q2 to about 100 mA. *Figure 15* shows a plot of distortion at 50 mW versus quiescent current.

C2 and C3 are connected between the output and the R4, R5 and R7, R8 junctions to provide a "bootstrapped" drive potential for the output stage during output voltage swings near the power supply potentials. The absolute magnitudes of the voltages at these junctions exceed the power supply voltages during the high output swings so that adequate current drives to Q4 and Q1 are available. C1 and C4 are used for compensating the output stage. C5 and C6 are used for power supply bypassing. R18, C7, R19 and L1 are included in the circuit to keep the amplifier stable under all load conditions. D5 and D6 provide protection for inductive loads.

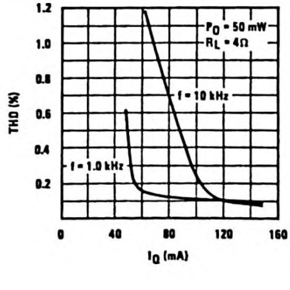


FIGURE 15. Quiescent Current vs Distortion

The input impedance of the audio amplifier is simply the value of R3. To keep the output offset voltages to a minimum, R3 ≅ R1 ll R2. The voltage gain is

$$A_V = 1 + \frac{R1}{R2} = 1 + \frac{2.0M}{100k} = 21$$

The following data was taken with $V_S = \pm 38V$:

i) Maximum power output before visible clipping:
  a) 90 Wrms at 1.0 kHz into 4Ω load
  b) 70 Wrms at 1.0 kHz into 8Ω load

ii) Distortion measurement: distortion versus frequency and power is plotted in *Figures 16 and 17.*

iii) Maximum capacitive load: 20μF

iv) Output noise, 10 Hz to 20 kHz: 100μVrms

v) Frequency response:
  a) Small signal (1.0 Vrms into 4.0Ω): −3.0 dB at 40 kHz
  b) Power (90W into 4Ω): −3.0 dB at 29 kHz
  c) Power (70W into 8Ω): −3.0 dB at 30 kHz

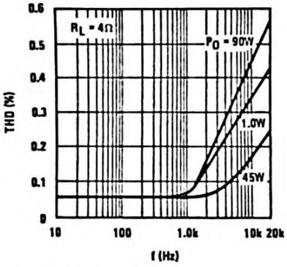


FIGURE 16. Distortion vs Frequency, $R_L = 4\Omega$

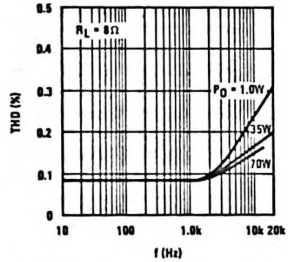


FIGURE 17. Distortion vs Frequency, $R_L = 8\Omega$

POWER SUPPLY CIRCUITS

The ability of the LM143 to withstand up to 80V can be exploited fully in the design of regulated power supplies. The circuits to be described use a zener reference voltage, an IC voltage amplifier, and a discrete power transistor pass element. If care is taken to keep the voltage drop across the pass element within 40V, standard three terminal voltage regulators such as the LM340, LM120, etc. may be used as pass elements and significantly decrease parts count and circuit complexity. Circuits using this approach are given in the LM340 application note (see AN-103).

A Tracking ±65V Supply with 500 mA Output

A tracking power supply circuit can be made by modifying the circuit for the 130 Vp-p driver circuit. The modified circuit is given in *Figure 18*.

A 2N4275 is used as a stable zener voltage reference of about 6.5V. Its output is amplified from one to about 10 times by the circuitry associated with IC1. The output of IC1 is applied through R10 to the Darlington connected transistors, Q2 and Q3. The feedback resistor, R5, one end of which is connected to the V^+ output node, is made variable so that the V^+ output voltage will vary from 6.5V to about +65V. The V^+ output is applied to a unity gain inverting power amplifier to generate the V^- output voltage. The output circuit of the unity gain inverter uses a composite PNP, Q4 and Q5, to provide the current boost.

Since the input terminals of A2 are at ground potential, the positive supply lead cannot be grounded; instead, it is connected to the output of a 4.7V zener diode, D8, to keep within the input common-mode range.

C1, C3 and C4 are used for decreasing the power supply noise. C2 is used in bypassing most of the noise generated by the reference voltage and C5 and C6 are used to reduce the voltage output noise. Short circuit protection is provided by D1, D2, D3, R10 and R14 on the positive side and by D4, D5, R11 and R15 on the negative side. The short circuit protection circuit is the same as the one used in the 1.0A current booster circuit.

The short circuit current is given by

$$I_{MAX} \cong \frac{V_{BE}}{R14} \cong \frac{V_{BE}}{R15}$$

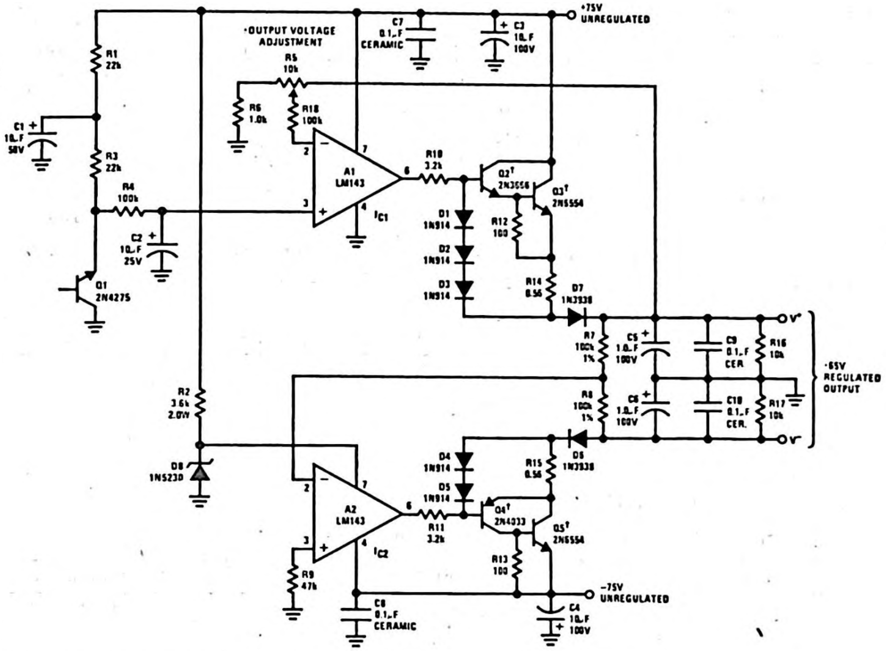
$$\cong \frac{0.7}{0.56} = 1.25A$$

where V_{BE} = voltage drop across a diode.

+65V, 1.0A Power Supply with Continuously Variable Output Current and Voltage

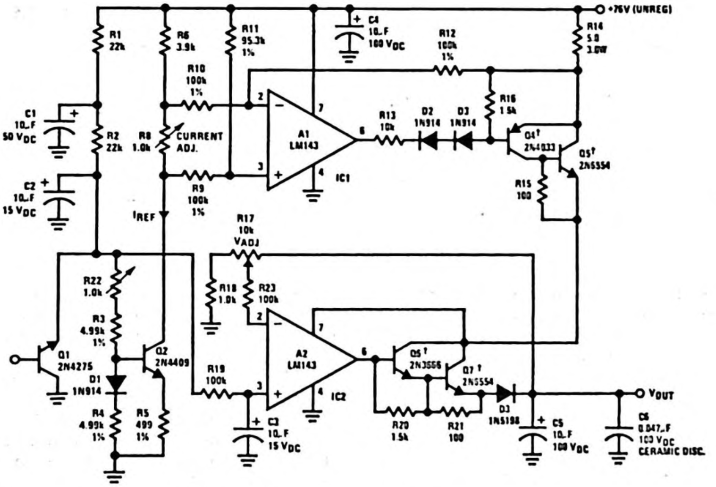
If a continuously variable output current as well as output voltage supply is needed, a power supply circuit given in *Figure 19* will do the job. It has an output range from 7.1V to 65V with an adjustable output current range of 0 to 1.0A.

Basically, the power supply circuit is a non-ideal voltage source in series with a non-ideal current source. A reference voltage of approximately 6.5V is obtained by zenering the base-emitter junction of the 2N4275. The positive temperature coefficient of the zenering voltage is compensated by the negative temperature coefficient of the forward biased base-collector junction. The output of the voltage reference goes to the variable gain power amplifier made up of IC2, Q6, Q7 and their associated components and to a reference current source made up of Q2, D1 and components around them. The variable gain power amplifier multiplies the reference voltage from one to ten times due to the variable feedback resistor, R17. Since the maximum current output of IC2 is at most 20 mA, the Darlington connected Q6 and Q7 are used to boost the available output current to 500 mA.


+75V UNREGULATED
R1 22k
C1 10µF 50V
R3 22k
R4 100k
C2 10µF 25V
Q1 2N4275
•OUTPUT VOLTAGE ADJUSTMENT
R5 10k
R6 1.0k
R18 100k
C7 0.1µF CERAMIC
C3 10µF 100V
A1 LM143
2
3
4
6
7
IC1
R10 3.2k
D1 1N914
D2 1N914
D3 1N914
Q2† 2N3566
Q3† 2N5554
R12 100
R14 0.56
D7 1N3938
R7 100k 1%
C5 1.0µF 100V
C9 0.1µF CER
R16 10k
V+
•65V REGULATED OUTPUT
R8 100k 1%
C6 1.0µF 100V
C10 0.1µF CER.
R17 10k
V−
R2 3.6k 2.0W
D8 1N5230
A2 LM143
2
3
4
6
7
IC2
R9 47k
C8 0.1µF CERAMIC
D4 1N914
D5 1N914
R11 3.2k
R15 0.56
D6 1N3938
Q4† 2N4033
Q5† 2N5554
R13 100
−75V UNREGULATED
C4 10µF 100V

†Put on common heat sink, Thermalloy 6006B or equivalent.
All resistors are 1/2W, 5%, except as noted.

FIGURE 18. Tracking 65V, 1A Power Supply with Short Circuit Protection


+76V (UNREG)
R1 22k
R6 3.9k
R11 95.3k 1%
C4 10µF 100 VDC
R12 100k 1%
R14 5.0 3.0W
C1 10µF 50 VDC
R2 22k
C2 10µF 15 VDC
R10 100k 1%
R8 1.0k
CURRENT ADJ.
R9 100k 1%
IREF
A1 LM143
2
3
4
6
7
IC1
R13 10k
D2 1N914
D3 1N914
R16 1.5k
Q4† 2N4033
Q5† 2N5554
R15 100
R17 10k VADJ
R22 1.0k
R3 4.99k 1%
Q1 2N4275
D1 1N914
Q2 2N4409
R4 4.99k 1%
R5 499 1%
R18 1.0k
R23 100k
R19 100k
C3 10µF 15 VDC
A2 LM143
2
3
4
6
7
IC2
Q6† 2N3566
Q7† 2N5554
R20 1.5k
R21 100
D3 1N5198
C5 10µF 100 VDC
C6 0.047µF 100 VDC CERAMIC DISC.
VOUT

†Put on common heat sink, Thermalloy 6006B or equivalent.
All resistors 1/2W, 10% unless otherwise noted.
All capacitors 20%.

FIGURE 19. 1A, 65V Power Supply with Variable Current Limit

Breadboard Data for the Tracking 65V Power Supply

$V_{IN} = \pm 75V$, $I_{OUT} = \pm 500$ mA, $T_j = 25°C$, $T_A = 25°C$, $V_{OUT} = \pm 40V$, unless otherwise specified.

PARAMETER	CONDITIONS	MEASURED DATA	
		$+V_{OUT}$	$-V_{OUT}$
Load Regulation	$0 \leq I_{OUT} \leq 500mA$	0.5 mV	1.0 mV
Line Regulation	$\lvert\pm 50V\rvert \leq V_{IN} \leq \lvert\pm 80V\rvert$		
	$I_{OUT} = \pm 100$ mA	175 mV	176 mV
	$I_{OUT} = \pm 500$ mA	169 mV	173 mV
Quiescent Current	$I_{OUT} = 0$	Pos. Supply 28.22 mA	Neg. Supply 6.55 mA
Output Noise Voltage*	$10 Hz \leq f \leq 100 kHz$	0.125 mV	0.135 mV
Ripple Rejection	$I_{OUT} = \pm 20$ mA, f = 120 Hz	−72.5 dB	−63.4 dB
Output Voltage Drift*		3.38 mV/°C	3.43 mV/°C

* The output noise and drift are due primarily to the zener reference.

Measured Performance of the 1A, 65V Power Supply

$V_{IN} = +76V$, $I_{OUT} = 500$ mA, $T_j = 25°C$, $V_{OUT} = +40V$ unless otherwise specified

PARAMETER	CONDITIONS	MEASURED DATA
Load Regulation	$0 \leq I_{OUT} \leq 500$ mA (Pulsed Load)	5.0 mV
Line Regulation	$46V \leq V_{IN} \leq 76V$	
	$I_{OUT} = 100$ mA	297 mV
	$I_{OUT} = 500$ mA	286 mV
	(dc Loads)	
Maximum Output Voltage	dc Load	68.6V
Quiescent Current		21.4 mA
Output Noise Voltage*	$10 Hz \leq f \leq 100 kHz$	0.280 mV
Ripple Rejection	$I_{OUT} = 20$ mA f = 120 Hz $\Delta V_S = 3.0$ Vp-p $\Delta V_O = 6.0$ mVp-p	66.6 dB
Loads are Pulsed Loads	200μs Pulse Every 200 ms	

* The output noise is due primarily to zener reference.

The power current source is an op amp used as a differential amplifier which senses the voltage drop across R8 and maintains this same voltage across R14. Hence, the maximum output current is

$$I_{OUT} = \frac{R8}{R14} \times I_{REF} \leq \frac{1.0k}{5.0\Omega} \times 5.0\text{ mA} = 1.0A.$$

Since the output load under most conditions will not demand what the power current source can deliver, Q4 and Q5 will remain in saturation during normal operation. When Q4 and Q5 are pulled out of saturation, the output load voltage will drop until the load current just equals what is available from the power current source. Because the positive supply terminal of IC2 is tied to the collectors of Q4 and Q5, IC2 will supply just enough current drive to Q6 and Q7 to keep itself on. Hence, a current limiting resistor is unnecessary for IC2. A 10k current limiting resistor, R13, is present since the total unregulated power supply voltage is available for IC1. R6 is used to stay within the input common-mode voltage range of IC1.

I_{REF} is derived from the 6.5V reference source, Q1, by using Q2 in a current source configuration. R22 is made adjustable so that I_{REF} can be set for 5.0 mA.

CONCLUSION

The LM143 is a high performance operational amplifier suited for applications requiring supply voltages up to ±40V. The LM143 is especially useful in power supply circuits where the unregulated voltages are as high as ±40V and in amplifier circuits where output voltages greater than ±30V peak are needed. The LM143 is internally compensated and is pin-for-pin compatible with the LM741. Compared with the LM741, the LM143 exhibits an order of magnitude lower input bias currents, better than five times the slew rate and twice the output voltage swing.

APPENDIX

Toward the goal of trouble-free applications, this appendix details some of the more subtle features of the LM143 and reviews application hints pertinent both to op amps in general and the LM143 in particular. The complete schematic of the LM143 is shown in *Figure 20.*

The circuit starts drawing supply current, at supply voltages of ±4V, when current is provided to a 7.5V zener diode D5 by the collector FET Q41. The gate-channel junction of Q41 exhibits 100V breakdown as source and drain are lightly doped NPN collector and substrate material. The collector current of Q18 biases current sources Q25 through Q30 and sets the supply current at nearly zero TC.

Q19 furnishes a bias voltage, 5V above the negative supply, for the collectors of Q15, Q20 and Q22. The low impedance 2V reference (V_{B1} in *Figure 1*) for the base of Q21 appears at the emitter of Q20 and has the correct TC to insure that Q23 never saturates. Should this occur, the low resistance of Q23 would cause premature LV_{CEO} breakdown of Q21.

The input transistors, Q1 and Q2, are biased by Q13 and Q14 which have a breakdown voltage essentially equal to BV_{CBO} by virtue of the high emitter impedance, R18 and R19, relative to the low dynamic impedance of D4. In a similar way, Q18 and Q19 stand off essentially the full supply voltage. These devices have a high output impedance caused by series feedback and so hold the supply current nearly constant to prevent excessive power dissipation at high supply voltages.

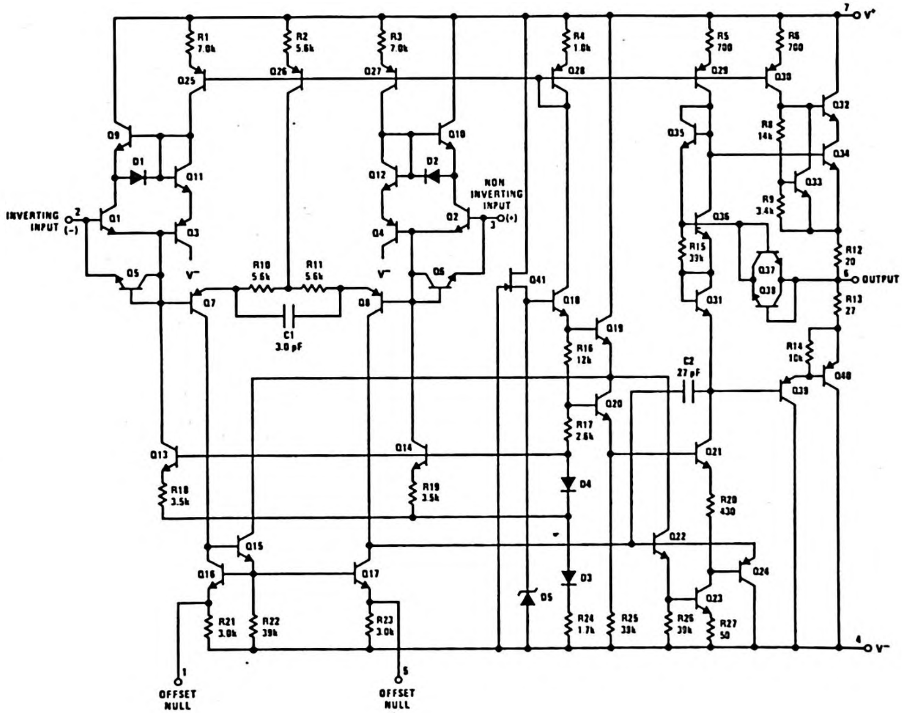

R1 7.0k
R2 5.6k
R3 7.0k
R4 1.0k
R5 700
R6 700
Q25
Q26
Q27
Q28
Q29
Q30
Q32
Q9
Q10
Q35
R8 14k
Q34
D1
Q11
Q12
D2
Q33
NON INVERTING INPUT
R9 3.4k
INVERTING INPUT (−)
2
Q1
Q3
Q4
Q2
3
(+)
Q36
R15 33k
R12 20
Q37
Q38
6
OUTPUT
Q5
V⁻
R10 5.6k
R11 5.6k
V⁻
Q6
Q7
Q8
Q41
Q18
Q31
R13 27
C1 3.0 pF
Q19
R16 12k
C2 27 pF
R14 10k
Q40
Q39
Q20
R17 2.6k
Q13
Q14
Q21
R18 3.5k
R19 3.5k
D4
R20 430
Q22
Q15
Q16
Q17
D3
Q24
D5
Q23
R21 3.0k
R22 39k
R23 3.0k
R24 1.7k
R25 33k
R26 39k
R27 50
7
V⁺
4
V⁻
1
OFFSET NULL
5
OFFSET NULL

FIGURE 20. Complete Schematic of the LM143

While the simple voltage clamping scheme, Q3 and Q4 in *Figure 1*, is adequate, it is prone to oscillation when built with high β PNPs. The more elaborate scheme of *Figure 20* prevents instability. This clamping method is similar to that used in the LM108, but allows large differential inputs to exist with complete input overvoltage protection. Q9 and Q10, which withstand the high input common-mode voltage, have a BV_{CBO}-type breakdown due to the low impedance diodes seen from the base leads and the high impedance of Q1 and Q2 (enhanced by 100% series feedback) in the emitter leads. Input overvoltage protection also holds up under high-level transient input voltages.

With a large negative-going step input, as could occur in the unity-gain voltage follower configuration, diode-connected Q6 turns "ON," protecting the emitter-base junction of Q2 from zener breakdown and subsequent long-term β degradation. At the same time, stray capacitance at the collector of Q2 is discharged by D2 through Q4 and Q12. This holds Q10 in a true BV_{CBO} mode (emitter open-circuited) and clamps the voltage across Q2 to 3 V_{BE}.

With a large positive-going step input, stray capacitance at the collectors of Q2 and Q12 is charged by the forward-biased collector junction of Q2. As before, with D2 conducting, Q10 is again in the BV_{CBO} breakdown mode. Since the inverting input can be subject to the same transients, Q1 is afforded the same protection.

Distributed capacitance associated with R10 and R11, together with the collector-base capacitance of Q26, cause a high frequency transmission pole (the "tail" pole(2)) which can degrade phase margin. This is avoided by adding a small lead capacitor, C1, which provides an alternative low-impedance signal path, thus bypassing the tail pole.

The offset null resistors, R21 and R23, are made larger than that strictly necessary to null the offset voltage. This reduces the transconductance of Q17 and, therefore, the noise gain of the active loads into R10 and R11. By this simple expedient, broadband input noise voltage is substantially reduced.

The voltage reference for the output stage (V_{B2} in *Figure 1*) is realized by actively simulating a 4-diode stack. The voltage across Q33, given by $(1 + R8/R9)$ V_{BE}, is about 3.5V. Biased at 400μA from Q30, the circuit presents a low impedance, less than 50Ω, to the base of Q32. Since the TC of the reference is negative, Q34 is designed to always remain out of saturation under worst-case conditions of high temperature and high output current. This avoids potential destructive breakdown of Q32.

Current limiting for Q32 and Q34 is provided by diode-connected Q37 and resistor R12. When the voltage drop across R12 turns on Q37, it removes base drive from Q34. In a similar fashion, current limiting in the negative direction is initiated when the voltage drop across R13 causes Q38 to conduct. This current is limited in Q21 by R20 to about 1 mA. When this occurs, base drive is removed from Q39.

Although output short circuits to ground or either supply can be sustained indefinitely at supply voltages lower than ±22V, short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. As with all IC op amps, voltage reversal between the power supplies will almost always result in a destroyed unit.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

REFERENCES

1. R. J. Widlar, "Super Gain Transistors for ICs," National Semiconductor TP-11, March 1969.
2. J. E. Solomon, "The Monolithic Op Amp: A Tutorial Study," IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.

A Linear Multiple Gain Controlled Amplifier

National Semiconductor
Application Note 129
Jim Sherwin
August 1975

INTRODUCTION

A linear control function over three decades of gain can be achieved with a FET in the feedback path of a non-inverting amplifier. Besides the ultimate simplicity of the circuit, multiple tracking gain control circuits can be constructed with dual op amps and monolithic dual FET's or quad op amps and monolithic quad FET's. Such circuits could even be integrated with ion-implanted FET's on single or multiple monolithic op amp chips. The gain control range may be designed for less than 2 to 1 or higher than 1000:1, but input voltage levels are limited by acceptable levels of distortion. Bandwidth is dependent on maximum gain and unity gain bandwidth of the op amp used. The gain control circuit is especially suitable for volume expansion applications.

GAIN CONTROL WITH FETS

The FET has long been used as a voltage controlled resistor (VCR), often as the shunt arm in the series-shunt attenuator of *Figure 1.* Advantages of the FET as a VCR are that:

1. The control signal is almost perfectly isolated from the controlled signal path, and
2. The resistance can be made to vary over an almost infinite max/min ratio.

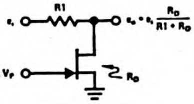


FIGURE 1. Voltage Controlled FET Attenuator

Disadvantages are that:

1. The FET behaves as a linear resistance only for small values of source-drain voltage V_{DS},
2. Non-linearity (of resistance) increases as the control voltage V_{GS} approaches cut-off voltage V_P when the resistance is maximum,
3. The relationship of resistance r_d to V_{GS} is reciprocal rather than direct linear,
4. VCR multiples with matched resistance characteristics over their full control range have been extremely difficult to obtain at any kind of reasonable price, and
5. Production spread in V_P requires separate bias set and gain set on each circuit.

Examination of the FET drain characteristics in *Figure 2* will reveal the essential non-linearity of r_d at high signal levels, especially as V_{GS} approaches V_P. This non-linear region must be avoided in order to achieve tolerable distortion levels. One obvious way is to limit V_{DS} to small values when r_d is high as suggested by *Figures 2c and 2d,* another is to utilize FET's with high V_P as suggested by reference to *Figures 2b and 2d.*

The reciprocal relationship of r_d and V_{GS} is an advantage, as it is precisely that which allows the linear control of gain in the circuit to be described. The availability of matched monolithic dual FET's such as the NSC 2N3958 (watch out for the matched pairs as their resistance match close to V_P may not be as good as that of the monolithic versions) make available low cost duals with very closely matched resistance characteristics over the full control range. There are even some monolithic quads available (such as the AM9709 series). The final problem of the production range of V_P can be much improved with ion-implant diffusion techniques whereby lot variation in V_P may be held to within a few tenths of one volt.

The gain control circuit is that of an ordinary non-inverting op amp with feedback. The usual circuit is modified in *Figure 3a* to include a FET as controlled resistor. The gain function is normal except that r_d replaces R2 in the usual form.

$$A_V = 1 + \frac{R1}{r_d} \qquad (1)$$

Now r_d can be equated to a control voltage V_C as follows:

$$r_d = r_o \frac{V_P}{V_P - V_{GS}} \qquad (2)$$

Where:

$$r_o = r_d \big|_{V_{GS} = 0}$$

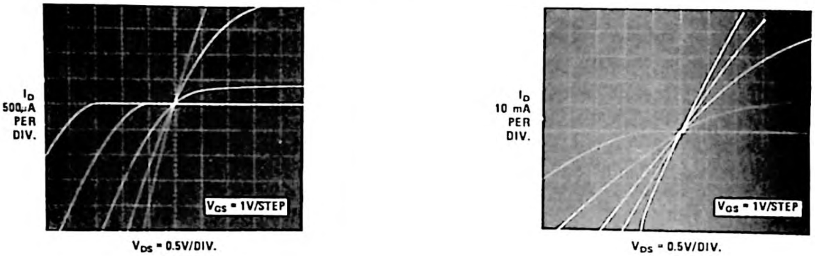
$$r_d = r_o \frac{V_P}{V_C} \qquad (3)$$

Where:

$$V_C = V_P - V_{GS}$$

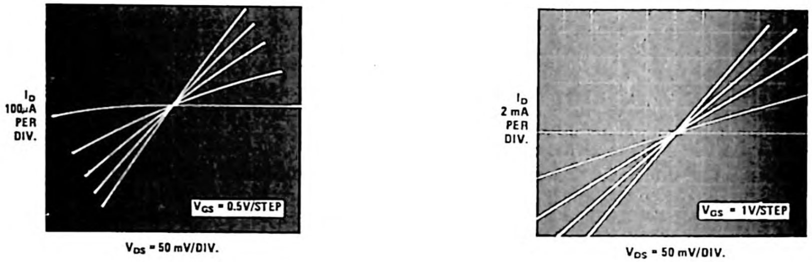
The gain function is thus seen to be linear with V_C.

$$A_V = 1 + \frac{R1}{r_o} \frac{V_C}{V_P} \qquad (4)$$



a) V_P = 2.8V

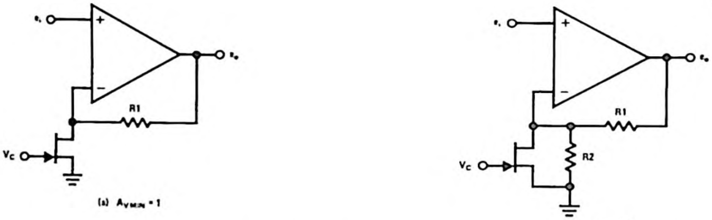
b) V_P = 9V



c) V_P = 2.8V

d) V_P = 9V

FIGURE 2. AC Output Characteristics of FET



(a) A_{VMIN} = 1

(b) A_{VMIN} > 1

FIGURE 3. FET/Op Amp Gain Control Circuit

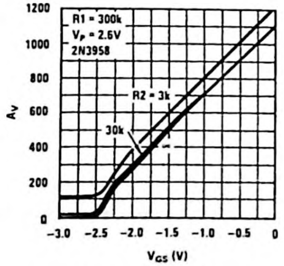


FIGURE 4. Gain vs Control Voltage For Short Channel FET

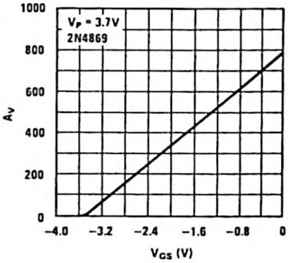


FIGURE 5. Gain vs Control Voltage For Long Channel FET

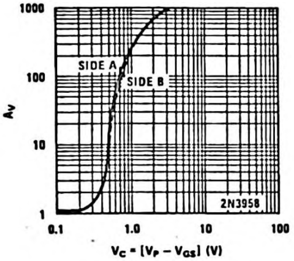


FIGURE 6. Control-Gain Match For Dual FET

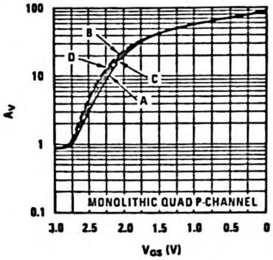
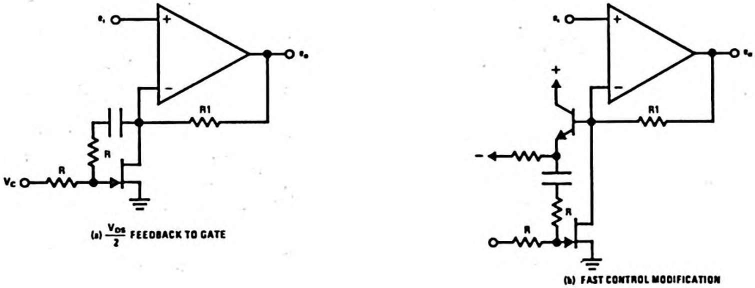


FIGURE 7. Monolithic Quad Gain Control Tracking



(a) $\frac{V_{DS}}{2}$ FEEDBACK TO GATE

(b) FAST CONTROL MODIFICATION

FIGURE 8. Circuit to Reduce Distortion

At $V_C = 0$, the gain reduces to unity; and at $V_C = V_P$, the gain increases to $1 + R1/r_o$ which may be as high as 1000 or so. If it is desired to limit the minimum gain to some value greater than unity, another resistor R2 may be added as in *Figure 3b.* Then the gain equation becomes:

$$A_V = 1 + \cfrac{R1}{\cfrac{R2\, r_o\, (V_P/V_C)}{R2 + r_o\, (V_P/V_C)}}$$

$$= 1 + \frac{R1\, [R2 + r_o\, (V_P/V_C)]}{R2\, r_o (V_P/V_C)}$$

$$A_V = 1 + \frac{R1}{R2} + \frac{R1\, V_C}{r_o\, V_P} \qquad (5)$$

In either case, the gain function is linear with V_C.

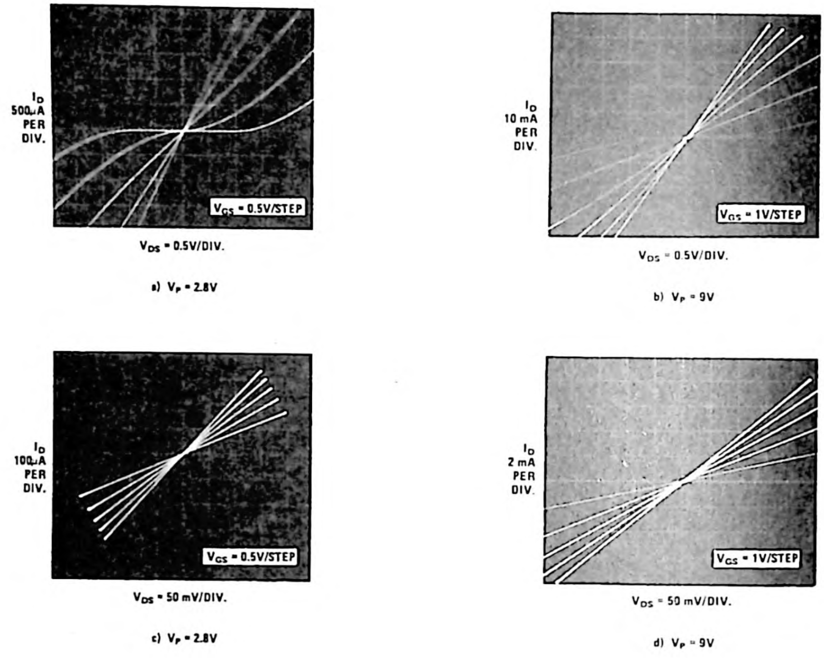
The circuits of *Figure 3* do indeed show a linear gain versus control voltage as plotted in *Figure 4* for several values of minimum gain. There is some non-linearity near minimum gain which appears in all curves. This is certainly due to a non-ideal characteristic of the FET caused by finite contact and bulk resistance at source and drain. *Figure 5* shows a similar control curve for a FET with longer channel in which the controlled channel resistance is a greater part of the total resistance than that of the short channel device of *Figure 4*. For those applications requiring a more precisely linear control of gain, the long channel devices will be preferable.

Several variable-gain circuits can be made to track when monolithic multiple FET's are used as the control elements with matched feedback resistors. A monolithic FET dual (NSC 2N3958) used in two identical control circuits shows remarkable tracking over the entire control range, even when V_{GS} is near V_P where variations would be expected to be most apparent. The plots appear in *Figure 6.* Similar performance for a quad gain control using a monolithic P-channel quad FET (AM97C09 or AM9709) is shown in *Figure 7.*

DISTORTION

Reference to *Figure 2* will show that the FET acts as a linear resistance only for relatively small values of drain-source voltage, in either polarity. This is particularly apparent for positive V_{DS} (for N-channel FET) and V_{GS} approaching V_P. The difference between *Figures 2c and 2d* indicates that the maximum allowed applied signal will be greater for high V_P as compared with low V_P.

It is possible to improve the linearity characteristics somewhat by applying a part of the V_{DS} in series with the control voltage applied as V_{GS}. The circuit to accomplish this is that shown in *Figure 8.* It happens that about half of V_{DS} applied to the gate provides the greatest improvement for small signals. The addition of two resistors and one capacitor as in *Figure 8a* is all that is required. The capacitor simply blocks the control voltage from the FET drain and the op amp input. *Figure 8b* shows the addition of an emitter follower to



a) V_P = 2.8V

b) V_P = 9V

c) V_P = 2.8V

d) V_P = 9V

FIGURE 9. AC Output Characteristics of FET with Feedback Linearization

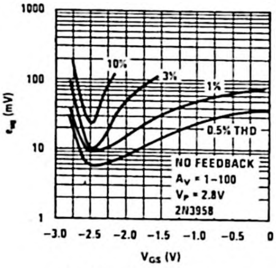


FIGURE 10. Distortion With V_P = 2.8V

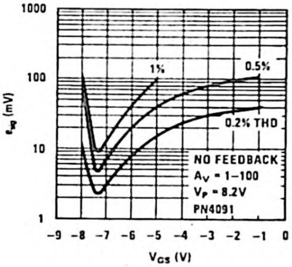


FIGURE 11. Distortion With V_P = 8.2V

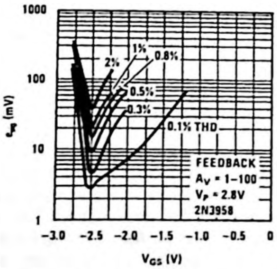


FIGURE 12. Distortion With V_P = 2.8V, With Linearization

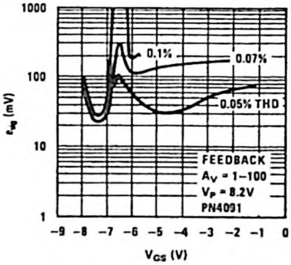


FIGURE 13. Distortion With V_P = 8.2V, Linearized

prevent abrupt changes in V_C from coupling to the op amp. *Figure 9* shows the improved linearity of the drain characteristics as compared to *Figure 2*. The improvement is also seen in the distortion versus input signal plots of *Figures 10—13*. Note particularly that the distortion at any value of V_C is primarily a function of input signal (which equals the feedback signal applied to the FET drain at the inverting input). Some modification is made to this direct relationship if an R2 is shunted across the FET as in *Figure 3b*. Measured distortion at low signal level is the result of noise rather than of signal distortion. Maximum gain is limited to about 100 in these plots so as to avoid the region of lower S/N. The noise is that of the op amp input stage and the signal source resistance plus the contribution of the FET which is essentially the thermal noise of r_d.

BANDWIDTH AND CONTROL TIME CONSTANT

The circuit bandwidth is the closed loop bandwidth of the op amp used at the (instantaneous) set gain. The gain control time constant is that of the input circuit to the FET (dependent on the value of R in *Figure 8*) limited by the slew rate of the op amp. The FET itself reacts practically instantly, producing a step change in feedback ratio. Control time constant is thus a few microseconds at most.

APPLICATIONS

Three obvious applications present themselves; they are:

1. Remote or multichannel gain control
2. Volume expansion
3. Volume compression/limiting

To this short list might be added a number of others, including applications in noise reduction and quad sound techniques.

The gain-controlled amplifier of *Figure 14* has a gain range of 1—1000, a maximum output level of 8.5 Vrms, and a bandwidth of better than 20 kHz at maximum gain. The FET used has high V_P for maximum freedom from distortion. *Figures 15 and 16* show the gain function and constant distortion contour lines. Note that the gain control curve is non-linear near unity gain because the PN4091 is a short channel FET. Distortion is quite low except as limited by maximum output voltage. Note that the maximum e_{in} is restricted by output saturation. The LM318 is used in the example only to achieve wideband response at maximum gain. The amplifier input voltage must be restricted to about 8 mVrms at maximum gain when the S/N will be about 60 dB over a 10 kHz bandwidth.

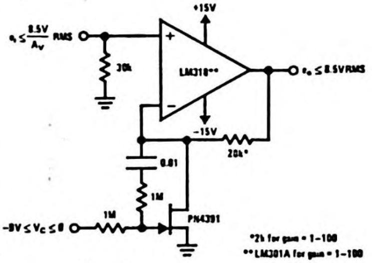


FIGURE 14. Amplifier With Gain Range = 1—1000

A more practical circuit might employ a gain range of 1—100. Then the amplifier could be a LM301A and still achieve a 10 kHz bandpass at maximum gain. The input signal could, accordingly, be increased to 80 mVrms for a S/N of 80 dB. This performance can be extended to dual and quad control circuits with tracking gain functions, but watch the bandwidth as required at maximum gain. Any of the several dual op amps could be used with the 2N3958 (monolithic dual from NSC), or the LM324 quad op amp can be used in limited gain times bandwidth applications with a quad monolithic FET. *Figure 17* shows all details of an ac coupled tracking quad gain control with 40 dB range. Gain varies over 1—100 range, bandwidth is 10 kHz minimum, S/N is better than 70 dB with 4.3 Vrms maximum output. *Figure 7* shows the gain curve and matching characteristics.

Noise considerations could be important in this method of gain control, as the signal is amplified rather than attenuated. To realize the function of a 40 dB variable attenuator, it is necessary to install a fixed attenuator at the amplifier input and perhaps also at the output. This will reduce the minimum signal level to millivolts, thus a low noise amplifier is desirable. The LM381 dual low-noise ac coupled amplifier could be used in a 40 dB

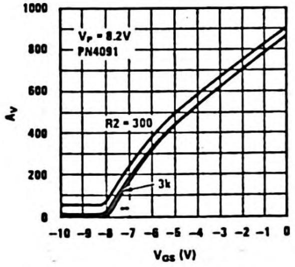


FIGURE 15. Gain For Circuit of Figure 14

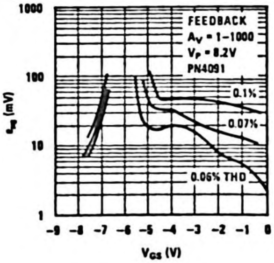


FIGURE 16. Distortion For Circuit of Figure 14

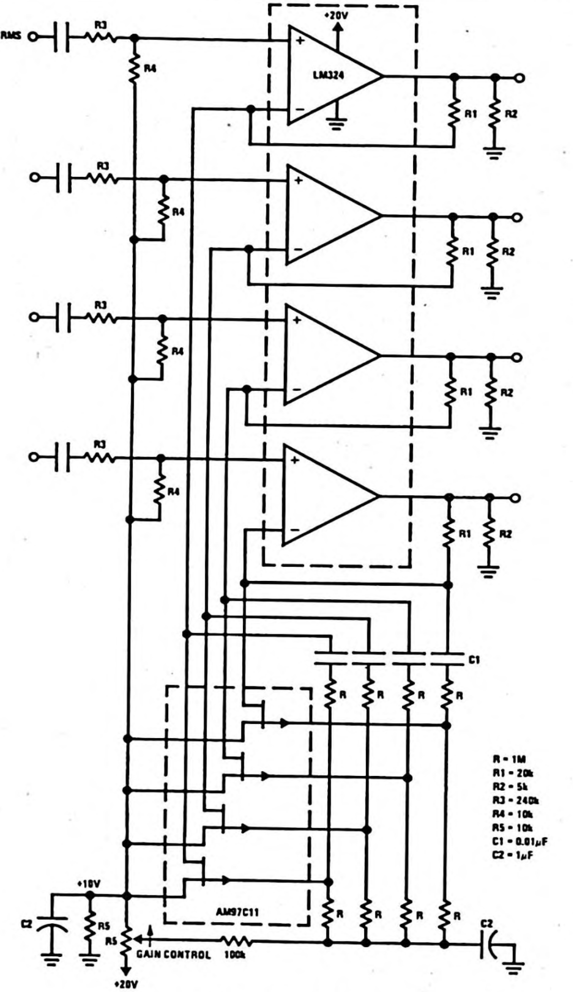

eᵢ ≤ 1VRMS
R3
R4
+20V
LM324
R1
R2
C1
R
AM97C11
+10V
C2
R5
GAIN CONTROL
100k
+20V
R = 1M
R1 = 20k
R2 = 5k
R3 = 240k
R4 = 10k
R5 = 10k
C1 = 0.01μF
C2 = 1μF

FIGURE 17. Quad Gain Control

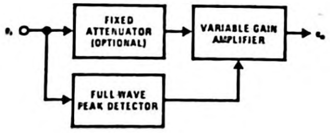

eᵢ
FIXED ATTENUATOR (OPTIONAL)
VARIABLE GAIN AMPLIFIER
eₒ
FULL WAVE PEAK DETECTOR

FIGURE 18. Volume Expander/Compressor Block Diagram

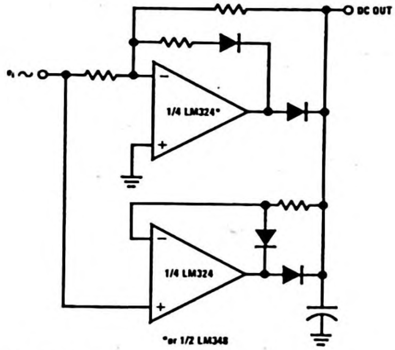

DC OUT
eᵢ ~
1/4 LM324*
1/4 LM324
*or 1/2 LM348

FIGURE 19. Full Wave Linear Precision Peak Detector

audio attenuator to realize S/N about 100 dB or in a 60 dB attenuator to realize 80 dB S/N. Improvements in S/N can be made by reducing system bandwidth in fixed or low frequency operation. Minimum noise is also achieved by using the minimum practical amplifier source resistance. Values as low as 1 kΩ are advantageous.

The effect of temperature will be to change the gain according to the temperature sensitivity of the FET. This effect can be reduced by using a silicon resistor for the feedback resistor, R1. If the FET were to be integrated onto the op amp chip, an attempt should be made to include R1 on the chip as well.

The application to a volume expander circuit is of interest as the control is linear, the required control range is only about 1:4, and the input signal is small for the low gain condition when distortion would otherwise be most apparent. The elements of a volume expander are indicated in *Figure 18.* The gain controlled amplifier need only exhibit a 12 dB variation in gain, being lowest for small signals. The slope of gain versus control should be linear, more specifically the slope of (log) gain in dB versus (log) signal in dB should be linear. A practical range is 12 dB gain change over a 30 dB input signal range. The peak detector should be linear down to very small signals, exhibit a fast attack or charge time of a millisecond or less, a discharge time constant of about 2 seconds, and operate on the first half cycle (full-wave detector). The detector should, therefore, be a full-wave precision linear peak detector with low internal impedance; the requirements can be met with the circuit of *Figure 19.*

The expander circuit shown in *Figure 20* will perform as desired. The gain control function is plotted in *Figure 21;* distortion is below 0.1% at all levels. Resistors R3 and R4 are added in order to modify the linear control curve to the desired log curve. Note that the input signal is attenuated prior to amplification in order to reduce distortion and maintain an overall gain of approximately 0 dB at midrange of expansion. The noise with the LM124 over a 20 kHz bandwidth is, of course, a function of signal; but the maximum signal to noise ratio is 80 dB. The circuit could be adapted to stereo or quad sound as in *Figures 22–23.* Questions for individual design concern the method of control. Whether to expand all channels together, and whether to derive the control signals individually from each channel, a summation from 2 to 4 channels, or from a single channel (assuming that high level from any channel indicates high levels from all channels). Note that the FET is biased OFF (minimum gain) for low signals, and increasing signals progressively bias the FET ON (maximum gain).

The volume compression circuit is a logical mate to the expander. The only difference would be that the FET is initially biased ON (maximum gain) for low signals, and

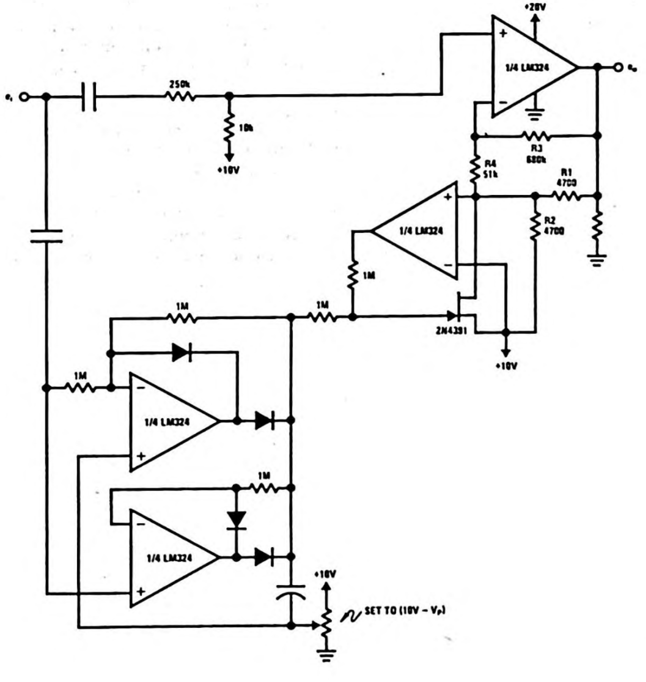


FIGURE 20. Volume Expander Circuit

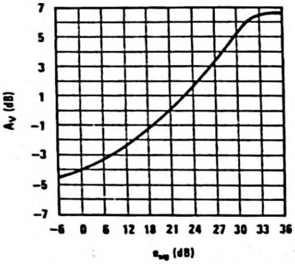


FIGURE 21. Expander Gain Characteristic

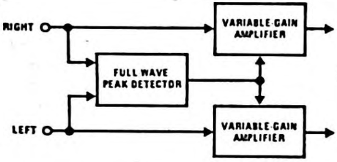
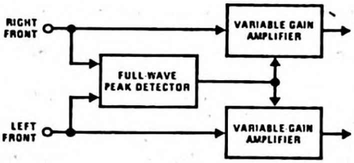

RIGHT
LEFT
FULL WAVE PEAK DETECTOR
VARIABLE-GAIN AMPLIFIER
VARIABLE-GAIN AMPLIFIER

FIGURE 22. Stereo Expander Block


RIGHT FRONT
LEFT FRONT
FULL-WAVE PEAK DETECTOR
VARIABLE GAIN AMPLIFIER
VARIABLE GAIN AMPLIFIER

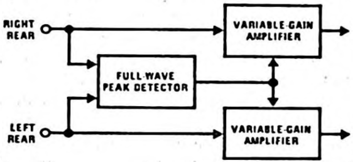

RIGHT REAR
LEFT REAR
FULL-WAVE PEAK DETECTOR
VARIABLE-GAIN AMPLIFIER
VARIABLE-GAIN AMPLIFIER

FIGURE 23. Four-Channel Expander Block

increasing signals progressively bias the FET OFF (minimum gain). A disadvantage is that the circuit produces greatest distortion in the low gain condition when signals are highest. Maximum S/N is degraded by 24 dB over that of the expander, minimum S/N is the same.

CONCLUSION

The combination of FET and op amp provides a linear dc (voltage) control of gain over a range to 60 dB. As the circuit realizes positive gain, rather than being a controlled attenuator, the input signal is limited. Input signal is further limited to several hundred millivolts by the non-linearity of the FET (which sees the full input signal). Because input signals will generally be in the 10–300 mV range, noise performance of the selected op amp will be important. Even so, S/N of 60–100 dB is obtainable with standard amplifiers. Tracking pair or quad gain-control amplifiers are realizable with existing monolithic dual or quad FET's, and the combination of FET and op amp lends itself to simple integration. The circuit is well-suited to remote and multiple linear gain control and to volume expander/compressors. The volume expander is especially interesting as the signal level and gain conditions result in extremely low distortion and more than adequate signal-to-noise ratio.

The Monolithic Temperature Transducer — A New Interfacing Concept

National Semiconductor
Application Note 132
Peter Lefferts
December 1974

INTRODUCTION

The percentage of analog and analog/digital signal handling done by monolithic integrated circuits is ever increasing. However, until now almost all input signals were voltages generated by often complex and expensive transducers needing special input wiring to the integrated circuit.

Now with the ability of an IC to *directly* sense absolute temperature, and provide a linear, buffered electrical output, the situation has greatly changed. A number of physical parameters can now be sensed directly by the National LX5600 monolithic transducer with a resulting saving in hardware, wiring, and therefore cost.

For example, using temperature sensing as an "interface"; position, air velocity, liquid presence, and conductivity can be measured or controlled. Rate of temperature change can be sensed to improve the performance of on-off temperature controllers. The monolithic transducer allows a much simplified servo for improving surface or moving-surface temperature measurements. The purpose of this note is to illustrate the possibility and practicality of a number of these sensing techniques.

As background for the rest of this note, the block diagram and operation of the thermometer will be briefly described. Also methods of powering the LX5600 will be outlined, and a special integrated power transistor ideal for isolating the thermometer from heavy or variable loads will be presented.

TRANSDUCER DESIGN

Figure 1 illustrates how the 3 separate functions of the thermometer IC are arranged so that only 4 external connections are needed. The zener and its amplifier form a shunt regulator with a typical impedance of 3Ω. The reference is quite stable with temperature so that a potentiometer across pin 3 and 4 can be used to set up a Centigrade or Farenheit zero calibration. This would be used when the thermometer is applied in its linear mode, such as with pins 1 and 2 shorted together so that the op amp forms a unity gain follower.

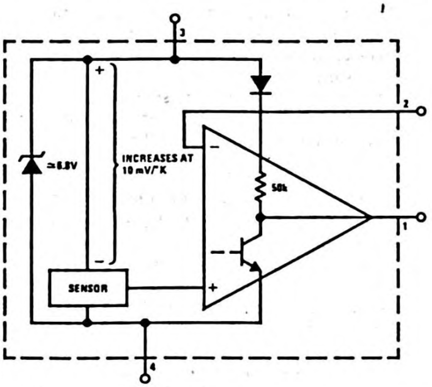


FIGURE 1. Block Diagram

Similarly a pot across 3 and 4 with the wiper to pin 2 determines a temperature set-point since the op amp can be operated "open loop," which will cause the output at pin 1 to swing about 30V for a 0.2°C (or Kelvin) change at the sensor around the set point.

The sensor section, with its associated amplifier, generates a negative going signal of 10 mV/°K. For instance, at 0°C this signal would be −2.73V (with respect to pin 3) and appear at the plus terminal of the internal operational amplifier. The actual sensor principle is somewhat more sophisticated than a resistance or diode-drop change with temperature. It uses the difference in V_{be} between matched transistors which involves operating two transistors at greatly differing collector currents but with their bases in parallel. If this collector current ratio is controlled there will be a very predictable difference of emitter voltage. Further, this voltage varies with temperature in a known and reproducible manner. This voltage change is less dependent on processing variations than any of the other known semiconductor effects. Further details on these effects can be found in the reference. (1)

The internal op amp provides a consistent, very light loading of the sensor output. Having a feedback terminal available, gains from unity up to 100 or so are feedback controllable, or an open-loop gain of several thousand is available. PNP input transistors allow the op amp to function as a comparator over a large range of inputs. Internal compensation is provided. Output is a collector with a 50k load (pull-up) resistor provided, that is, however diode decoupled for output voltages higher than the pin 3 supply voltage. A complete schematic of the transducer is provided in the appendix.

POWERING THE TRANSDUCER

Successful application of the LX5600 starts with providing power in the optimum way. Since the device senses its own temperature, it follows that minimum internal power dissipation is desirable. With no output load, the internal electronics (op amp, etc.) typically need about 1/2 mA to operate correctly. If the zener shunt regulator is to operate also, 1 mA is recommended. Let us examine the four powering methods of *Figure 2* with regard to zener operation and temperature rise. Still air operation, a 6.8V zener, and 0.17°C/mW temperature rise for a TO-5 package are assumed for the following discussion.

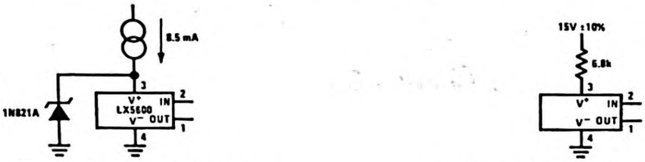


FIGURE 2a. Constant Voltage Mode

FIGURE 2b. Dropping Resistor Method

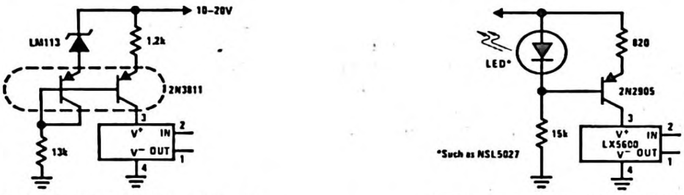


FIGURE 2c. Precision Current Source

FIGURE 2d. Low Cost Current Source

FIGURE 2. Powering the Monolithic Transducer

Figure 2a illustrates minimum device dissipation by sacrificing use of the internal reference. A typical unit would self-heat only about 0.5°C and would vary only about 0.1°C over supply and temperature variations. This connection is particularly useful for accurate air temperature measurements and is very suitable for differential measurements where a second transducer can supply the reference.

The simplest method is *Figure 2b* using only a resistor. With the supply variations shown, the reference typically varies less than 1 mV. The temperature rise is only about 1.25°C with plus or minus about a quarter degree for supply variations. With a modestly-regulated supply, the resistor powering method obviously becomes very good. However, if one considers an aging automotive battery with a loaded output of only 11V available, a 3.9k resistor would be needed to insure 1 mA of current. Then the same battery being heavily charged (15 V_{DC}) would supply twice the current to the thermometer with an *increase* of self-heating of about 1.2°C.

One of the applications to follow involves reading outside air temperature. Since most people are accustomed to reading temperature in °F, the over 2°F error of the above example will be noticeable. The two constant current supplies to be described solve this problem. Total *change* in self-heating becomes well less than 0.1°F over a 100°C temperature range and a 2:1 supply voltage range. Further, the internal reference is properly powered, with current changes causing less than 1 mV change in V_Z.

The reference current source of *Figure 2c* uses the precision 1.22V reference diode which changes only about 1% over the entire −55°C to +125°C temperature range. A diode-connected transistor, temperature compensates the constant current transistor so almost exactly the reference voltage appears also across the emitter resistor, stabilizing the current.

The source of *Figure 2c* is probably of greater cost and precision than is needed in this application. The *Figure 2d* current source is much less expensive and yet reasonably stable. With only about a volt needed between power input and collector output, it is much superior to the usual zener referenced current source requiring 5 to 6V of such loss.

A little used characteristic of light emitting diodes is employed in stabilizing this current source. At the low currents used, the LED has a typical drop of 1.5 to 1.7V, or about 0.8 to 1V *more* than the junction drop of a small transistor. Thus, when paired as shown in *Figure 2d* the remaining voltage appears across the transistor's emitter resistor. Further this voltage is temperature *stable* since the LED's junction temperature coefficient is just about the same as a transistor's base-emitter junction coefficient. In both cases this is about −2 mV/°C. Preliminary tests indicate that adjustments of the temperature coefficient can be made by changing the ratios of transistor to LED current, and that once a stable combination is found similar parts (same part number and same process) should reproduce the stability obtained within 1 or 2%, over the −55°C to 100°C range. Doubling LED current only results in approximately 40 mV increased junction drop, so a 2:1 supply change will only result in a 5% further current change.

OPTIMUM LOAD ISOLATION

The need to minimize power dissipation has already been emphasized. In fact the previous heat rise figures were based on zero load on the thermometer's output transistor. Certain of the applications to be presented involve driving of lamps, solenoids, or heaters. Much would be lost in simplicity if the thermometer had to drive a buffer amplifier followed by two or more cascaded power transistors.

To solve this problem the LM195/LM395 monolithic power transistor is used. An ampere of load current may be handled requiring only a few microamperes drive from the monolithic thermometer. Under this condition, power dissipation due to the thermometer's output signal can be as little as 1% of the total device dissipation, and thus be negligible in causing temperature error.

The block diagram of *Figure 3* shows how this very high gain is achieved. Integrated on the same chip as the power transistor is an NPN emitter follower driver which is driven by another PNP emitter follower. The emitter-base drops of these two drivers are in the opposite direction, and tend to substantially cancel. Remaining is the emitter-base drop of the power transistor so input signals seem to see a power transistor of normal input voltage but abnormal current gain resulting from the three transistor cascade. Further, the input resistor and integrated PNP transistor allow +40V and −20V overdrives to the base without damage.

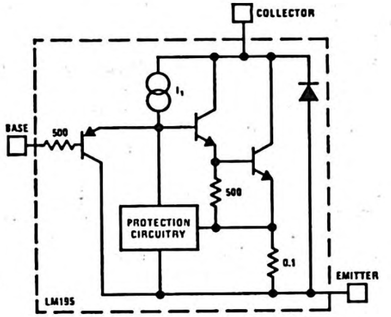


FIGURE 3. Simplified Circuit of the LM195

Reliability under adverse environments is enhanced by other protective circuitry that has been integrated in with this transistor. Collector current is limited to 2 amperes by sensing drop across the 0.1Ω emitter resistor internally. Junction temperature is limited by turning off the output transistor at 170°C junction temperature, using an internal temperature sensor. Thus the LM195 is extremely difficult to destroy except by exceeding collector voltage from a low impedance supply. (2)

APPLICATIONS AREAS

Applications areas will be covered in two sections. First, in the obvious area of temperature sensing and control, several uses with different types of output signals will be illustrated. Then some other sensing functions will be covered. All circuits shown have been breadboarded and are functional, but have not been given field testing at this time.

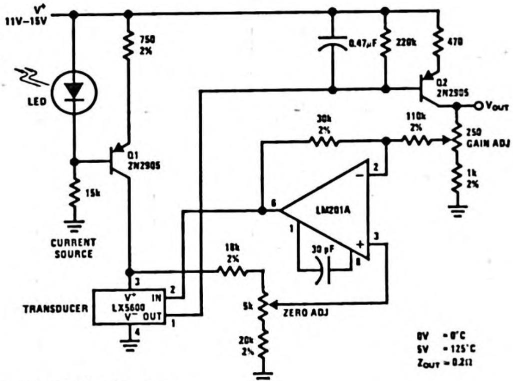
When a 15V supply is shown, the circuit is assumed a lab or instrument application. When a supply varying from 11V to 15V is shown, it is intended that this represent a 12V automotive battery or similar unregulated supply. The circuit has then been tested over a range of 10V to 16V, without significant degradation of performance.

TELEMETRY INTERFACE

Various pieces of mobile test equipment such as instrumentation recorders or telemetry subcarrier VCOs operate best with a calibrated 0 to +5V input. In some cases a low output impedance is also helpful. The LX5600, for certain design reasons, indicates increasing temperature by a negative going voltage with respect to the positive supply pin. Thus the thermometer's output must be inverted, level shifted, and given an extra voltage gain of 4 to provide the illustrated output.

Figure 4 provides the methods of doing this. Q1 supplies the thermometer with a constant current as previously described. The output transistor, Q2, provides the inverting function and requires very little base drive, holding down transducer dissipation. The entire system now requires dc feedback around it to stabilize gain (and thus the full scale calibration) and to eliminate supply and base-emitter voltage variations from the output. Feedback to pin 2 of the transducer is shown (by *Figure 1*) to be the "minus" input to an operational amplifier within the transducer. Thus the output signal needs to be reinverted by the LM201A operational amplifier.

The system has an open loop gain of 5,000 to 10,000, so the attenuation of the output signal that is fed back negatively determines closed loop gain. The reinverting op amp actually has an attenuation of 0.27. The 250Ω pot in the output divider is thus the full-scale adjust and trims the attenuation to 0.25, or a gain of 4. Pin 3 of the transducer provides the voltage reference for the zero adjust divider. At the calibration point of 0°C, the LM201A output must be at a nominal 2.73V below pin 3 of the transducer. Since voltages at both ends of the 30k, 110k network are known at 0°C, it is easy to predict the voltage adjustment at pin 3 of the LM201A required to fulfill this condition.



Op amp pin numbers shown for metal can

FIGURE 4. Telemetry Interface

The 0.47µF capacitor loading the transducer's output is required for stability against oscillations. The system has a very long feedback loop (3 different amplifiers), thus it is extremely easy for the total phase shifts to become 180° at a relatively low frequency. The large capacitor lowers overall gain to less than one at a frequency much less than this. There is no adverse effect on performance since temperature is such a slow moving parameter.

By design, the full-scale adjust has no effect when V_{OUT} is at zero. This means that if zero is calibrated first, and full-scale second, the controls are non-interacting. Calibrating to 4V out, at boiling water temperature may be convenient. The unit we calibrated exhibited a 0.1% independent linearity up to 100°C, and less than 2 mV output change (1/20°C) with a 4V supply change. One little trick is needed for exact zero calibration. Due to loading by the op amp network, a temporary bias of about 0.1 mA is needed at the full-scale pot wiper to read a true zero out. The minus current can be temporarily provided by a 100k resistor and 9V "transistor battery." Obviously, other calibrating points can be chosen, and other ranges can be obtained by changing the different resistor networks.

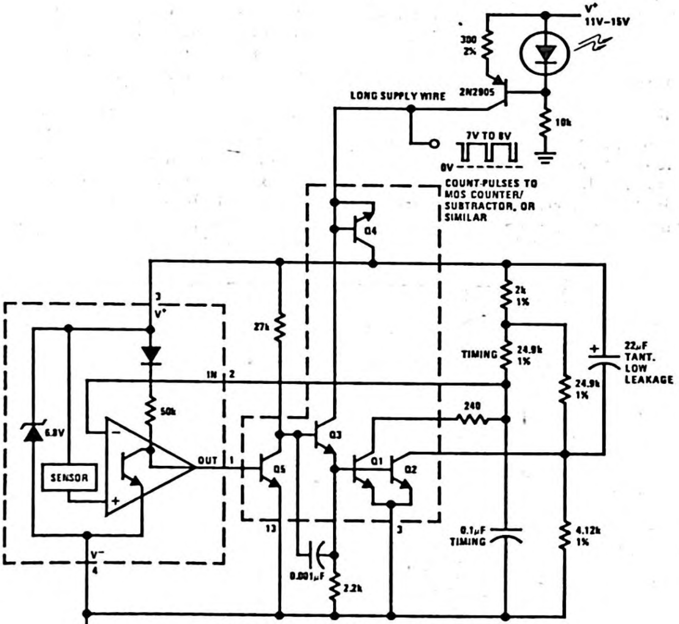
A few precautions may be needed. For maximum accuracy three of the ground points should be common, or brought to the same point with separate wires. These points are the bottoms of the two dividers, and pin 4 of the thermometer. The others are less critical. If long wires, or a noisy supply is anticipated the V^+ pin (pin 7) of the LM201A should be bypassed. Since the V^- pin of the op amp is at ground, resistor networks for other ranges must be such that none of the input or outputs have to go closer than 2V to ground (3V under coldest conditions).

For the purposes of this and other circuits discussed, resistors are all 1/2 watt unless noted, and have the following characteristics. One percent resistors should be high stability metal film or wire wound types (e.g., 50 ppm/°C). Resistors marked 2% can be lower cost medium stability types such as tin oxide. Others can be standard 5% carbon types.

TEMPERATURE TO FREQUENCY CONVERTER

For test data transmission, or to interface conveniently with existing digital displays, a proportional frequency signal may be desirable. In trying to determine the lowest cost package for an automotive exterior temperature indicator, a novel system evolved. It was obvious that a simple circuit in the same protective enclosure as the transducer would minimize cost and wiring. If the single positive supply wire could be made to carry the output signal frequency, it would represent an irreducible minimum cost to hook up.

The above aim was achieved using only the transducer, a very low cost IC (array), a few external parts, and a single supply/output wire. During the short negative output pulses on the supply wire, an internal 22µF capacitor keeps the converter electronics running. Pulse repetition rate is directly proportional to absolute temperature. Again, a LED/transistor constant-current source provides an ideal, modulateable supply from a varying voltage source.



Transistors Q1 through Q5 on LM3046 transistor array

FIGURE 5. Temperature to Frequency Converter

The type of oscillator is similar to a number of "timer" circuits. A capacitor ramps up to a reference voltage, and trips a comparator. The comparator immediately lowers the reference to another fixed point and starts the ramp down. Upon reaching the lower reference the conditions are reversed.

In the converter, there are three slight differences. For one, the run-down of the ramp is made very fast, and contributes negligibly to the timing. Secondly, the upper reference the ramp charges to, moves negatively in linear proportion to temperature. Finally, the lower reference is controlled to be a fixed voltage below the upper at all times. This controls the generated sawtooth to a fixed amplitude at all times. However, since the upper comparison limit moves down with increased temperature, the whole dc level of the sawtooth moves down, increasing voltage across the charging resistor linearly with temperature.

Following are the detailed functions of the various components. The op amp inside the transducer is operated open-loop as a comparator. The 0.1μF timing capacitor is connected directly to the minus input of this amplifier and causes its output to switch "low" when capacitor charge reaches temperature sensor voltage. Transistor Q5 inverts and speeds up the op amp switch transition, and drives the base of Q3. This transistor's collector puts the negative pulse on the supply line, while its emitter drives the bases of Q1 and Q2. As a result, Q1 starts discharging the timing capacitor, and Q2 switches the bottom of the 22μF filter/coupler capacitor to ground.

This is an important step as it determines exactly how far the timing capacitor discharges. It can be seen that due to the large filter capacitor, voltage at the transducer's pin 3 is immediately lowered by the amount of voltage that had appeared across the 4.12k resistor. The sensor and op amp "plus" input follow this drop exactly. Therefore the new comparison point (toward which the timing capacitor is discharging) is lower by exactly the voltage drop of the 4.12k resistor. This voltage sets sawtooth amplitude to about 1V; with the upper and lower limits following temperature as described.

The voltage across a capacitor is predicted by current x time, divided by the capacitance. Since frequency has the units 1/t then:

$$f = \frac{1}{CV} \qquad (1)$$

In other words, frequency will be linear with current change; with a fixed capacitance and a constant voltage change across the capacitance. There are some second order effects due to the slight change of the RC curve as charging percentage varies from about 30% cold to 20% hot. This was measured as less than 2°F out of a range from −68°F to +127°F. It is believed a compensation can be arranged for this small effect.

The remaining transistor, Q4 of the array, is connected so its collector becomes a decoupling diode. When the supply is modulated with the large negative output pulse, the charge on the critical filter/coupling capacitor is not substantially disturbed during the 10μs or so discharge time.

There is a simple, but interesting advantage to the single-package concept for the T/F Converter. Since it shares the same thermal environment with the sensor, linear changes with temperature of the oscillator components can be calibrated out as part of the entire system's frequency change with temperature. This somewhat relaxes the requirement for premium components.

PROBE WITH SERVO'D SHIELD

When only part of a sensor can touch a surface to be measured, it has difficulty reaching the actual surface temperature. This is due to radiative and convective as well as normal conductive effects from all parts not touching the surface. Errors may be 10 or even 20% of the amount by which the surface is hotter than ambient. A very large improvement can be obtained if the sensor is surrounded loosely on all but one side by a thermal shield. The shield should be actively driven to within a degree of the surface temperature.

It sounds like going in circles, (i.e., knowing the surface temperature in order to measure it). However, the system is made to work by having the shield *track* the actual surface temperature sensor. If the coupling between surface and sensor is just a little better than sensor to shield, the whole system converges on a accurate final reading. This explains why there is *insulation* between sensor and shield, while the servo control sensor is soldered directly to the heater transistor.

Figure 6 provides the mechanical details of the system. The LM195 power transistor is both the main power amplifier and heater, being capable of about 23W of heating as shown. Internal current and thermal limit make this a safe and practical mode of operation, and places a great deal of heat in a small area. The system is also surprisingly fast, with the application of heat electrically being sensed within 1/2 second by the servo sensor. The servo sensor is closer to the heat generating silicon die than any of the rest of the system.

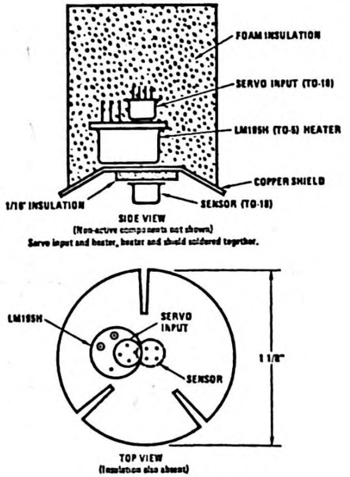


FIGURE 6. Servo'd Shield

Circuitry available inside the LX5700 sensors makes the Servo'd Shield Schematic, *Figure 7*, extremely simple. The close tracking of sensors after adjustment, simply allows the output of the surface sensor to become the setpoint signal for the servo input sensor. The 27 kΩ and 3 MΩ resistors set the servo's op amp gain to about 100. This is needed because the LM195H decreases in required base drive as it heats up, thus appearing to add positive feedback, increasing gain of the system. The 100k/56k divider provides a helpful level shift and absorbs bias current generated by the integrated power transistor.

The 100μF capacitor compensates for an interesting thermal characteristic of the system. Especially at lower temperatures, the power transistor heats at least an order of magnitude faster than it cools. The LX5700 op amp can sink much more current than it sources, so the capacitor establishes a slow turn-on, fast turn-off base signal to the LM195. This compensates the system to prevent large heating overshoots.

Several of the other components need explaining. The diode in series with the sensor ground leg allows the internal zener to be non-conducting, so that pin 3 can be adjusted up or down the 40 to 80 mV necessary to cause the two thermometers to track. A DVM with two digits to the right of the decimal will read directly in °C by moving the point right two places. The meter can be zeroed at 0°C by the 1k trimmer. The heavy filter at the "Lo" or minus input to the DVM is needed because many meters with "floating" input are not well isolated, and inject noise back into the sensing system. The negative going thermometer output at the minus DVM terminal enables the temperature displayed to have the correct sign.

As a cautionary note, the 2-wire ground system as shown is needed to reject feedback caused by initial large heating current surges drawn by the LM195H. Passive components shown as in the probe can be in the foam insulation (on standoffs or a miniature board) but would be better placed above the insulation to avoid heating them to probe temperatures also.

THE ANTICIPATING CONTROLLER

If the conditions are right, and the hardware available, the anticipating controller can be executed rather simply. Normally 2 amplifiers and about 3 different kinds of feedback are required to make a controller stable *and* accurate under varying load conditions. This is due to the unavoidable delay between application of heat and a usable sensor output. The anticipating controller adds a selected amount of phase *leading* signal to the normal amplified output from the temperature sensor. This, at least partially, compensates for the sensing lags.

In the system shown, heater/sensor delays up to about a minute can be compensated for. A simple electronic system can be constructed because of the high sensor output obtainable (100 mV/°C) and the very low bias currents required by the LM216 op amp. This allows use of the 100 MΩ feedback resistor and thus very high differentiator (or anticipating) gain without significant errors. In a test using a heated plate with about a 30 second lag from ideal response, addition of the anticipating signal decreased thermal oscillations from 3° to one or two tenths of a degree.

The LX5700 amplifies its normal 10 mV/°C by about 10 due to the feedback network for its internal op amp. The feedback resistor is the 100k pot and the other gain setting resistance is the series combination of the 5.6k resistor and the setpoint pot resistance at the wiper. The dc gain of the LM216 op amp is set by the 10 MΩ and 100 MΩ resistors at another factor of 10, yielding 1V/°C. Differentiator gain is set by the same 100 MΩ resistance and the 2μF capacitor. A temperature change of 1/20°/second would result in a 1V output if the 100k pot were set to maximum differentiator gain. The 33k resistor in series with the differentiating capacitor, and the 0.001μF feedback capacitor serve to limit high frequency gain and reduce the effects of noise and

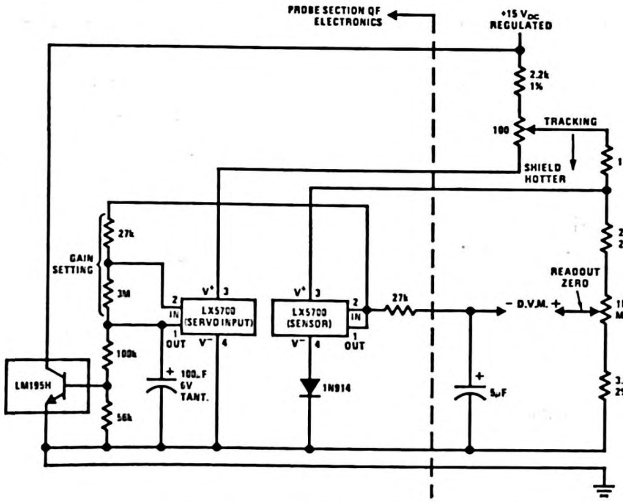
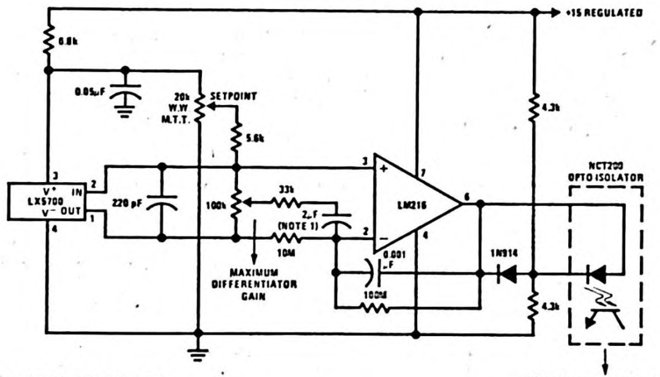


FIGURE 7. Servo'd Shield Schematic


+15 REGULATED
6.8k
0.05µF
20k W.W M.T.T.
SETPOINT
5.6k
4.3k
NCT200 OPTO ISOLATOR
3
V+ IN
LX5700
V− OUT
4
2
1
220 pF
100k
33k
2µF (NOTE 1)
10M
MAXIMUM DIFFERENTIATOR GAIN
LM216
7
6
4
3
2
0.001 µF
100M
1N914
4.3k

TO POWER TRANSISTOR CONTROL OR NARROW BAND PROPORTIONING S.C.R. CONTROL (LED "ON" FOR POWER "OFF") (NOTE 2)

Note 1: Must be low leakage film dielectric type.
Note 2: Connections to LED and diode can just be reversed for reverse control action.

FIGURE 8. Anticipating Controller

pickup which can otherwise be greatly emphasized in a differentiator.

The output circuit energizes the opto-isolator when the op amp output swings somewhat above the supply centertap set by the two 4.3k resistors. Depending on divider value, current gain of the coupler, and sensitivity of its load, almost arbitrarily small changes of temperature or *rate* of temperature change may control heating or cooling. In some cases gain will have to purposely be reduced to get a stable control point.

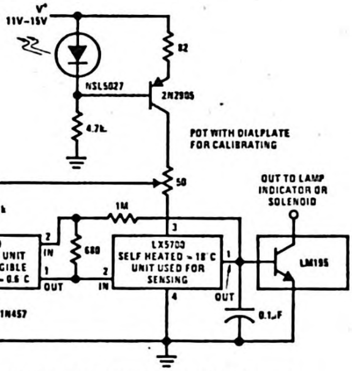
OTHER SENSING FUNCTIONS

Temperature is easy, but what about temperature difference? Monolithic transducers are very good at sensing this because of their close tracking and the capability of delivering from tens of millivolts to many volts of output for each °C of temperature difference. Any physical process that generates a small temperature gradient to ambient or a reference can be sensed by a pair of transducers. This potentially involves chemical processes, friction, compression of gasses, radiation, evaporation, and a whole raft of heat generating or absorbing phenomena. Three rather simple such applications will be illustrated.

Liquid or Moving Air Detection

Figure 9 shows a basic 2 sensor configuration for performing a number of differential temperature functions. As noted, one sensor is heated considerably by internal dissipation, and the other is biased slightly lower at supply voltage pin 3 so that if the "hot" sensor lost half its excess heat, its output (operating essentially open loop) will switch to a "high" state. This of course turns on the power transistor. The feedback network consisting of a 1M resistor and 680Ω resistor provides slightly less than 1/2°C hysteresis or snap action which prevents partial outputs or oscillation near the setpoint.

Adjustments are not too critical due to the large temperature differences that are created. Cooling of the sensing unit by an electrically non-conducting liquid (such as oil) is about 16°C. Still liquid was used for the measurement. Air at about 400 FPM (a little under 5 mph) provides about 10°C cooling.


V+
11V–15V
82
NSL5027
2N2905
4.7k
POT WITH DIALPLATE FOR CALIBRATING
50
OUT TO LAMP INDICATOR OR SOLENOID
1k
1M
3
2
IN
680
3
LX5700 REFERENCE UNIT WITH NEGLIGIBLE SELF HEAT, ≈ 0.6°C
1
OUT
2
IN
LX5700 SELF HEATED ≈ 18°C UNIT USED FOR SENSING
1
OUT
4
4
LM195
1N457
0.1µF

Output "OFF" if sensing unit becomes hot, i.e., out of liquid or airstream.
Reference unit is 1 inch from the sensing unit in airstreams, and below the sensor in liquid sensing systems.

FIGURE 9. Liquid or Moving Air Detection

For either application the adjustment is fairly simple. With the sensing transducer in the "hot" condition (still-air, or out of liquid for 2 minutes) find the pot setting that just turns the power output off. Tnen with the sensing transducer in the cool condition (in liquid or moving air) for 30 seconds, find the setting that just turns the output on. Since these two settings "overlap," a final setting between these two will provide stable operation. If it is noted that response in the heating direction is markedly slower, displacing the adjustment toward the "cool" setting (referring to the pot dialplate) can partially compensate for this.

If the detector is used as a failsafe sensor in a system cooled by a fan, the sensor's self-heating delay gives time for said cooling fan to come up to speed without requiring a special delay or override for system start-up. Speed of response can have good or bad effects on the over-all system. The sensors are essentially slow enough so that momentary air blockage or liquid splashing won't give erroneous signals. In liquid sensing, drops adhering to the sensing transducer can slow it down by 2 or 3 to 1. A "drip point" such as 3/8" long piece of #28 bare wire soldered to the lowest part of the case helps. Insulating supports, or lead insulation, within 1/2" of the sensing LX5700 slows it down considerably.

Wind Velocity

Actual "air speed" has more effect on gasoline mileage than road speed at above 40 mph. Further there is great interest by sailboat racers as to wind velocity or air speed. Again, a differential between a heated and unheated transducer can be used in this sensing job.

Briefly, the setpoint input (pin 2) of the transducer that is to sense velocity, is biased so that its voltage is always equivalent to a number of degrees above ambient. This voltage is obtained by adding a small dc level to the output of an ambient sensing transducer. The output of the velocity transducing LX5700 is used to control its own heating; holding it the specified number of degrees above ambient. The current to do this is measured, and is obviously a measure of the amount of heating required. As wind velocity rises, so does this current as the transducer "servo's" its temperature to a constant amount above ambient.

In *Figure 10* this amount of heating is set by the wiper voltage of the 20k pot into the 100k/4.12k divider. The bottom of this divider is driven by the LX5600 air temperature reference, connected in unity gain mode. The output of the velocity sensor drives the base of Q1. If this sensor cools, Q1 base goes positive, reducing its emitter current and collector current. The current drawn by the 620Ω collector load doesn't change significantly however. The current now *not* supplied by Q1 is drawn instead through D2, through the meter, and eventually through the reference zener of the velocity sensor. This of course heats the sensor, closing the feedback loop.

The system is made electrically stable by the 0.1 compensating capacitor and the fact that Q1 exhibits practically no collector voltage gain. Q2 is not normally conducting, but it and the divider on its base provide a clamp voltage for the Q1 collector. This prevents a "latchup" mode that occurs if Q1 happens to draw a transient current pulse. The "zero velocity current" adjustment allows this heating current needed at zero velocity to bypass the meter. To avoid a low velocity discontinuity, it is probably best to "zero" the meter at about 1% of full scale.

Sensor Arrangement as shown in *Figure 11*, minimizes the sensitivity of the system to vertical components of wind, and limits the exposed part of the sensor to a controlled area (no lead effects, etc.) which has uniform nondirectionality in the horizontal plane. The breadboard used Balsa wood due to its good insulation qualities *and* very low thermal mass. In the field consideration should be given to prevention of water absorption. No thermal air velocity system will give correct data in rain or dense fog.

The current vs airspeed curve shows the typical decreasing sensitivity with increasing velocity, but a good calibration curve has not been obtained at this time through lack of instrumentation. Response speed is decidedly slower than that of thermocouple types, but in some cases this may be an advantage, such as in determining average airspeed on a gusty day.

Position Sensing

This may be the most novel or, on the other hand, strangest of the applications shown. Under certain conditions however, the very considerable position "integration" due to the thermal mass of the sensor may make this system quite practical, and much less expensive than electronic filtering. As shown in *Figures 12 and 13* the essence of the system is a small sliding *heater* acting as a position transmitter. The receiver is a brass tube which allows the total heater output to be transmitted out toward the ends. The temperature reached at each end is proportional to heater position.

Logically, with the heater in the center, both ends reach the same temperature. With the heater at one end, that end is about 50°C warmer than ambient, and

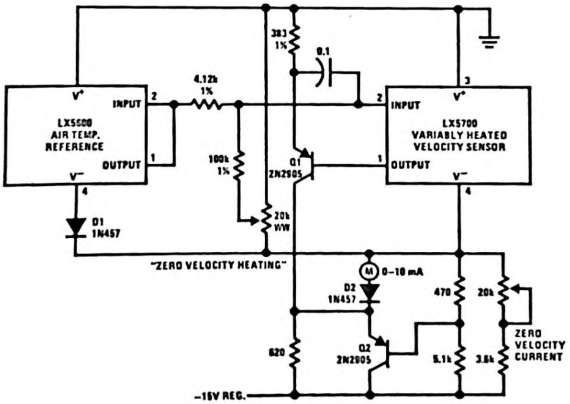


FIGURE 10. Air Velocity Meter

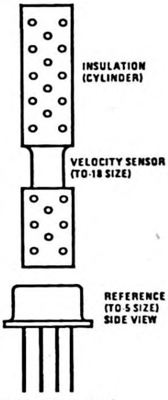
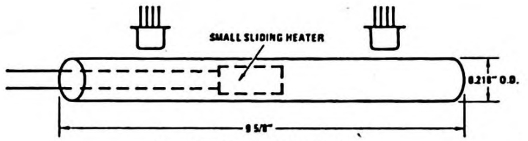


FIGURE 11. Sensor Arrangement



Thin wall brass tube with an LX5700 soldered on 7/8" from each end. Mount horizontally in still air.

FIGURE 12. Position Sensor Tube

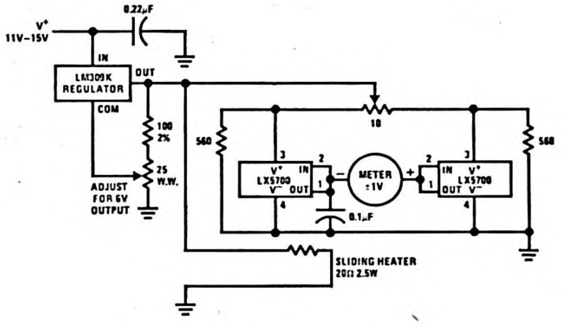


FIGURE 13. Position Sensor Schematic

the other end is near ambient. As the heater moves toward one end, one thermometer becomes more sensitive, and the other less. The differential effects tend to cancel, and the first breadboard unit had a temperature difference linearity within 4% relative to measured position. The heater must stay *between* the sensors to achieve this, with the extra length of tube at the ends helping to linearize the system.

The electrical system powers the sensors at minimum dissipation, and regulates heater power to keep position "gain" constant. The pot simply allows an electrical zero of the two thermometers and meter, which can be done with the heater off. The meter can be a 2 polarity DVM with 600 mV to 1V full scale, or a zero centered mechanical meter with similar deflection either side of zero.

The system takes 2 to 3 minutes to reach 98% of final reading. This may make it a very good position *averaging* system in cases where there is high amplitude vibration. Average truck spring deflection could be read while it is rolling along a rough road for instance. The system will have less wear problems than a sliding position pot and be less expensive than a Linear Variable Transformer system. It may also be useful in a position servo system that needs very heavy filtering.

SUMMARY AND CONCLUSIONS

Since the monolithic temperature transducer is a relatively new and unique device, this has been primarily an applications paper attempting to broaden the base of practical Integrated Circuit usage. Some general techniques were explained and seven specific systems have been described in construction and performance. Hopefully these concepts will remain after the details are forgotten.

First, there are many considerably different schemes for temperature control or measurement based on the versatility of a transducer that has both amplifying and regulating capability in the same package. This three circuits in one package availability allows consideration of systems that formerly would have been too expensive or complex.

Secondly, the ease of accurately sensing small temperature *differences* leads to sensors for other than just temperature sensing. Sensing liquids, air velocity, and mechanical position have been demonstrated, and other possibilities include rate-of-rise sensors for fire detection, RMS regulators, and humidity gauges. It will be interesting to see what others turn up that we have missed.

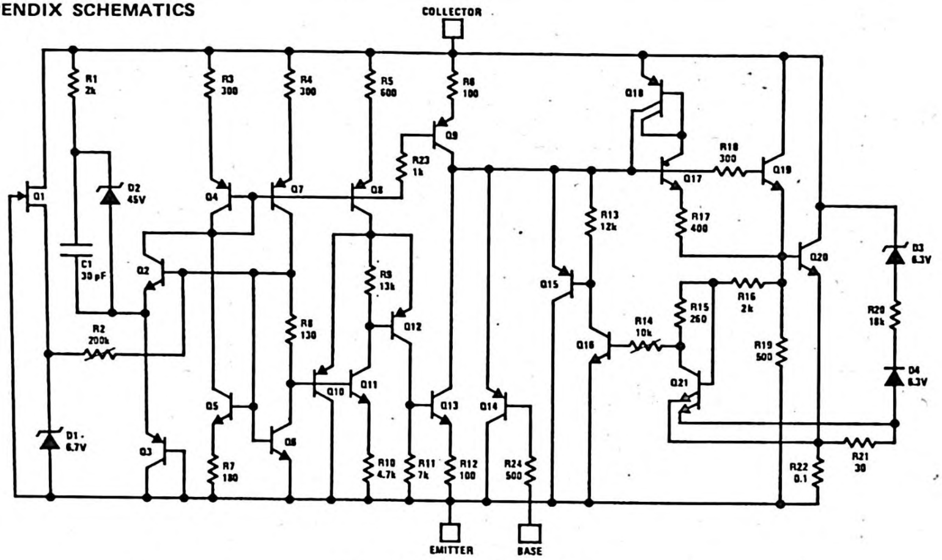
REFERENCES

(1) Robert C. Dobkin, *1.2 Volt Reference,* National Semiconductor Corporation Application Note 56, December 1971.

(2) Robert C. Dobkin, *Fast IC Power Transistor with Thermal Protection*, National Semiconductor Corporation Application Note 110, May 1974.

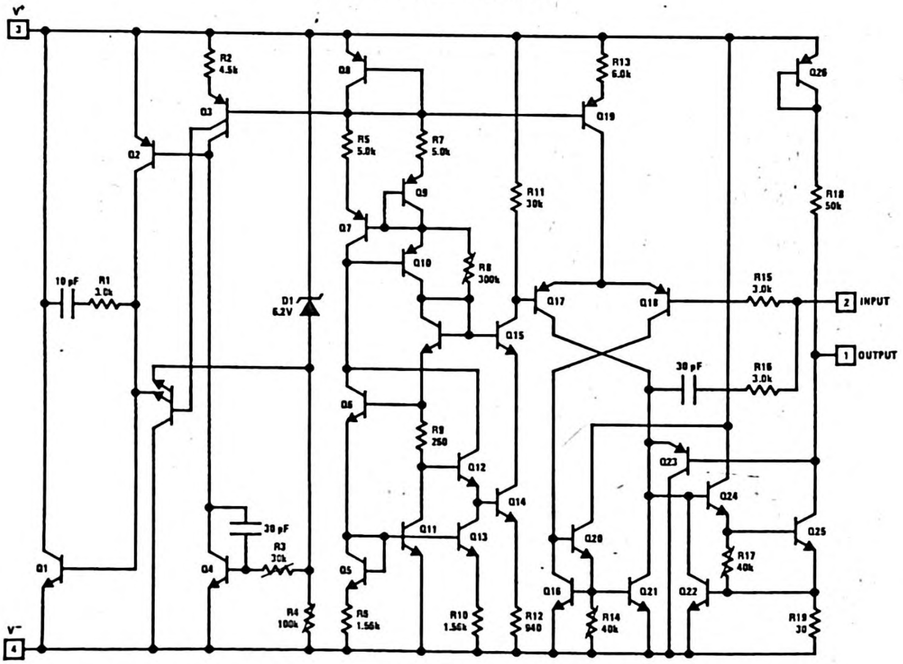
(3) *Transducers, Pressure & Temperature,* National Semiconductor Corporation catalog and handbook, August 1974.

APPENDIX SCHEMATICS



COLLECTOR
R1 2k
R3 300
R4 300
R5 600
R6 100
Q18
Q9
R23 1k
R18 300
Q19
Q1
D2 45V
Q4
Q7
Q8
Q17
R13 12k
R17 400
C1 30 pF
Q2
R9 13k
Q20
D3 6.3V
Q15
R16 2k
R15 250
R20 18k
R2 200k
R8 130
Q12
R14 10k
Q16
R19 500
Q10
Q11
Q21
D4 6.3V
Q5
Q13
Q14
D1 6.7V
Q3
Q6
R7 180
R10 4.7k
R11 7k
R12 100
R24 500
R22 0.1
R21 30
EMITTER
BASE

Schematic Diagram of the LM195



V⁺
3
R2 4.5k
Q8
R13 6.0k
Q26
Q3
Q19
Q2
R5 5.0k
R7 5.0k
Q9
R11 30k
R18 50k
Q7
Q10
R8 300k
10 pF
R1 3.0k
D1 6.2V
Q17
Q18
R15 3.0k
2 INPUT
Q15
1 OUTPUT
30 pF
R16 3.0k
Q6
R9 250
Q23
Q12
Q24
Q14
30 pF
R3 30k
Q11
Q13
Q20
Q25
Q1
Q4
Q5
R17 40k
Q16
Q21
Q22
R4 100k
R6 1.56k
R10 1.56k
R12 940
R14 40k
R19 30
V⁻
4

Schematic Diagram of the LX5600/LX5700

FM Remote Speaker System

National Semiconductor
Application Note 146
Jim Sherwin
Nello Sevastopoulos
Tim Regan
June 1975

AN-146 FM Remote Speaker System

INTRODUCTION

A high quality, noise free, wireless FM transmitter/receiver may be made using the LM566 VCO and LM565 PLL Detector. The LM566 VCO is used to convert the program material into FM format, which is then transformer coupled to standard power lines. At the receiver end the material is detected from the power lines and demodulated by the LM565.

The important difference between this carrier system and others is its excellent quality and freedom from noise. Whereas the ordinary wireless intercom uses an AM carrier and exhibits a poor signal-to-noise ratio (S/N), the system described here uses an FM carrier for inherent freedom from noise and a PLL detection system for additional noise rejection.

The complete system is suitable for high-quality transmission of speech or music, and will operate from any AC outlet anywhere on a one-acre homesite. Frequency response is 20-20,000 Hz and THD is under ½% for speech and music program material.

Transmission distance along a power line is at least adequate to include all outlets in and around a suburban home and yard. Whereas many carrier systems operate satisfactorily only when transmitter and receiver are plugged into the same side of the 120-240V power service line, this system operates equally well with the receiver on either side of the line.

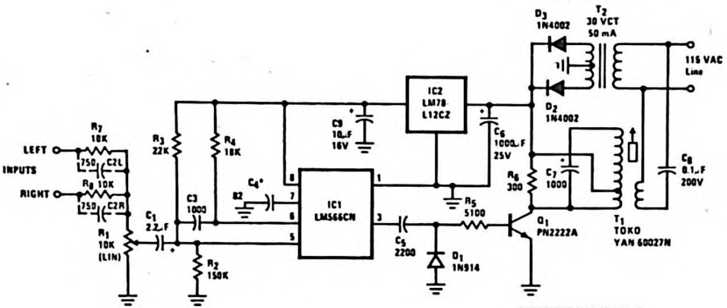
The transmitter is plugged into the AC line at a radio or stereo system source. The signal for the transmitter is ideally taken from the MONITOR or TAPE OUT connectors provided on component system Hi-fi receivers.. If these outputs are not available, the signal could be taken from the main or extra speaker terminals, although the remote volume would then be under control of the local gain control. The carrier system receiver need only be plugged into the AC line at the remote listening location. The design includes a 2.5W power amplifier to drive a speaker directly.

TRANSMITTER

Two input terminals are provided so that both LEFT and RIGHT signals of a stereo set may be combined for mono transmission to a single remote speaker if desired.

The input signal level is adjustable by R_1 to prevent over-modulation of the carrier. Adding C_2 across each input resistor R_7 and R_8 improves the frequency response to 20 kHz as shown in *Figure 5.* Although casual listening does not demand such performance, it could be desired in some circumstances.

The VCO free-running frequency, or carrier frequency f_c, determined by R_4 and C_4 is set at 200 kHz which is high enough to be effectively coupled to the AC line. VCO sensitivity under the selected bias conditions with $V_s = 12V$ is about ±0.66 f_c/V. For minimum distortion, the deviation should be limited to ±10%; thus maximum input at pin #5 of the VCO is ±0.15V peak. A reduction due to the summing network brings the required input to about 0.2V rms for ±10% modulation of f_c, based on nominal output levels from stereo receivers. Input potentiometer R_1 is provided to set the required level. The output at pin #3 of the LM566, being a frequency modulated square wave of approximately 6V pk-pk amplitude, is amplified by a single transistor Q_1 and coupled to the AC line via the tuned transformer T_1. Because T_1 is tuned to f_c, it appears as a high impedance collector load, so Q_1 need not have additional current limiting. The collector signal may be as much as 40-50V pk-pk. Coupling capacitor C_8 isolates the transformer from the line at 60 Hz.

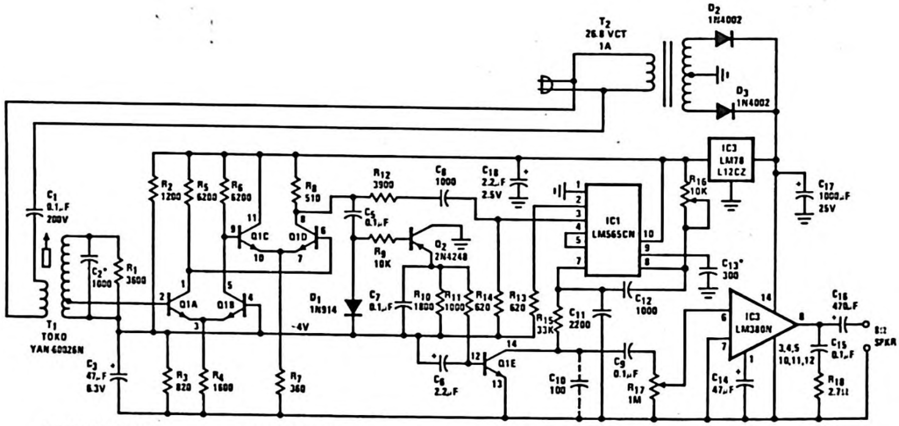


D3 1N4002
T2 30 VCT 50 mA
115 VAC Line
IC2 LM78L12CZ
C9 10μF 16V
C6 1000μF 25V
D2 1N4002
C8 0.1μF 200V
R7 10K
LEFT
INPUTS
RIGHT
750
C2L
R8 10K
C2R
R1 10K (LIN)
C1 2.2μF
R3 22K
R4 18K
C3 1000
C4† 82
IC1 LM566CN
R2 150K
C5 2200
D1 1N914
R5 5100
R6 300
C7 1000
Q1 PN2222A
T1 TOKO YAN 60027N

CAPACITOR VALUES IN pF
RESISTOR VALUES IN Ω
†SELECT FOR CARRIER FREQ.

f_c	C_4	C_7
200 kHz	82	1000
100 kHz	160	3900

FIGURE 1. Carrier System Transmitter



T2 26.8 VCT 1A
D2 1N4002
D3 1N4002
IC3 LM78L12CZ
C17 1000μF 25V
C1 0.1μF 200V
R2 1200
R5 6200
R6 6200
R8 510
R12 3900
C8 1000
C18 2.2μF 2.5V
IC1 LM565CN
R16 10K
C5 0.1μF
R9 10K
Q2 2N4248
Q1C
Q1D
Q1A
Q1B
Q1E
C2* 1000
R1 3600
T1 TOKO YAN 60026N
D1 1N914
C7 0.1μF
R10 1800
R11 1000
R14 620
R13 620
R15 33K
C11 2200
C12 1000
C13* 300
IC3 LM380N
C16 470μF
8Ω SPKR
-4V
C3 47μF 6.3V
R3 820
R4 1600
R7 360
C6 2.2μF
C10 100
C9 0.1μF
R17 1M
C14 47μF
C15 0.1μF
R18 2.7Ω

CAPACITOR VALUES IN PF
RESISTOR VALUES IN Ω
*SELECT FOR CARRIER FREQ.

f_o	C_2	C_{13}
200 kHz	1000	300
100 kHz	3900	620

Q1A–Q1E = LM3046

FIGURE 2. Carrier System Receiver

A voltage regulator provides necessary supply rejection for the PLL. The power transformer is sized for peak secondary voltage somewhat below the regulator breakdown voltage spec (35V) with a 125V line.

RECEIVER

The receiver amplifies, limits, and demodulates the received FM signal in the presence of line transient interference sometimes as high as several hundred volts peak. In addition, it provides audio mute in the absence of carrier and 2.5W output to a speaker.

The carrier signal is capacitively coupled from the line to the tuned transformer T_1. Loaded Q of the secondary tank T_1C_2 is decreased by shunt resistor R_1 to enable acceptance of the ±10% modulated carrier, and to prevent excessive tank circuit ringing on noise spikes. The secondary of T_1 is tapped to match the base input impedance of Q_{1A}. Recovered carrier at the secondary of T_1 may be anywhere from 0.2 to 45V p-p; the base of Q_{1A} may see pk-to-pk signal levels of from 12mV to 2.6V.

Q_{1A}-Q_{1D} operates as a two-stage limiter amplifier whose output is a symmetrical square wave of about 7V pk-pk with rise and fall times of 100 ns.

The output of the limiting amplifier is applied directly to the mute peak detector, but is reduced to 1V pk-pk for driving the PLL detector.

The PLL detector operates as a narrow band tracking filter which tracks the input signal and provides a low-distortion demodulated audio output with high S/N. The oscillator within the PLL is set to free-run ot or near the carrier frequency of 200 kHz. The free-run frequency is $f_o \approx 1/(3.7\ R_{16}C_{13})$. Since the PLL will lock to a carrier near its free-run frequency, an adjustment of R_{16} is not strictly necessary; R_{16} could be fixed at 4700 or 5100Ω. Actually, the PLL with the indicated value of C_{11} can lock on a carrier within about ±40 kHz of its center frequency. However, rejection of impulse noise in difficult circumstances can be maximized by carefully adjusting f_o to the carrier frequency f_c. Adding C_{10} = 100 pF will reduce the carrier level fed to the power amplifier. Even though the listener cannot hear the carrier, the audio amplifier could overload due to carrier signal power.

A mute circuit is included to quiet the receiver in the absence of a carrier. Otherwise, when the transmitter is turned OFF, an excessive noise level would result as the PLL attempts to lock on noise. The mute detector consists of a voltage doubling peak detector $D_1Q_2C_7$. The peak detector shunts the 1-2 mA bias away from Q_{1E} without loading the limiter amplifier. When no carrier is present, the +4V line biases Q_{1E} ON via R_{10} and R_{11}; and the audio signal is shorted to ground. When a carrier is present, the 7V square wave from the limiter amplifier is peak detected, and the resultant negative output is integrated by R_9C_7, averaged by R_{10} across C_7, and further integrated by $R_{11}C_6$. The resultant output of about −4V subtracts from the +4V bias supply, thus depriving Q_{1E} of base current. Peak detector integration and averaging prevents noise spikes from deactivating the mute in the absence of a carrier when the limiter amplifier output is a series of narrow 7V spikes.

The LM380 supplies 2.5W of audio power to an 8 ohm load. Although this is adequate for casual listening in the kitchen or garage, for hi-fi listening, a larger amplifier may be desired.

CONSTRUCTION

PC board layout and stuffing diagrams are shown in *Figures 3 & 4.* After the receiver board has been loaded and checked, the power transformer is mounted to the foil side of the board with a piece of fish-paper or electrical insulating cloth between board and transformer. Insulating washers of 1/16-1/4 inch thickness can be used to advantage in holding the transformer away from the foil. The board is laid out so that the volume control potentiometer may be mounted on either side of the board depending on the desired mounting to a panel.

The line coupling coils are available in production quantities from TOKO AMERICA INC, 5520 West Touhy, Skokie, IL.

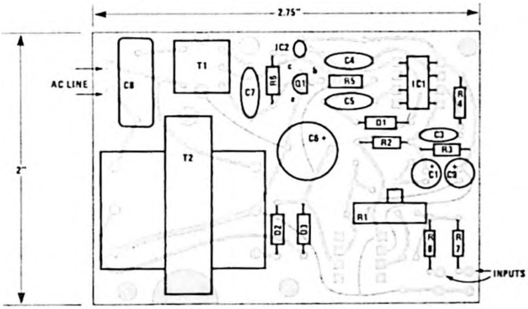


FIGURE 3. Carrier System Transmitter PC Layout and Loading Diagram (Not Full Scale)

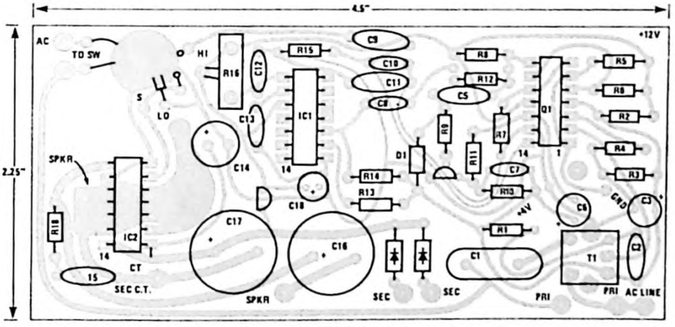


FIGURE 4. Carrier System Receiver PC Layout and Loading Diagram (Not Full Scale)

ADJUSTMENT

Adjustments are few and extremely simple. Transmitter carrier frequency f_c is fixed near 200 kHz by R_4 and C_4; the exact frequency is unimportant. T_1 for both transmitter and receiver are tuned for maximum coupling to and from the AC line. Plug in both receiver and transmitter; no carrier modulation is necessary. Insure that both units are operative. Observe or measure with an AC VTVM the waveform at T_1 secondary in the receiver. Tune T_1 of the transmitter for maximum observed signal amplitude. Then tune T_1 of the receiver for a further maximum. Repeat on the transmitter, then the receiver. Tuning is now complete for the line coupling transformers and should not have to be repeated for either. If the receiver is located some distance from the transmitter in use, or on the opposite side of the 110-220V service line, a re-adjustment of the receiver T_1 may be made to maximize rejection of SCR dimmer noise. The receiver PLL free-running frequency is adjusted by R_{16}. Set R_{16} near the center of its range. Rotate slowly in either direction until the PLL loses lock (evidenced by a sharp increase in noise and a distorted output). Note the position and then repeat, rotating in the other direction. Note the new position and then center R_{16} between the two noted positions. A fine adjustment may be made for minimum noise with an SCR dimmer in operation. The final adjustment is for modulation amplitude at the transmitter. Connect the audio signal to the transmitter input and adjust the input potentiometer R_1 for a signal maximum of about 0.1V rms at the input to the LM566. Adjustment is now complete for both transmitter and receiver and need not be repeated.

A STEREO SYSTEM

If full stereo or the two rear channels of a quadraphonic system are to be transmitted, both transmitter and receiver must be duplicated with differing carriers. Omit R_8 and include R_7 & C_2 on the transmitter if desired. Carriers could be set to 100 and 200 kHz for the two channels. Actually, they need only be set a distance of 40 kHz apart.

PERFORMANCE

Overall S/N is about 65 dB. Distortion is below about 1/4% at low frequencies, and in actual program material it should not exceed 1/2% as very little signal power occurs in music above about 1 kHz.

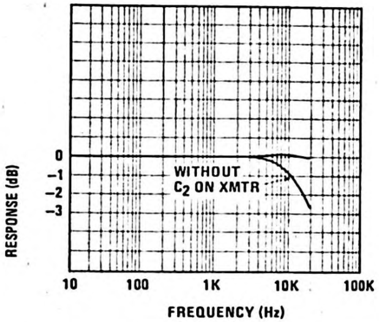


FIGURE 5. Overall System Performance Transmitter Input to Input of Receiver Power Amplifier

The 2.5W audio amplifier provides an adequate sound level for casual listening. The LM380 has a fixed gain of 50. Therefore for a 2.5W max output, the input must be 89 mV. This is slightly less than the ±10% deviation level so we are within design requirements. Average program level would run a good 10 dB below this level at 28 mV input.

Noise rejection is more than adequate to suppress line noise due to fluorescent lamps and normal line transients. Appliance motors on the same side of the 110-220V line may produce some noise. Even SCR dimmers produce only a background of impulse noise depending upon the relative location of receiver and SCR. Otherwise, performance is noise-free anywhere in the home. Satisfactory operation was observed in a factory building so long as transmitter and receiver were connected to the same phase of the three-phase service line.

APPLICATIONS

Additional applications other than home music systems are possible. Intercoms are one possibility, with a separate transmitter and receiver located at each station. A microphone can serve as the source material and the system can act as a monitor for a nursery room. Background music may be added to existing buildings without the expense of running new wiring.

AN-147 Low Cost IC Stereo Receiver

Low Cost IC Stereo Receiver

National Semiconductor
Application Note 147
Dennis Bohn
Jim Sherwin
June 1975

INTRODUCTION

The recent availability of a broad line of truely high-performance consumer integrated circuits makes it possible to construct a high quality, low noise, low distortion and low cost AM/FM/Stereo receiver, Design emphasis is placed on a high level of performance, minimum factory adjustments and low parts count. As such, the receiver has immediate applications to table-top, high-fidelity, automotive and communications markets.

Provisions are included for the addition of a ceramic phono unit as well as a tapehead amplifier allowing inclusion of eight-track or cassette transport systems. Complete tone control circuitry is provided offering both boost and cut of Bass and Treble frequencies. Left and right channel Balance, and system Volume complete the manual front-panel controls.

Panel meters are employed in the FM system for both signal strength and center tuning, allowing for easy and accurate tuning. A directly driven LED offers immediate indication of FM stereo reception.

The complete design requires just five IC's, restricting the use of discrete active elements to the preassembled FM front-end and the single transistor tone control design.

FM and FM STEREO

A preassembled front-end was selected as the cost-effective approach to minimum parts count and minimum factory adjustments. This model features an FET input stage providing excellent distortion performance. High selectivity is obtained thru the use of two cascaded ceramic filters yielding an approximate 6-pole response with less than 12 dB insertion loss.

The LM3089 FM IF System does all the major functions necessary for FM processing, including a three stage amplifier/limiter and balanced product detector, as well as an audio preamplifier. A single quadrature coil was used for ease of alignment; yielding recovered audio with THD less than 0.5%, however a double coil may be used to diminish THD to 0.1% if required. Carrier level detectors provide delayed AGC, SIGNAL strength meter drive, and adjustable interstation mute control R_{11}. The internal AFC amplifier was used to drive the TUNING meter, giving a visual indication of center tuning.

FM stereo demodulation is accomplished by the use of the LM1800 phase locked loop, thereby eliminating the need for external coils. Only two adjustments are necessary: R_{14}, which sets the 19 kHz oscillator, and R_{17},

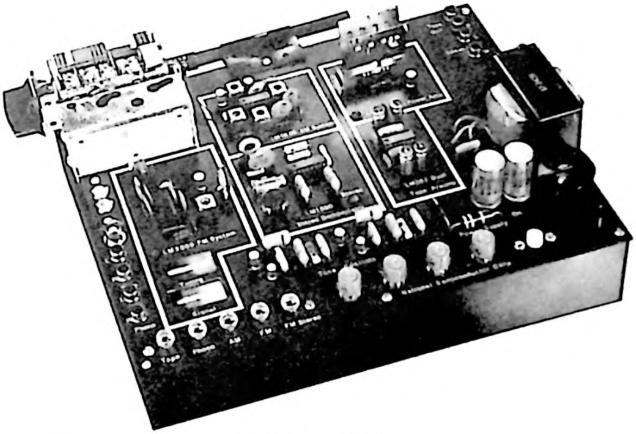


FIGURE 1. IC Receiver

which corrects for excess phase shift thru the IF stages, and yields maximum channel separation. Automatic stereo/monaural switching is built-in, and may be used in lieu of mechanical switching if desired. The open collector lamp driver is used to light a LED whenever a stereo station is encountered. (Further details available from application note AN-81.)

AM

The AM function of the receiver is done completely with the LM1820 AM radio system. While designed for 3 section tuned superheterodyne applications, the LM1820 may be used with the less expensive 2 section tuned designs by omitting the RF stage and redefining its function as 2ND IF stage (see linear brief LB-29). As shown, the LM1820 provides the necessary converter/oscillator, IF, and AGC detector functions, while the external diode D_1 does the audio demodulation, D_1 is slightly forward biased thru R_2 for improved distortion performance. In addition its resistance is used in conjunction with C_9 to form the first stage of the required low pass filter; the second stage consists of R_3 and C_{10}.

TAPE

The LM382 dual preamplifier was selected for its minimum parts count and low noise capability. With a guaranteed maximum equivalent input noise voltage of 1.2μVrms (10 kHz BW), it easily amplifies the low level tape signals while retaining excellent S/N ratio (~64 dB below 2 mV input level). An ion-implanted resistor matrix is supplied on the chip for self-biasing the output to half-supply, and provides the resistors necessary to create the NAB equalization curve; requiring only four external capacitors per channel to complete the amplifier. For production models this preamplifier would normally be mounted directly on the tape player to minimize hum and noise pick-up.

TONE CONTROLS

A single transistor tone control circuit was designed as the optimum cost/performance trade-off. The transistor is configured in a shunt-shunt feedback design, allowing gain variations between input functions. This is necessary to prevent sudden changes in output level when different inputs are selected. With a shunt feedback design the gain is easily controlled by choice of source impedance per *Figure 5.*

Approximately 20 dB of boost or cut of Bass and/or Treble frequencies is possible with the network shown. The turnover frequencies are approximately 500 Hz and 1600 Hz for bass and treble, respectively. The insertion loss of approximately 27 dB is made up by the gain of the transistor tone control amplifier. Balance and Volume controls are included as shown. Loudness control may be included by using a tapped Volume pot and the associated bass boost RC network if desired. More elaborate tone controls such as Baxandall feedback are possible, but at a premium in cost.

POWER AMPLIFIER

The stereo power section, consisting of the LM378 dual audio amplifier, delivers 3W/channel with total harmonic distortion (THD) less than 1%, and 4W/channel with THD less than 10%, operating from split supply voltages of ±11V. Split supplies were chosen to facilitate a minimum parts count design. This approach allows direct coupling of the amplifier to the speakers since the output DC level is zero volts (offset voltage will be less than 25 mV), thereby eliminating the need of large coupling capacitors and their associated degradation of power, distortion and cost. Since the input bias voltages are zero volts, the need for bias resistors and the bias-pin supply bypassing capacitor are also eliminated. Input capacitors are omitted and bias current for the positive input is obtained directly thru the Volume pots since the tone control circuitry has been designed such that there is no DC potential applied.

It is important to apply proper supply voltages and adequate heatsinking in using the LM378 (see application note AN-125). Note that while the standby and low output power operating points of the power supply are ±15V, the maximum power out point causes the supply to sag to ±11V therefore reducing package power dissipation to acceptable levels. Socketable heatsinking is possible using a Staver V7-5 heatsink soldered directly to the center three pins on both sides of the LM378.

POWER SUPPLY

The worst case ripple rejection of 45 dB for the IC's used allows for a simple unregulated power supple, however the discrete front-end and tone control amplifiers require some regulation to preserve the IC performance. A single zener diode Z_1 was selected to create a +12V supply for this function. The split supplies required for the power amplifier are derived from a conventional full-wave bridge rectifier operating off of the center-tapped secondary of the line transformer.

REFERENCES

1. Isbell, T.D. and Mishler, D.S., *"LM1800 Phase Locked Loop FM Stereo Demodulator."* National Semiconductor Application Note AN-81, June 1973.

2. Papanicolaou, E.S. and Mortensen, H.H., *"Low-Cost AM-Radio System Using LM1820 And LM386."* National Semiconductor Linear Brief LB-29, May 1975.

3. Sherwin, J., *"LM377, LM378 And LM379 Dual Two, Four, And Six Watt Power Amplifiers."* National Semiconductor Application Note AN-125, January 1975.

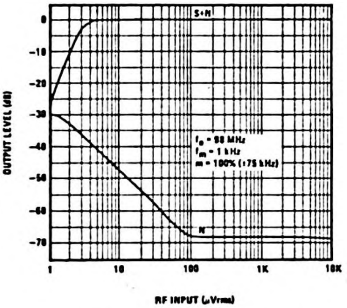


FIGURE 2. FM Sensitivity

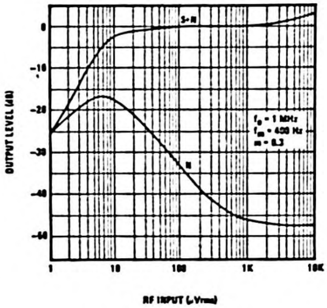


FIGURE 3. AM Sensitivity

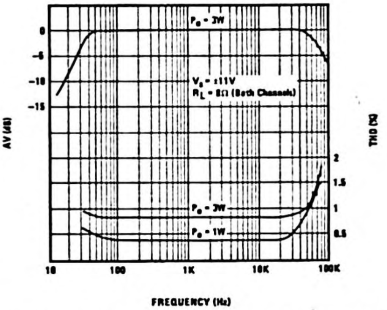


FIGURE 4. Power Amplifier Frequency Response and Total Harmonic Distortion

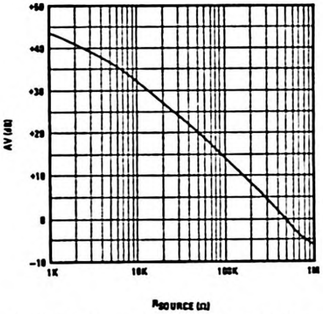


FIGURE 5. A_V vs. R_{SOURCE} for Tone Control Preamplifier Stage.

SPECIFICATIONS

FM-MONO

Sensitivity: 2.5μV for 30 dB quieting
Harmonic Distortion: 0.3%
Hum & Noise: −65 dB
Frequency Response: 50-15 kHz ±3 dB

FM-STEREO

Channel Separation: 45 dB
Harmonic Distortion: 0.4%

AM

Sensitivity: 20μV for 20 dB S+N/N
Harmonic Distortion: 2%
Hum & Noise: −45 dB

TAPE

Frequency Response: NAB equalized ±2 dB
Harmonic Distortion: 0.3%
Hum & Noise: −64 dB below 2 mV input level

AMPLIFIER

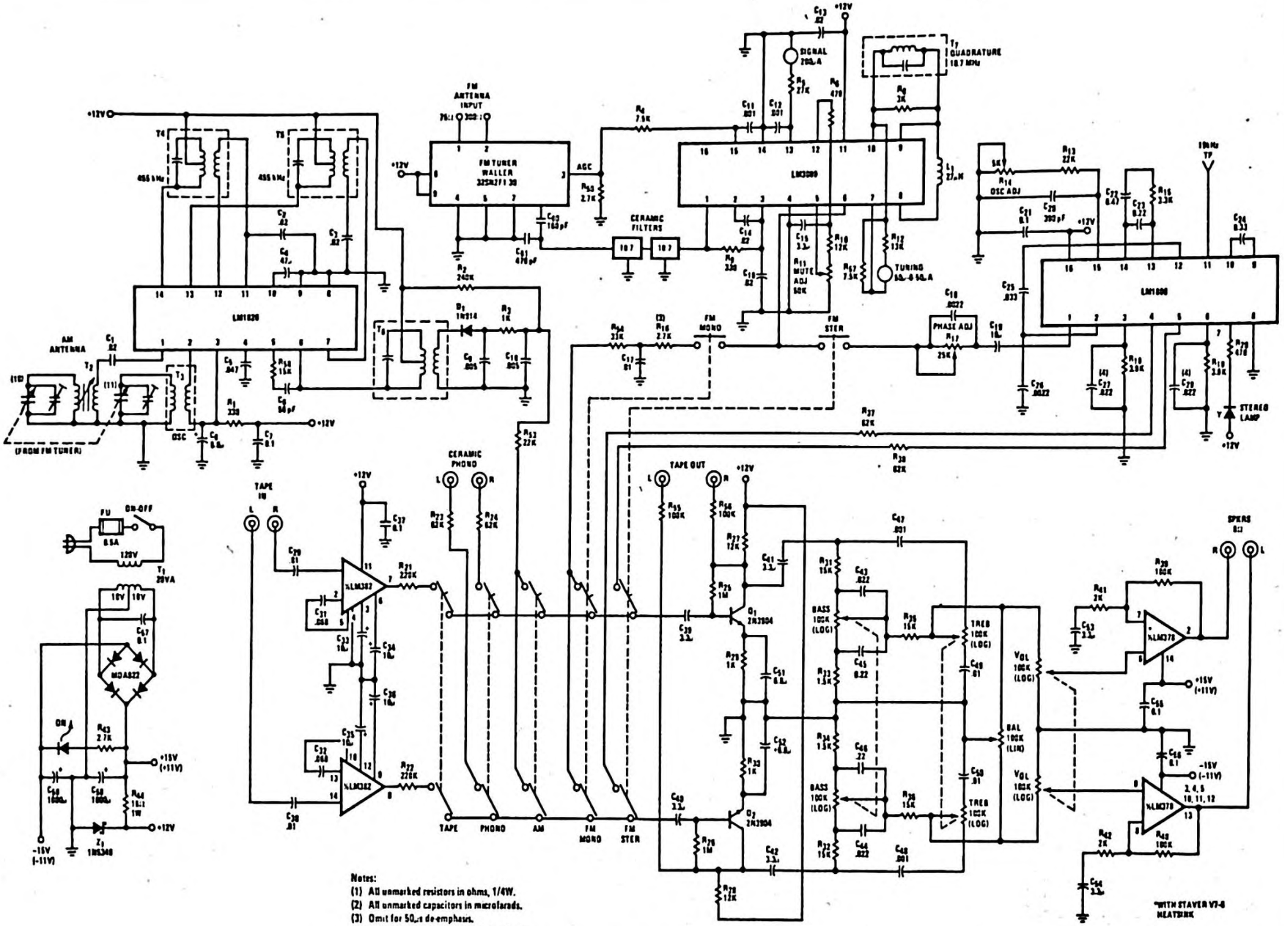
Power Output: 3W RMS, per channel into 8 ohms at less than 1% THD from 40-30 kHz
Frequency Response: 35-55 kHz ±3 dB

VENDOR DEVICES

FM Tuner: Waller 32SN2F1-30
Coils: T3: AM Osc. Toko RWO-6A6255
T4: IF, 455 kHz Toko RRC-3A6426N
T5: IF, 455 kHz Toko RRC-3A6427A
T6: IF, 455 kHz Toko RZC-1A6425A
T7: Quadrature, 10.7 MHz – Toko TKXC-33733BS
Ceramic Filters: 10.7 MHz Toko CFS-30AE-10
Selector Switch: IEE/Schadow Type F-4U with FA201 Mech. Reflecting Indicators
Meters: TUNING: #11226, SIGNAL: #11222 Mercer Electronics
Heatsink: Staver V7-5

VENDOR LOCATIONS

Waller Corp., Crystal Lake, Ill. (815) 459-6510
Toko (America), Inc., New York, N.Y. (212) 736-0245
IEE/Schadow Corp., Eden Prairie, Minn. (612) 944-1820
Mercer Electronics (Simpson Electric Co.), Elgin, Ill. (312) 379-1130
Staver Co., Bay Shore, N.Y. (516) 666-8000


+12V
T4
455 kHz
T5
455 kHz
C2 .02
C3 .02
C4 47µ
LM1820
AM ANTENNA
C1 .02
T2
(10)
(11)
T3
OSC
(FROM FM TUNER)
C5 .047
R58 15K
C8 56pF
R1 330
C6 6.8µ
C7 0.1
FM ANTENNA INPUT
75Ω
300Ω
FM TUNER WALLER 32SR2F1 30
AGC
C60 150pF
C61 470pF
R2 240K
D1 1N914
R3 1K
T6
C9 .005
C10 .005
R53 2.7K
CERAMIC FILTERS
10.7
10.7
R4 7.5K
C11 .001
C12 .001
C13 .02
SIGNAL 200µA
R5 27K
R6 470
LM3089
R9 3K
T7 QUADRATURE 10.7 MHz
L1 27µH
C14 .02
R8 330
C16 .02
C15 3.3µ
R10 12K
R11 MUTE ADJ 50K
R57 7.5K
R12 13K
TUNING 50µ-0-50µA
R54 33K
(3) R16 2.7K
C17 .01
FM MONO
FM STER
C18 .0022
PHASE ADJ
R17 25K
C19 1µ
5K
R14 OSC ADJ
R13 22K
C20 390pF
C21 0.1
C22 0.47
C23 0.22
R15 3.3K
19kHz TP
C24 0.33
C25 .033
LM1800
C26 .0022
(4) C27 .022
R18 3.9K
R19 3.9K
(4) C28 .022
R79 470
STEREO LAMP
R37 62K
R38 62K
FU
0.5A
ON-OFF
120V
T1 20VA
18V
18V
C57 0.1
MDA922
ON
R43 2.7K
+15V (+11V)
C58 1000µ
C59 1000µ
R44 18Ω 1W
Z1 1N5348
-15V (-11V)
TAPE IN
L
R
C29 .01
C30 .01
C37 0.1
½LM382
C31 .068
C32 .068
C33 10µ
C34 10µ
C35 10µ
C36 10µ
R21 220K
R22 220K
CERAMIC PHONO
R73 62K
R74 62K
R53 22K
TAPE
PHONO
AM
FM MONO
FM STER
TAPE OUT
R55 100K
R56 100K
R77 12K
R75 1M
C39 3.3µ
C40 3.3µ
Q1 2N3904
Q2 2N3904
R29 1K
R33 1K
C51 6.8µ
C52 6.8µ
R76 1M
R78 12K
C41 3.3µ
C42 3.3µ
C47 .001
C48 .001
R31 15K
R32 15K
C43 .022
C44 .022
BASS 100K (LOG)
C45 0.22
C46 .22
R33 1.5K
R34 1.5K
R35 15K
R36 15K
TREB 100K (LOG)
C49 .01
C50 .01
VOL 100K (LOG)
BAL 100K (LIN)
R41 2K
R42 2K
C53 3.3µ
C54 3.3µ
R39 100K
R40 100K
½LM378*
C55 0.1
C56 0.1
2, 4, 5 10, 11, 12
SPKRS 8Ω
*WITH STAVER V7-8 HEATSINK

Notes:

(1) All unmarked resistors in ohms, 1/4W.

(2) All unmarked capacitors in microfarads.

(3) Omit for 50µs de-emphasis.

(4) Change to 0.015µF for 50µs de-emphasis.

FIGURE 6. Complete Schematic

The Low Noise JFET—
The Noise Problem Solver

National Semiconductor
Application Note 151
John Maxwell
January 1976

The most versatile low noise active device available to the designer today is the Junction Field-Effect Transistor (JFET). JFETs are virtually free of the problems which have plagued bipolar transistors—limited bandwidth, popcorn noise, a complex design procedure to optimize noise performance. In addition, JFETs offer low distortion and very high dynamic range.

Most designers think of JFETs for very high source impedances. However, modern devices offer the designer performance improvements over bipolar transistors in NF for all but lowest impedance (<500Ω) sources and even then may provide improved performance if popcorn noise, bandwidth or circuit component noise is a consideration (see *Figure 1)*.

Therefore, the purpose of this article is to review low noise design procedures and indicate the simplicity of designing high performance low noise amplifiers with low cost JFETs.

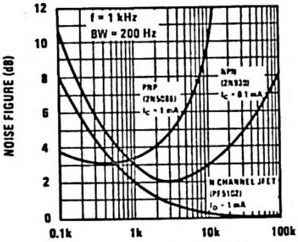


FIGURE 1. Bipolar and JFET Transistor Noise Comparison

REVIEW OF BASICS

Before guidelines are established for designing low noise JFET amplifiers, a method of noise characterization must be chosen. Designers are confronted with a multitude of different noise parameters such as Noise Figure (NF), noise voltage and current densities, noise temperature, noise resistance, etc. Designers are primarily concerned with signal to noise (S/N) ratios preferring noise voltage, (e_n) and current (i_n) density.

Noise generally manifests itself in three forms: thermal noise, shot noise and flicker or "1/f" noise. Thermal noise arises from thermal agitation of electrons in a conductor and is given by Nyquist's relation:

R
$\overline{V_R^2}$

$$\overline{V_R^2} = 4k\,TR\,\Delta f \qquad (1)$$

$\overline{V_R^2}$ = mean square noise voltage
k = Boltzmann constant (1.38 x 10^{-23} VAS/°K)
T = Absolute temperature (°K)
R = Resistance in ohms
Δf = Noise bandwidth (Hz)

The noise of a resistor may be represented as a spectral density (V^2/Hz) or more commonly in $\mu V/\sqrt{Hz}$ or $nV/\sqrt{Hz}$ and is given by:

$$e_{nR} = (\overline{V_R^2}/\Delta f)^{1/2} \qquad (2)$$

It is sometimes more convenient to represent thermal noise as noise current instead of a noise voltage. One needs only to consider the Norton equivalent yielding a noise current density.

$$i_{nR} = \frac{e_{nR}}{R} = \left(\frac{4\,kT}{R}\right)^{1/2} \qquad (3)$$

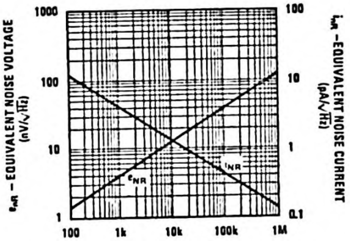


FIGURE 2. Thermal Noise Voltage and Current Densities vs Resistance.

The second basic form of noise, shot noise, is due to the randomness of current flow (discrete charge particles) in semiconductor P-N junctions.

$$\overline{i^2} = 2\,q\,I_{DC}\,\Delta f \qquad (4)$$

$\overline{i^2}$ = Mean square noise current
q = Charge of an electron (1.6 x 10^{-19} AS)
I_{DC} = dc current flowing through the junction (A)
Δf = Noise bandwidth (Hz)

As with thermal noise, shot noise may be represented as a current density (A^2/Hz) or $pA/\sqrt{Hz}$.

$$i_n = (\overline{i^2}/\Delta f)^{1/2} \qquad (5)$$

It should be noted that both thermal noise and shot noise are "white" noise sources, i.e., frequency independent.

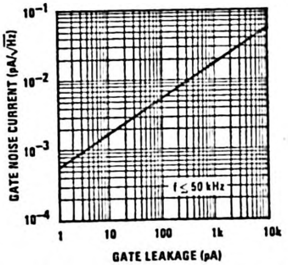


FIGURE 3. Current Noise vs Gate Leakage Current

AN-151 The Low Noise JFET — The Noise Problem Solver

The third basic noise source confronting designers is flicker or "1/f" noise whose density is roughly inversely proportional to frequency starting at about 1 kHz in both JFETs and bipolar transistors and increasing as frequency is decreased. Through careful processing, flicker noise in JFETs has been reduced to levels nearly insignificant to the designer. Flicker noise in JFETs is primarily a noise voltage and is source independent. Flicker noise in bipolar transistors is a function of base and leakage currents increasing with increased source impedance or operating currents.

A simple noise model of a JFET or any amplifying device may be constructed using a thermal and shot noise source which would adequately describe its noise performance allowing signal to noise ratios to be calculated directly.

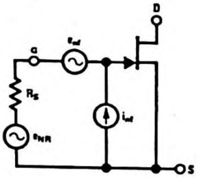


FIGURE 4. Simple JFET Noise Model

The input noise per unit bandwidth at some frequency may be calculated from the mean square sum of the noise sources (assuming the JFET noise sources are uncorrelated or independent of one another).

$$e_{nt}^2 = e_{nR}^2 + e_{nf}^2 + i_{nf}^2 \ R_s^2 \qquad (6)$$

The total noise in the same bandwidth Δf, where the noise sources are independent of frequency, is simply:

$$V_{NOISE} = (e_{nt}^2 \ \Delta f)^{1/2} \qquad (7)$$

Practically, noise sources are not frequency independent except resistor noise with no dc bias. The total input noise for the nonideal case may be calculated by breaking the spectrum up into several small bands and calculating the noise in each band where the noise sources are nearly frequency independent. The total input noise would then be the RMS sum of the noise in each of the bands N1 . . . Nn.

$$V_{NOISE} = (V_{N1}^2 + V_{N2}^2 + \ldots V_{Nn}^2)^{1/2} \qquad (8)$$

THE DESIGN PROCESS

The final circuit configuration and suitable JFET will be determined by the external circuit constraints.

1) Minimum signal to noise ratio (maximum amplifier noise)
2) Type and magnitude of source impedance (resistive or reactive)
3) Amplifier input impedance requirements
4) Bandwidth and maximum frequency of interest
5) Maximum operating temperature
6) Stage gain
7) Power supply voltage and current limitations
8) Circuit configuration, single or dual device

The design procedure is dependent on the type of source and each case must be considered separately. Resistive sources will be considered first because they are the least restrictive for the preamplifier.

Resistive Sources

Preamplifiers for resistive sources are typically voltage amplifiers requiring a fixed input resistance and capacitance consistent with the maximum frequency of interest and source resistance. In most cases a resistor of the desired value connected between the gate and ground will satisfy the input resistance requirement leaving the maximum input capacitance as the major concern.

The maximum amplifier input capacitance is a function of the JFET source resistor, input resistance, source capacitance and maximum frequency. The maximum allowable input capacitance will be used in eliminating unsuitable JFET geometrics and optimizing the circuit configuration. Sometimes the JFET geometry (or type) with the lowest noise may also have an input capacitance that makes it unsuitable. The JFET input capacitance should be considered before noise in high source resistance, wideband amplifier designs.

$$C_{in} \cong C_{rs}\left(1 + \frac{gm\ R_D}{1 + gm\ R_s}\right) + \frac{C_{gs}^{*}}{1 + gm\ R_s} \qquad (9)$$

$^{*}C_{gs} = C_{is} - C_{rs}$.

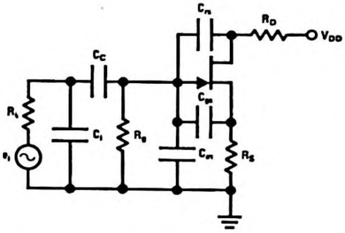


FIGURE 5. A Typical Resistive Source JFET Amplifier

If low input capacitance is required, a cascode configuration minimizes input capacitance and still allows high gain within a device type. The cascode configuration can also be used to reduce the voltage across a device, reducing device heating (for high current operation) and gate leakage currents when source impedances are very high.

Once the basic circuit configuration has been decided upon or dictated by gain, bandwidth and power supply limitations, the final JFET selection will be on noise. Redrawing the amplifier in *Figure 4* with all of the noise sources, the total amplifier noise per unit bandwidth can be found.

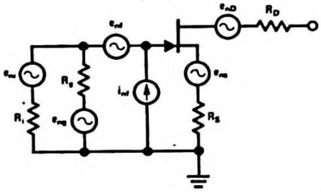


FIGURE 6. A Typical Resistive Source JFET Amplifier with Noise Sources

$$e_{nt} = \left[e^2_{nig} + e^2_{nf} + e^2_{ns} + \frac{e^2_{nD}}{A_V{}^2} + i^2_n \; (R_i // R_g)^2 \right]^{1/2} \qquad (10).$$

where: e^2_{nig} = The noise of the parallel connection of R_i and R_g

e^2_{nf} = The noise voltage of the JFET

e^2_{ns} = The noise of the source resistor R_s

$\frac{e^2_{nD}}{A_V{}^2}$ = The noise at the drain (thermal noise of the load plus the second stage noise)

$i^2_n (R_i//R_g)^2$ = The current noise contribution of the JFET

When the amplifier is operated at room temperature and moderate drain voltages, the current noise term is usually negligible with source resistances as high as 10 MΩ. Depending on the voltage gain of the stage, the drain circuit noise may be negligible, simplifying the input noise expression.

$$e_{nt} = (e^2_{nig} + e^2_{nf} + e^2_{ns})^{1/2} \qquad (11)$$

The final JFET selection will be based on the noise requirements from the maximum allowable noise V_{MAX}.

$$V_{MAX} = (e^2_{nf} + e^2_{ns})^{1/2} \qquad (12)$$

Depending on V_{MAX} and e^2_{nf} the source resistor may have to be bypassed to ground to eliminate noise of the bias resistor.

Capacitive Sources

Preamplifiers for capacitive sources are primarily current amplifiers requiring very high input resistance and controlled input capacitance to match the source capacitance.

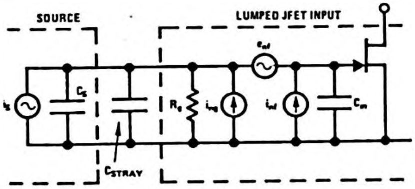


FIGURE 7. JFET Preamplifier with a Capacitive Source

The source capacitance should equal the sum of the preamplifier input capacitance and the stray capacitance for maximum frequency response and power transfer from the signal source. Assuming the gate resistor, R_g, is so large as to not load the capacitive source, the input noise voltage is:

$$e_{nt} \cong \left[e^2_{nf} + (i^2_{nf} + i^2{}_{ng}) \left(\frac{R_g{}^2}{(1 + \omega^2 R_g{}^2 C^2)} \right) \right]^{1/2} \qquad (13)$$

where $C = C_S + C_{in}$

with an input signal of

$$e_s \cong i_s \left(\frac{R_g{}^2}{1 + \omega^2 R_g{}^2 C^2} \right)^{1/2} \qquad (14)$$

When the source and input capacitance are matched, the final JFET geometry will be selected on two criteria: the noise voltage, e_n, and the current noise from the gate leakage, $I_{G(ON)}$, to optimize the signal to noise ratio. As in the resistive source case, the circuit configuration and JFET selection is an iterative process using all of the external circuit constraints and device parameters and limitations.

Inductive Sources

Amplifiers designed for inductive sources (including transformers) require fixed input resistance (as in the resistive source case) and controlled input capacitance (as in the capacitive source case). The input noise per unit bandwidth will rise with increasing frequency to a maximum value at resonance of the inductive source and the input capacitance or when the shunt resistance of the inductor is larger than the input resistance of the amplifier.

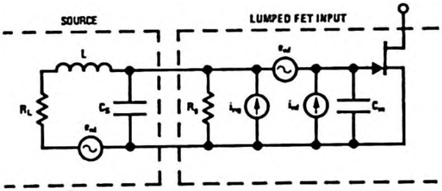


FIGURE 8. JFET Amplifier with an Inductive Source

The inductive source amplifier is the most difficult to analyze due to the complex input impedance. The input noise per unit bandwidth is given by:

$$e^2_{nt} = e^2_{nf} + (i^2_{nf}) (|Z_{in}|^2) + 4\,kT\,(\mathrm{Re}\,(Z_{in})) \qquad (15)$$

where $Z = X_{CIN} // R_g$

and $Z_{in} = Z // (Z_L + R_L)$

Usually the current noise of the JFET is negligible, simplifying the expression a little, but not much. The optimization process for inductive sources is very complex and it will require the spectrum to be broken up into several small bands to arrive at a final design. Generally, a JFET with a minimum noise voltage will be the proper choice.

Transformers may be used with JFET amplifiers to minimize noise with very low source impedances. Transformers have both drawbacks and advantages and both must be examined before a transformer design is chosen. Poor frequency response, susceptibility to mechanical and magnetic pickup and thermal noise head the list of disadvantages to be weighed against two very important advantages. First, the noise voltage is transformed by the turns ratio N; second, the resistance is transformed by N^2. These can be used to advantage by matching very low values of source resistance to a relatively noisy amplifier and still maintaining a good signal to noise ratio, i.e., the total noise at the source assuming an ideal transformer is

$$e_{nt}^2 = e_{nRs}^2 + \frac{e_{nAmp}^2}{N^2} \qquad (16)$$

SUMMARY

Low noise amplifier design concepts have been introduced for the three basic types of sources. Basic parameters (C_{In}, e_n, gm) were discussed that affect both circuit configuration and JFET type. There is no universal low noise JFET or circuit configuration that solves all problems. Each low noise amplifier design is different and must be considered within its own framework of performance requirements.

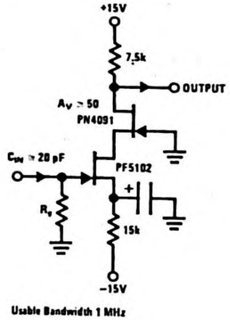
REFERENCES

A. Van der Ziel, "Noise," Prentice-Hall, 1954.

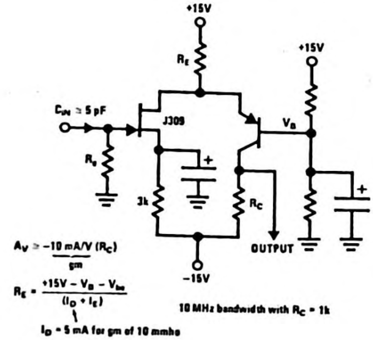
Richard S.C. Cobbold, "Theory and Applications of Field-Effect Transistors," John Wiley & Sons, 1970.

C.D. Motchenbacher and F.C. Fitchen, "Low Noise Electronic Design," John Wiley & Sons, 1973.

SOME PRACTICAL LOW NOISE JFET INPUT CIRCUITS


+15V
7.5k
OUTPUT
$A_V \simeq 50$
PN4091
$C_{IN} \simeq 20$ pF
PF5102
+
R_s
15k
−15V
Usable Bandwidth 1 MHz

a) Wide Band, Low Input Capacitance, Very Low Noise Preamplifier


+15V
R_E
+15V
$C_{IN} \simeq 5$ pF
J309
V_B
+
R_s
3k
R_C
+
OUTPUT
−15V
$A_V \simeq \underbrace{-10\text{ mA/V}}_{gm}(R_C)$
$R_E = \frac{+15V - V_B - V_{be}}{(I_D + I_E)}$
$I_D = 5$ mA for gm of 10 mmho
10 MHz bandwidth with $R_C = 1k$

b) Low Noise, Very Low Input Capacitance Video Amplifier

APPENDIX A

Important National JFET Process Parameter Guide

Test Conditions $V_{DS} = 15V$, $I_D = 1\ mA$ ($V_{GS} = 0V$)*

PROCESS	e_n @ 10 Hz ($nV/\sqrt{Hz}$)	e_n @ 1 kHz ($nV/\sqrt{Hz}$)	e_n @ 100 kHz ($nV/\sqrt{Hz}$)	g_{fs} (mmho)	$I_{G(ON)}$ (pA)	C_{GD} (pF)	C_{GS} (pF)
50	15	5	2.5	3	5V 2 pA 10V 10 pA 15V 1 nA	0.7	2.5
51	5	3	1.3	7	30	3	9
55	10	4	2.5	2.4	5	2	4
92	10	4	1.5	4.5	10V 20 pA 15V 1 nA	2	4
83	10	5	2.5	2	5	1	2.5
84*	50	15	9	0.2	0.1	0.01	2
94	10	5	2.5	2	1–2	0.01	4
95	10	4	2.5	1.5	15	3.5	15
96	5	3	1.3	7	30	3	9
93	15	7	2	3.5	10V 20 pA 15V 1 nA	1	3.2

National JFET Process Low Noise Amplifier Guide

PROCESS	50	51	55	92	83	84	93	94	95	96
Low Noise Application	Single JFET				Dual JFET					
Resistive Ultra-Low $e_n < 5\ nV/\sqrt{Hz}$ @ 10 Hz		X								X
Resistive Low Freq < 20 kHz		X	X		X			X	X	X
Resistive Wideband < 10 MHz	X	X		X	X		X	X	X	X
Resistive Wide Band > 10 MHz	X			X			X			
Resistive Very High $R_S > 10\ M\Omega$	X					X		X		
Capacitive Low C < 10 pF	X		X	X	X	X	X	X		
Capacitive High C > 20 pF		X	X						X	X
Inductive	X	X	X	X	X	X	X	X	X	X

APPENDIX B

NOISE PARAMETER CONVERSION

Noise Figure (NF) to an Effective e_n

It is more convenient to present noise data for bipolar transistors in the form of contours of constant noise figure at a fixed frequency or plots of noise figure versus frequency at a fixed source resistance due to large values of noise current (i_n). Noise figure must be converted to an effective noise voltage (e_{nE}) for comparisions to be made between a BJT and a JFET or for signal to raise ratio calculations.

By definition:

$$NF = 10 \log \frac{\text{Total Output Noise Power}}{\text{Output Noise Power of the Source}} \quad \text{(B1)}$$

From equations 1 and 2, one finds the source noise power to be

$$\text{Source Noise Power} = \frac{e_{nR}^2 \, \Delta f}{R_S} \quad \text{(B2)}$$

for some source resistance R_S.

Referring to *Figure 4*, the total output noise power at the input of the amplifier would be:

$$\text{Total Output Noise Power} = \frac{e_{nR}^2 \, \Delta f}{R_S} + \frac{e_{nf}^2 \, \Delta f}{R_S} + i_{nf}^2 \, R_S^2 \, \Delta f \quad \text{(B3)}$$

The noise figure (NF) can now be expressed in terms of the noise source generators, e_{nR}, e_{nf} and i_{nf} allowing. an expression to convert noise figure (NF) to an effective noise voltage (e_{nE}).

$$NF = 10 \log \left(1 + \frac{e_{nf}^2 + i_{nf}^2 \, R_S^2}{e_{nR}^2}\right) \quad \text{(B4)}$$

yielding

$$e_{nf}^2 + i_{nf}^2 \, R_S^2 = e_{nE}^2 = (10^{NF/10} - 1) \; e_{nR}^2 \quad \text{(B5)}$$

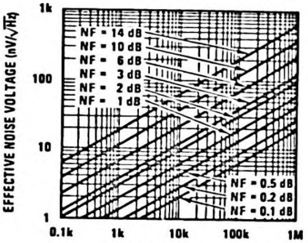


FIGURE B1. Effective Noise Voltage (e_{nE}) vs Noise Figure and Source Resistance (R_S)

Noise Resistance

The effective noise voltage density (e_n) and noise current density (i_n) are found directly by referring to *Figure 1*, and reading the values for the corresponding resistances.

$$e_{nR} = (4\,KTR)^{1/2} \quad \text{(1)}$$

$$i_{nR} = \left(\frac{4\,KT}{R}\right)^{1/2} \quad \text{(3)}$$

APPENDIX C

JFET Current Noise

At low frequencies the current noise and voltage noise sources are uncorrelated in JFETs with the current noise being pure shot noise due to gate leakage currents. As frequency is increased, the current noise also increases starting at frequencies as low as 50 kHz in some high capacitance device types.

It has been suggested and experimentally verified that the noise current at high frequencies is due to increased gate input conductance.

$$i_n^2 = 4\,KT\left[\text{Re}\,(Y_{11})\right]^{-1} \quad \text{(C1)}$$

Re (Y$_{11}$) is available on high frequency JFET data sheet as the real portion of the common source input admittance parameters. In effect the channel noise is coupling to the gate circuit through the source-gate and drain gate capacitances. Hence low capacitance devices exhibit lower values of noise current at high frequencies than do high capacitance devices.

Constant Current LED

National Semiconductor
Application Note 153
Peter Lefferts
October 1975

INTRODUCTION

The NSL4944 is a simple two-lead device normally used as an AC or DC indicator, yet can also be used as a rectifier and constant current source at the same time in associated circuitry. A number of such applications will be illustrated. Further, most of the regulating circuitry is not in series with the LED. This allows the complete regulated LED to operate at only about 300 mV more than a standard red LED. Thus the NSL4944 operates on half the voltage needed by previously available regulated or resistor LEDs. The device is rated for a maximum of 18 V forward and reverse.

These characteristics provide several advantages. Unloaded TTL gates provide enough voltage, in either high or low states, to directly drive the universal indicator. Size and weight can be saved in instruments with a number of indicator lights by reducing the size of filter capacitors or voltage regulators. The NSL4944 can operate on unfiltered DC or at somewhat reduced intensity on 3 to 12 VAC rms. Since the IC within the regulated LED blocks reverse voltage, the device can be used as a low voltage rectifier or polarity indicator.

DESIGN FEATURES

The LED and its current source, as illustrated in Figure 1, both fit within a standard LED package. The typical operating voltages shown allow the device to operate with lower supplies and take up less room than an LED and component dropping resistor.

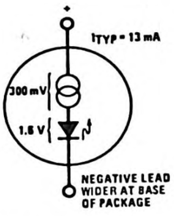


FIGURE 1. Equivalent Circuit

Figure 2 shows how some of the operating features of the NSL4944 are achieved. The rectifying characteristic occurs because the only input to the device passes through the IC's PNP emitters. These have a high reverse voltage in standard linear processing. The voltage reference and comparison amplifier operate from the same low voltage that the LED does. The big PNP transistor which passes both I_{LED} and I_{REF} can be operated almost in saturation since the comparison amplifier can pull the PNP base down to only one volt from common.

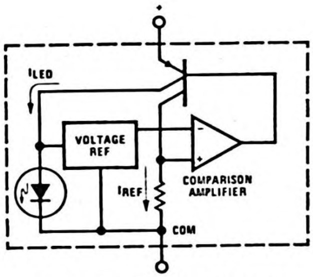


FIGURE 2. Simplified Schematic

INDICATOR POWERING

The following figures contain some of the innumerable ways of providing power to the NSL4944.

Power and parts count is minimized by powering the indicator from a low voltage transformer winding as shown in Figure 3. This method, however, provides only half intensity light, but the apparent visual decrease is not as great. Some flicker occurs if the observer moves his head rapidly. The supply of Figure 4 will provide up to 87% of maximum light output. The bulk of a filter capacitor is still not needed, and at 12 VAC in, flicker will be almost imperceptible since the LED "off" periods will be less than a millisecond. In both situations, the indicator may be switched a number of ways, including bipolar transistors, since only DC can pass through the indicator.

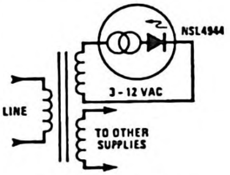


FIGURE 3. AC Power

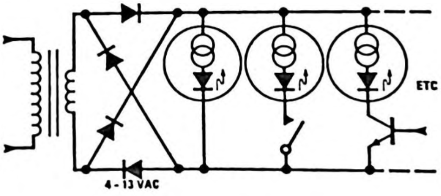


FIGURE 4. Unfiltered DC Power

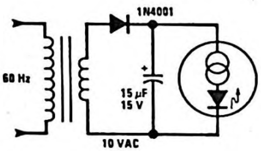


FIGURE 5. Minimizing DC Filtering

As shown in Figure 5, full intensity and zero possible flicker are achieved by minimal DC filtering. The small capacitor shown operates with 10 V p-p ripple and only about 8 V average DC, while the constant current drain characteristics of the NSL4944 allow only a few percent change in light intensity. If a system or instrument with a regulated supply has a number of LED indicators, regulator size and dissipation can be minimized by powering the regulated LEDs from the unregulated voltage.

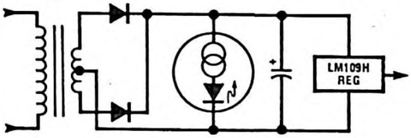
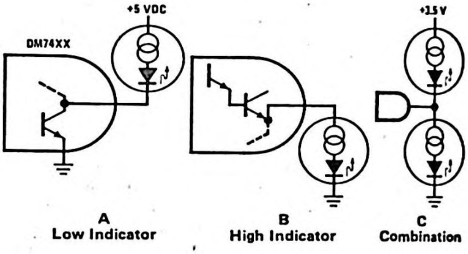


FIGURE 6. Unregulated DC

LOGIC APPLICATIONS

The low operating voltage and constant current characteristics make the regulated LED an ideal status indicator for digital circuitry. An interesting fact to keep in mind is that full regulator current is not needed to light the LED. If, for example, only 8 mA is available (from a voltage of 1.6 to 1.9 V) the LED will light at a somewhat reduced intensity. The regulator will be switched full on instead of current limiting . . . but in such a situation it doesn't matter.

Any circuit capable of supplying 10 to 20 mA and a voltage swing of at least 1 V can switch the NSL4944 from an off to an on state. Within 25°C of room temperature, an input voltage of 1.3 V will produce little or no light, and 2.3 V will produce 70% to 90% of full output. However, with a small signal change, the preexisting biases must be correct. The output swing of a TTL stage goes much closer to ground than to the 5 V supply. Therefore, Figure 7-C requires a 3.5 V supply for the indicators to have complete on-off switching.



A
Low Indicator

B
High Indicator

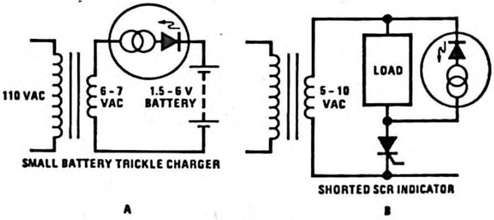
C
Combination

FIGURE 7. TTL Indicators

CIRCUIT APPLICATIONS

In many circuits or small instruments the need for a constant current source or current limiter arises. FETs can generally only be used as low current sources, so for 10 mA or more, construction of a current source requires 3, 4, or more parts. If an indicator or pilot light is also needed, the regulated LED may be a very economical source of the needed constant current.

The examples below illustrate all three characteristics of the NSL4944. It is a combined rectifier, constant current source, and pilot light.



SMALL BATTERY TRICKLE CHARGER
A

SHORTED SCR INDICATOR
B

FIGURE 8.

Constant currents have a number of circuit or equipment design uses. Some of these have been combined for illustration in Figure 9. A number of LEDs can "share" a single constant current LED. Further, any of the ordinary LEDs can be turned on and off by a shunting switch without affecting operation of any of the others.

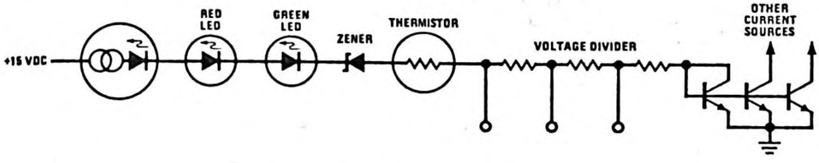


FIGURE 9. Uses for Constant Current

In equipment with unregulated supplies, or supplies having some unfiltered ripple, the 20,000 Ω impedance of the NSL4944 current source will be helpful. Supply ripple and variation passed on to Zener diodes, thermistors, and low value voltage divider bias sources will be greatly reduced. The sensitivity of low value thermistors to temperature changes will be increased. If practical, the regulated LED should be put in the same, or similar temperature environment as the thermistor used for temperature measurement. Otherwise a 20 to 40 degree temperature change at the LED would lead to an apparent one degree change sensed at the thermistor. Multiple current sources find use in some audio amplifier designs, and in power op-amp modules.

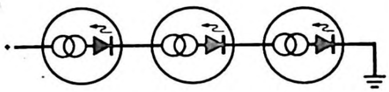


FIGURE 10. Series NSL4944s

There are some characteristics of seriesed regulated LEDs, and current sources in general, that should be kept in mind. All the LEDs will light properly, and the string will run at the current of the least current source. This lowest value source will absorb most of the supply voltage, with the other LEDs having only the starting voltage of about 2 V across them. Thus the maximum forward voltage increases only slightly as more devices are added. In the example above it would be 22 V. However, due to non-linear reverse current characteristics, maximum reverse voltages can be added.

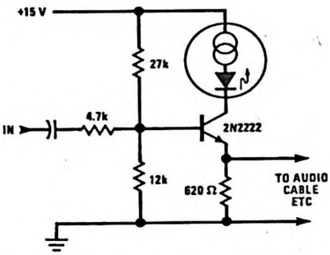


FIGURE 11. Current Limiting and Short Protection

A current source can also be a current limiter. Figure 11 shows an NSL4944 put in the collector of an emitter follower such as might be used in a pre-amp or mike mixer cable driver.

Normally voltage across the LED is only 2 V, allowing almost full supply-to-supply swing of the emitter follower output. In comparison a limiting resistor would either greatly increase output impedance, or severely limit output swing. However, if the output cable is accidentally shorted, only a little more than the rated current of the LED will flow. Output transistor dissipation actually decreases under emitter short conditions.

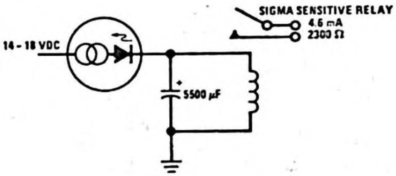


FIGURE 12. Six Second Time Delay

Logically, a constant current source is helpful in designing time delay circuits. If the circuit of Figure 12 were built with a resistor, the timing period would only be half the amount shown, and timing would vary over 50% with the supply variations shown.

Instead, the current regulated LED is still drawing within 10% of full current when the relay reaches its 11 V pull-in voltage. The 14 to 18 V supply variation will produce only about a 3% timing variation, a considerable improvement. Variations due to temperature and electrolytic capacitor tolerances will remain, however.

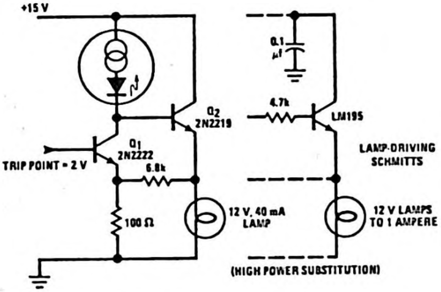


FIGURE 13. Use as Active Load

The lamp-driver Schmitt of Figure 13 illustrates a still further use of the NSL4944's constant current source. Substituting a current source for the collector resistor increases the useful voltage gain of Q_1. Further, almost full base current remains available to Q_2, even when supplying 12 V output, which would not be possible using a resistor. When the lamp and Q_2 are off, most of the LED current flows in the 100 Ω resistor, thus determining the circuit's switching or trip point of 2 V.

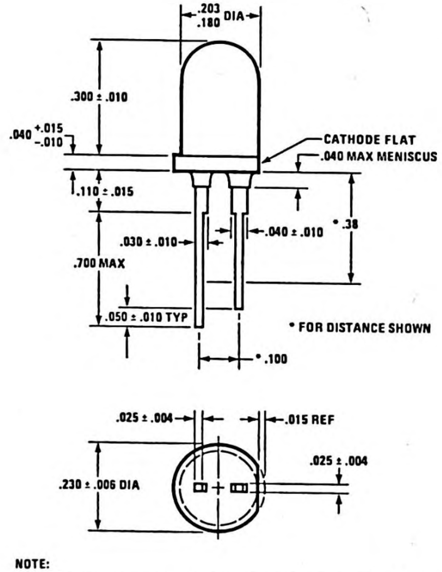
With Q_1 saturated, Q_2 still provides a volt to the bulb, contributing some preheating and reducing the bulb's starting current surge. On, Q_2 provides the bulb with 12 V due to the minimum voltage drop in the constant current LED. The 6.8k feedback resistor sets hysteresis at a measured 50 mV at the input. This can be varied without having to change the rest of the circuit. 10k provides almost "0" hysteresis (undesirable and unstable) while 2k sets a hysteresis of 0.5 V.

CONCLUSION

A number of applications have been examined for a highly improved two-lead LED/IC. Its indicating capabilities, high reverse voltage, and wide constant current range may make it the most useful of the two-lead, hence simple to use, IC devices. To begin with, it can be lit from AC, unfiltered DC, and very poorly filtered or regulated DC with a savings in parts or size.

The NSL4944 may be driven from the 1 to 1.5 V swing of TTL circuitry, to the 15 to 18 V swing of Linear and MOS circuits. Its rectifying capabilities allow it to act as a small battery charger or reverse voltage monitor for power supplies, batteries, or low voltage SCRs. For all these, and the following functions, the LED "on" indication is in addition to the constant current circuit function performed. The device's constant current can power other LEDs, Zeners, thermistors, or other current or voltage sources. It has been shown that the current regulated LED can be a current limiter, a timing element, or an active load while simplifying and improving circuit performance.

PHYSICAL DIMENSIONS


.203
.180 DIA
.300 ± .010
.040 +.015 −.010
CATHODE FLAT
.040 MAX MENISCUS
.110 ± .015
.030 ± .010
.040 ± .010
* .38
.700 MAX
.050 ± .010 TYP
* FOR DISTANCE SHOWN
* .100
.025 ± .004
.015 REF
.025 ± .004
.230 ± .006 DIA

NOTE:

1. ±.015 TOLERANCE ON ALL DIMENSIONS UNLESS OTHERWISE SPECIFIED.

1.3V IC Flasher, Oscillator, Trigger or Alarm

National Semiconductor
Application Note 154
Peter Lefferts
December 1975

INTRODUCTION

Most linear integrated circuits are designed to operate with power supplies of 4.5 to 40 V. Practically no battery/portable equipment is provided with indicator lights due to unacceptable power drain. Even LEDs (solid state lamps) won't light from a 1.5 V battery, and drain the common 9 V radio battery in a few hours.

The LM3909 changes all this. Obtaining long life from a single 1.5 V cell, it opens a whole new area of applications for linear integrated circuits. Sufficient voltage for flashing a light emitting diode is generated with cell voltage down to 1.1 V. In such low duty cycle applications batteries will last for months to years of continuous operation. Such flasher circuits then become practical for marking location of flashlights, emergency equipment, and boat mooring floats in the dark.

The LM3909 is simple in design, easy to use, and includes extra resistors to minimize external circuitry and the size of the completed flasher or oscillator.

CIRCUIT OPERATION

The circuit below in figure A is the LM3909 connected as the simplest type of oscillator. Ignoring the capacitor for a moment, and assuming 1.5 V on pin 5, current will flow in the 3k and 6k timing resistors through the emitter of Q_1. This current will be amplified by about 3 by Q_2 and passed to the base of Q_3. Q_3 will then conduct, pulling down on the base of Q_4 and hence the base of Q_1. This is a negative feedback since it will reduce timing resistor current and current to the power transistor's base until a balance is reached. This will occur with the collector of Q_3 at about 0.5 V, the base of Q_4 at about 1 V, and a very small voltage from pin 8 to ground. The difference between these two voltages is the base-emitter drop of Q_1 and 2/3 the base-emitter drop of Q_4 as set by the high resistance divider from its base to emitter.

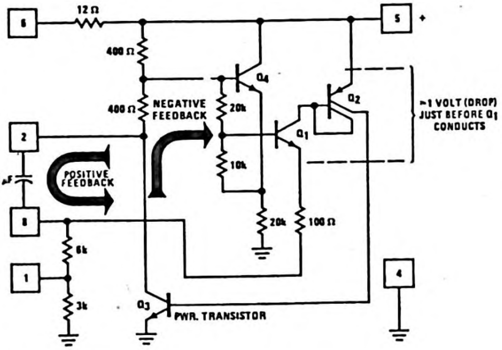


FIGURE A.

Note that negative feedback *voltage* is attenuated by at least 2 due to the divider of two 400 Ω resistors. Now considering the capacitor, its positive feedback is initially unity. Therefore the DC bias condition and the temporary excess positive feedback conditions are met and the circuit must oscillate.

The waveform at pin 8 of the above oscillator is shown below. The waveform at pin 2, the power transistor collector, is almost a rectangle. It extends from a saturation voltage of 0.1 V or less to within about 0.1 V of the supply voltage. The "on" period of course coincides with the negative pulses at pin 8. Other circuit voltages can easily be inferred from these two waveforms.

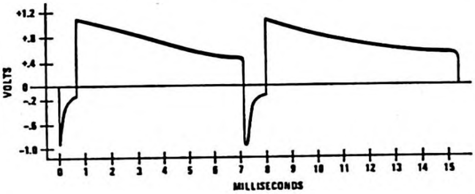


FIGURE B.

The simplicity of LED and incandescent pilot lamp flashers is illustrated below. In the LED flasher, the LM3909 uses the single capacitor for both timing and voltage boosting.

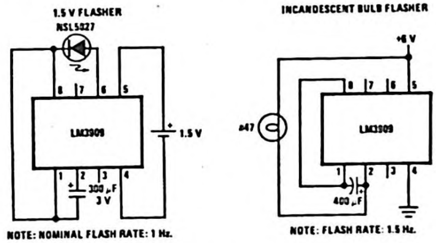

1.5 V FLASHER
NSL5027
8
7
6
5
LM3909
1.5 V
1
2
3
4
300 µF
3 V
NOTE: NOMINAL FLASH RATE: 1 Hz.
INCANDESCENT BULB FLASHER
+6 V
8
7
6
5
#47
LM3909
1
2
3
4
400 µF
NOTE: FLASH RATE: 1.5 Hz.

FIGURE 1. Two Simple Flashers

The LM3909, although designed as a LED flasher, is ideal for other applications such as high current, trigger pulse for SCRs and "Triacs." The frequency of oscillation adjusts from under 1 Hz to hundreds of kHz. Waveshape can be set from pulses a few µs wide to approximately a square wave. Thus the LM3909 can perform as a sound effects generator, an audible alarm, or audible continuity checker. Finally it can be a radio (detector/amplifier), low power one-way intercom, two-way telegraph set, or part of a "mini-strobe" light flashing up to 7 times per second.

Operating with only a 1.5 V battery as a supply gives the LM3909 several rather unique characteristics. First, *no* known connection can cause immediate destruction of the IC. Its internal feedback loop insures self-starting of properly loaded oscillator circuits. Experimenters can safely explore the possibilities of the LM3909 as an AC amplifier, one-shot, latch circuit, resistance limit detector, multi-tone oscillator, heat detector, or high frequency oscillator.

With the accent on the practical, a brief circuit description will be given followed by circuits in the following application areas:

Flasher & Indicator Applications
Audio & Oscillator Applications
Trigger & Other Applications

For those who want to modify or design their own circuits using the LM3909, application hints will be covered near the end of this note.

CIRCUIT DESCRIPTION

The circuit of figure 2 again shows the typical 1.5 V LED flasher, but with the internal circuitry of the IC illustrated.

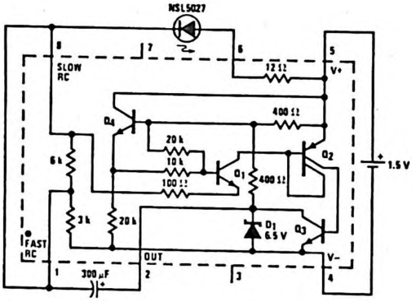


FIGURE 2. Circuit Operation

The flasher achieves minimum power usage in two ways. Operated as above, the LED receives current only about 1% of the time. The rest of the time, all transistors but Q_4 are off. The 20k resistor from Q_4's emitter to supply-common draws only about 50 µA. The 300 µF capacitor is charged through the two 400 Ω resistors connected to pin 5 and through the 3k resistor connected to pin 4 of the circuit.

Transistors Q_1 through Q_3 remain off until the capacitor becomes charged to about 1 V. This voltage is determined by the junction drop of Q_4, its base-emitter voltage divider, and the junction drop of Q_1. When voltage at pin 1 becomes a volt more negative than that at pin 5 (the supply positive terminal) Q_1 begins to conduct. This then turns on Q_2 and Q_3.

The LM3909 then supplies a pulse of high current to the LED. Current amplification of Q_2 and Q_3 is between 200 and 1000. Q_3 can handle over 100 mA and rapidly pulls pin 2 close to supply common (pin 4). Since the capacitor is charged, its other terminal at pin 1 goes *below* the supply common. The voltage at the LED is then higher than battery voltage, and the 12 Ω resistor between pins 5 and 6 limits the LED current.

Many of the other oscillator circuits work in a similar fashion. If voltage boost is not needed (with or without current limiting) loads can be hooked between pins 2 and 6 or pins 2 and 5.

APPLICATIONS: Flasher & Indicator

Differing uses and supply voltages will require adjustment of flashing rates. Often it is convenient to leave the capacitor the same value to minimize its size, or to fix the pulse energy to the LED. First, the internal RC resistors can be used to obtain 3k, 6k, or 9k by hooking to or shorting the appropriate pins. Further adjustment methods are shown in the two parts of figure 3 below.

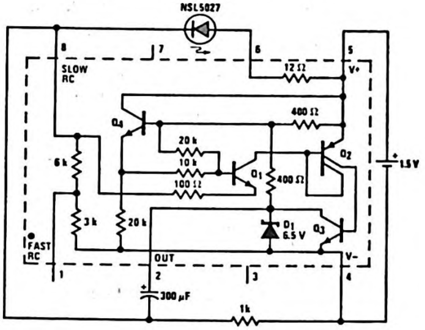


FIGURE 3a. Fast Blinker

In figure 3a, it can be seen that the internal RC resistors are shunted by an external 1k between pins 8 and 4. This will give a little over 3 times the flashing rate of the typical 1.5 V flasher of figure 1.

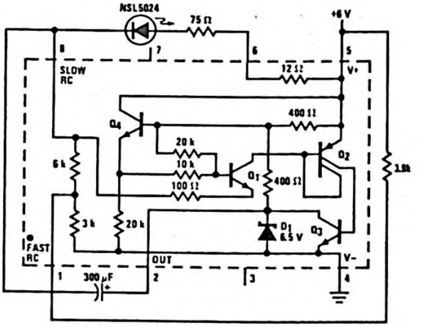


FIGURE 3b. 6 Volt Flasher

The 3.9k resistor in figure 3b connected from pin 1 to the 6 V supply raises voltage at the bottom of the 6k RC resistor. Charging current through that resistor is greatly reduced, bringing flashing rate down to about that of the 1.5 V circuit (1 Hz). As will be explained later, this biasing method also insures starting of oscillation even under unfavorable conditions.

Two precautions are taken for circuit reliability. The added 75 Ω series resistor for the LED keeps current peaks within safe limits for the diode and IC. Also, in operation above a 3 V supply, the electrolytic capacitor sees momentary voltage reversals. It should be rated for periodic reversals of 1.5 V.

A continuously appearing indicator light can also be powered from a single 1.5 V cell. Duty cycle and frequency of the current pulses to the LED are increased until the average energy supplied provides sufficient light. At frequencies above 2 kHz, even the fastest movement of the light source or the observer's head will not produce significant flicker.

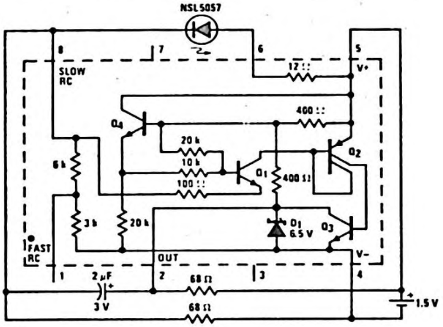


FIGURE 4. "Continuous" 1.5 V Indicator

Since this indicator powering circuit uses the smallest capacitor that will reliably provide full output voltage, its operating frequency is well above the 2 kHz point. The indicator is not, however, intended as a long life system, since battery drain is about 12 mA.

High frequency operation requires addition of *two* external resistors, typically of the same value. One, of course, shunts the high internal timing resistors. If only this one were used, the capacitor charging current would have to pass through the two 400 Ω resistors internally connected between pin 5 and the collector of Q_3. Oscillation at a slower rate and lower duty cycle than desired would occur, and oscillation might cease altogether before the battery was fully discharged. The second 68 Ω resistor shunting the two 400 Ω resistors eliminates these problems.

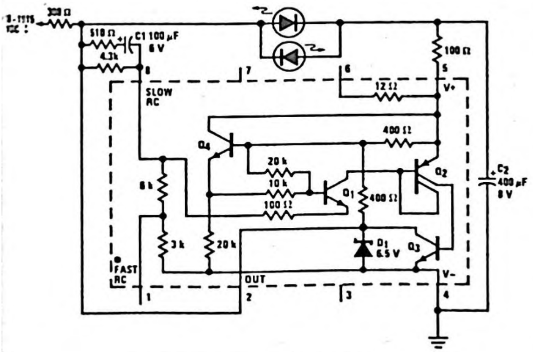


FIGURE 5. Alternating Flasher

The circuit above is a relaxation type oscillator flashing 2 LEDs sequentially. With a 12 VDC supply, repetition rate is 2.5 Hz. C_2, the timing and storage capacitor, alternately charges through the upper LED and is discharged through the other by the IC's power transistor, Q_3.

If a red/green flasher is desired, the green LED should have its anode or plus lead toward pin 5 (like the lower LED). A shorter but higher voltage pulse is available in this position.

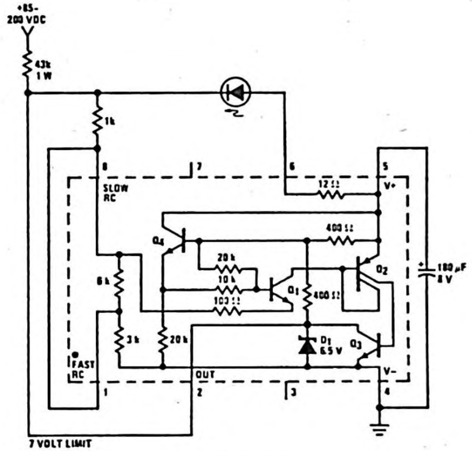


FIGURE 6. Safe, High Voltage Flasher

Indication or monitoring of a high voltage power supply at a remote location can be done much more safely than with neon lamps. If the dropping resistor (43k as in figure 6 above) is located at the source end, all other voltages on the line, the IC, and the LED will be limited to less than 7 V, above ground.

The timing capacitor is charged through the dropping resistor and the two 400 Ω collector loads between pins 2 and 5 of the IC. When capacitor voltage reaches about 5 V, there is enough voltage across the 1k resistor (to pin 8) to turn on Q_1, and hence trigger on the whole IC to discharge the capacitor through the LED.

There are many other LED applications and variations of circuits. A chart outlining operation of the above circuit at various voltages appears on the LM3909 data sheet. Also shown are circuits for adjusting the flash rate, flashing 4 LEDs in parallel, and details for building a blinking locator light into an ordinary flashlight.

Incandescent bulbs can also be flashed, as already illustrated in figure 1. However, most such bulbs draw more than the 150 mA that the LM3909 can switch. The two following circuits therefore use an added power transistor rated at 1 A or more. In each circuit, an NPN transistor is used, so the power transistor's base drive is obtained from the common or ground pin of the flasher IC.

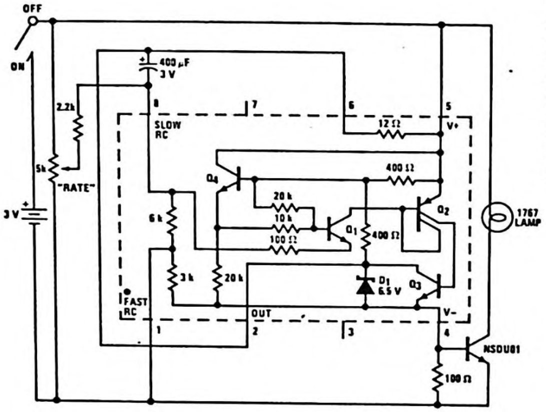

OFF
ON
2.2k
5k
"RATE"
3 V
400 µF
3 V
8
SLOW
RC
7
6
5
12 Ω
V+
Q4
400 Ω
20k
10k
100 Ω
Q1
400 Ω
Q2
1767
LAMP
6k
3k
20k
D1
6.5 V
Q3
FAST
RC
OUT
1
2
3
4
V−
NSDU01
100 Ω

FIGURE 7. "Mini-Strobe" Variable Flasher

The 3 V "mini-strobe" of figure 7 may be used as a variable rate warning light or for advertising or special effects. The rate control is so wide range that it adjusts from no flashes at all to continuously on. Chosen for rapid response, the miniature 1767 lamp can be flashed several times a second.

A "mini-strobe" circuit was tested in a Lantern Flashlight with a large reflector. In a dark room, the flashes were almost fast enough to stop a person's motion. As a toy, the fast setting can mimic the strobes at rock concerts or the flicker of old-time movies.

Figure 8 below shows a higher power application such as would use an automotive storage battery for power. It provides about a 1 Hz flash rate and powers a lamp drawing a nominal 600 mA.

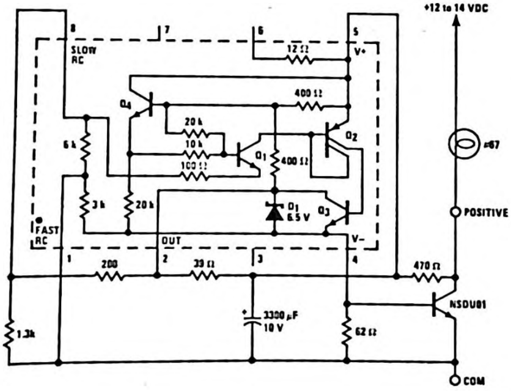
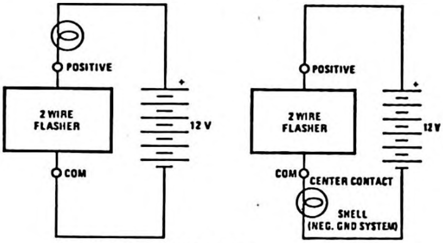

+12 to 14 VDC
8
SLOW
RC
7
6
5
12 Ω
V+
Q4
400 Ω
20k
10k
100 Ω
Q1
400 Ω
Q2
#67
6k
3k
20k
D1
6.5 V
Q3
POSITIVE
FAST
RC
OUT
V−
1
200
2
39 Ω
3
4
470 Ω
NSDU01
3300 µF
10 V
62 Ω
1.3k
COM

FIGURE 8. 12 Volt Flasher (2 Wire)

A particular advantage of this circuit is that it has only 2 external wires and thus may be hooked up in either of the two ways shown below in figure 9. Further, no circuit failure can cause a battery drain greater than that of the bulb itself, continuously lit.


POSITIVE
+
2 WIRE
FLASHER
12 V
COM
POSITIVE
+
2 WIRE
FLASHER
12 V
COM
CENTER CONTACT
SHELL
(NEG. GND SYSTEM)

NOTE: IF FLASHER CASE INSULATED, IT WILL OPERATE IN POSITIVE OR NEGATIVE GROUND SYSTEMS.

FIGURE 9. 2 Wire Flasher Usage

In the circuit of figure 8, the 3300 µF capacitor performs a number of other functions. It makes the LM3909 immune to supply spikes, and provides the means of limiting the IC's supply voltage. Since the LM3909 can only operate with 7.5 V or less on pin 5 (in this circuit) the 200 Ω/1.3k divider attached to pin 8 of the IC causes it to turn fully on at 7 V or less on pin 5. Then the LM3909 discharges the timing capacitor (its own supply voltage) to 4 V or less, whereupon it turns off. The capacitor discharge current comes out of pin 4 of the IC, turning on the NSD U01 transistor. It is the large size of the timing capacitor that allows it to *store* all the needed energy for turning on the power transistor. This in turn permits the whole flasher circuit to operate as a 2 wire device.

Many other flasher possibilities exist. LED flash rate can be varied from 0 to 20 Hz, or a number of LEDs may be flashed in parallel. With a 3 V supply, yellow and green LEDs may be flashed. A 6 V incandescent "emergency lantern" can be made and its PR-13 bulb may be made to give continuous light or flash by switch selection. This is a more reliable, longer lived system than a lantern with a second thermal flasher bulb. The NSL4944 Current Regulated LED makes possible flashing many LEDs in parallel or with high voltages without series resistors.

APPLICATIONS: Audio & Oscillator

Very economical continuity checkers, tone generators, and alarms may be made from the LM3909. No matching transformer is needed because the 150 mA capability of the LM3909 output can drive many standard permanent magnet (transistor radio) loudspeakers directly. The 1.5 V battery used in most applications is both lower in cost and longer lasting than the conventional 9 V battery.

In the continuity checker of figure 10, a short, up to about 100 Ω, across the test probes provides enough power for audible oscillation. By probling 2 values in quick succession, small differences such as between a short and 5 Ω can be detected by differences in tone.

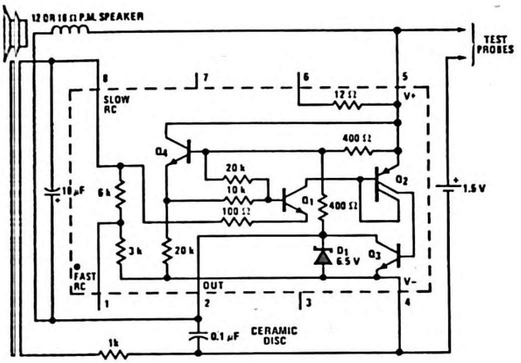


FIGURE 10. "Buzz Box" Continuity and Coil Checker

A novel use of this circuit is found in setting the timing of certain types of motorcycles. This is due to the difference in tone that can be heard from the tester depending whether there is a short or not across the low resistance primary of the 'cycle's ignition coil. In other words, the difference between a 1 Ω resistor and a 1 Ω inductor can be heard. Quick checks for shorts and opens in transformers and motors can therefore be made.

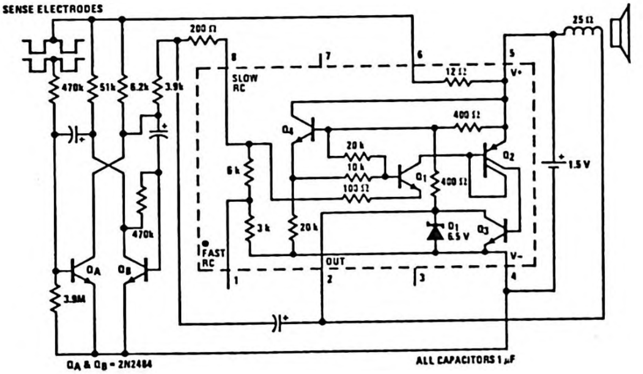
Darkrooms, laundry rooms, laboratories, and cellar workshops can often suffer damage from spills or water seepage ruining lumber, chemicals, fertilizer, bags of dry concrete, etc. The circuit of figure 11 is safe on potentially damp floors since there is no connection to the power line. Further, its standby battery drain of 100 μA yields a battery life close to (or, according to some experiments, exceeding) shelf life.

Without moisture, multivibrator transistor Q_a is completely off, and its collector load (6.2k) provides enough current to hold pin 8 of the LM3909 above 0.75 V where it cannot oscillate. When the sense electrodes pass about 0.25 μA, due to moisture, Q_a starts turning on, and since Q_b is already partially biased on, positive feedback now occurs. Q_a and Q_b are now an astable multivibrator which starts at about 1 Hz and oscillates faster as more leakage passes across the sense electrodes.

This "multi" then acts as both an amplifier and a modulator. The pulse waveform at the collector of Q_a varies the timing current through the 3.9k resistor to pin 8 of the LM3909 resulting in a distinctively modulated tone output.

The sensor should be part of the base of the box the alarm circuitry is packaged in. It consists of two electrodes six or eight inches long spaced about 1/8 inch apart. Two strips of stainless steel on insulators, or the appropriate zig-zag path cut in the copper cladding of a circuit board will work well. The bare circuit board between the copper sensing areas should be coated with warm wax so that moisture on the floor, *not* that absorbed by the board, will be detected. The circuit and sensor can be tested by just touching a damp finger to the electrode gap.

Minimum cost, simplicity, and very low power drain are the aims of the Morse Code set of figure 12. One oscillator simultaneously drives speakers at both sending and receiving ends. Calculations and actual use tests indicate life of a single alkaline penlight cell to be 3 months to over a year depending on usage. "Buzzer" type sets use two or more batteries with much shorter life.

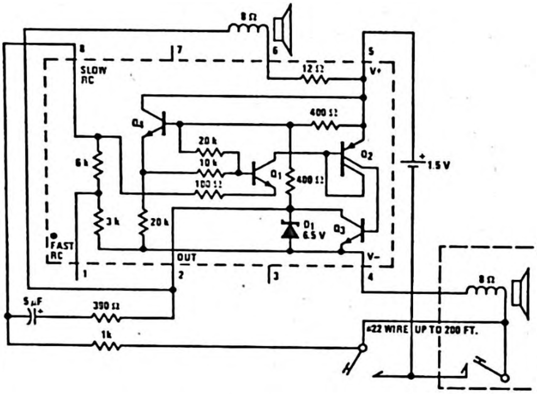


Q_A & Q_B = 2N2484

ALL CAPACITORS 1 μF

FIGURE 11. Water Seepage Alarm

Commonly available, low cost 8 Ω speakers are effectively in series to better match LM3909 characteristics. The three wire system and parallel telegraph keys allow beginners and children to use the set without having to understand use of a "send-receive" switch.



8 Ω
8
7
6
5
SLOW RC
12 Ω
V+
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
6 k
1.5 V
3 k
20 k
D1 6.5 V
Q3
FAST RC
OUT
V-
1
2
3
4
5 μF
390 Ω
1k
8 Ω
#22 WIRE UP TO 200 FT.

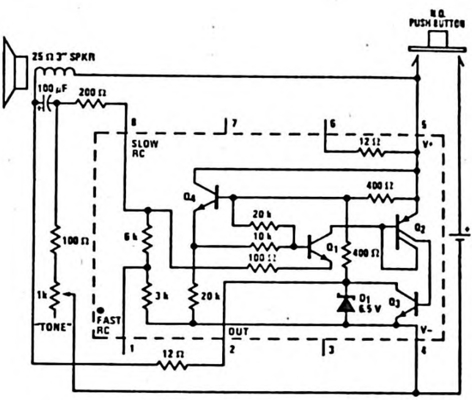
FIGURE 12. Morse Code Set

The two resistors are added to obtain a suitable average power output and electrically force the oscillator toward the desired 50% duty cycle. Acoustically, both speakers are operated at resonance (about 400 Hz in the prototype) for maximum pleasing tone with minimum power drain. Each of the two speaker enclosures has holes added to augment this resonance. For each different type or brand of speaker and size of box, hole and capacitor sizes will have to be determined by experiment for the most stable resonant tone over the expected battery voltage variation.

Experiments with the above circuit led to development of the circuit in figure 13. It is optimized to oscillate at any *acoustic* load frequency of resonance! With just a speaker, oscillation occurs at the speaker cone "free-air" resonance. If the speaker is in an enclosure with a higher resonant frequency . . . this becomes the frequency at which the circuit oscillates.

An educational audio demonstration device, or simply an enjoyable toy, has been fabricated as follows. A roughly cubical box of about 64 in.^{3} was made with one end able to slide in and out like a piston. The box was stiffened with thin layers of pressed wood, etc. Minimum volume with the piston in was about 10 in.^{3}. Speaker, circuit, battery, and all were mounted on the sliding end with the speaker facing out through a 2 1/4 in. hole. A tube was provided (2 1/2 in. long, 5/16 in. ID) to bleed air in and out as the piston was moved while not affecting resonant frequency.

"Slide tones" can be generated, or a tune can be played by properly positioning the piston part and working the push button. Position and direction of the piston are rather intuitive, so it is not difficult to play a reasonable semblance of a tune after a few tries.

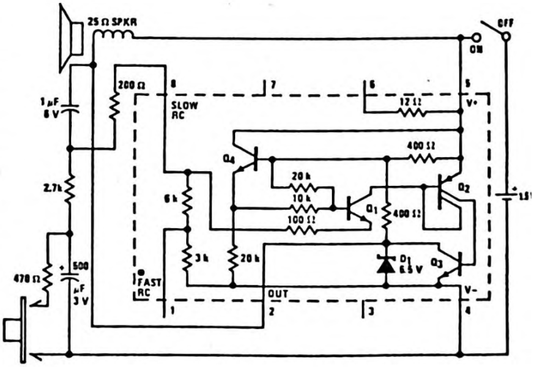


N.O. PUSH BUTTON
25 Ω 3" SPKR
100 μF
200 Ω
8
7
6
5
SLOW RC
12 Ω
V+
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
100 Ω
6 k
1.5 V
1k
3 k
20 k
D1 6.5 V
Q3
"TONE"
FAST RC
OUT
V-
1
12 Ω
2
3
4

FIGURE 13. Electronic "Trombone"

The 12 Ω resistor in series with pin 2 (output transistor Q_3's collector) and the speaker, decouples voltages generated by the resonating speaker system from the low impedance switching action of Q_3. The 100 μF feedback capacitor would normally set a low or even sub-audio oscillation frequency. Therefore, the major positive feedback voltage to pin 8 is the resonant motion *generated* voltage from the speaker voice coil. Therefore the LM3909 will continue to drive the speaker at the resonance with the highest combined amplitude and frequency.

It can be seen already that the LM3909, having direct speaker drive and resonance following capability, can do things that are a lot less practical with older timer and unijunction circuitry. Two final "sound effect" type of circuits are illustrated below.



25 Ω SPKR
OFF
ON
200 Ω
8
7
6
5
SLOW RC
12 Ω
V+
1 μF 6 V
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
2.7k
6 k
1.5 V
3 k
20 k
D1 6.5 V
Q3
470 Ω
500 μF 3 V
FAST RC
OUT
V-
1
2
3
4

FIGURE 14a. Fire Siren

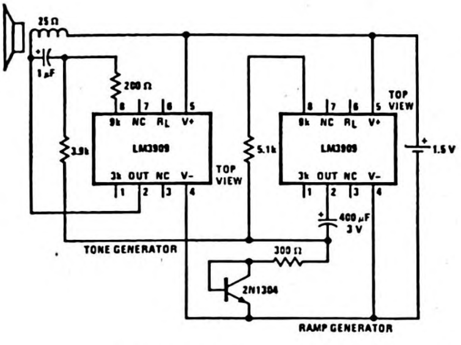


FIGURE 14b. Whooper Siren

The siren of figure 14a produces a rapidly rising wail upon pressing the button, and a slower "coasting down" upon release. If it is desirable to have the tone stop sometime after the button is released, an 18k resistor may be placed between pins 8 and 6 of the IC. The sound is then much like that of a motor driven siren.

In this circuit, the oscillation must not be influenced by acoustic resonances. The 1 μF capacitor and 200 Ω resistor determine a pulse to the speaker that is wider than that for flashing LEDs, but much narrower than is used in the tuned systems of figures 12 and 13. The repetition rate of speaker pulses is determined by the 2.7k resistor, and the charge on the 500 μF capacitor. Discharging this capacitor with the pushbutton increases current in the 2.7k resistor causing a rapid upshift in tone.

The "whooper" of figure 14b sounds somewhat like the electronic sirens used on city police cars, ambulances, and airport "crash wagons." The rapid modulation makes the tone seem louder for the same amount of power input.

The tone generator is the same as in the previous siren. Instead of a pushbutton, a rapidly rising and falling modulating voltage is generated by a second LM3909 and its associated 400 μF capacitor. The 2N1304 transistor is used as a low voltage (germanium) diode. This transistor along with the large feedback resistor (5.1k to pin 8) forces the ramp generator LM3909 into an unusual mode of operation having longer "on" periods than "off" periods. This raises the average tone of the tone generator and makes the modulations seem more even.

APPLICATIONS: Trigger & Other

With its high pulse current capability, the LM3909 is a good pulse-transformer driver. Further, it uses fewer parts and operates more successfully from low voltage supplies than do the equivalent unijunction circuits. The "Triac" trigger of figure 15 operates from a 5 V logic supply and provides gate trigger pulses of up to 200 mA. With no gate input, or a TTL logic high input, the LM3909 is biased off since pin 1 is tied to V+. With a logic low at the gate in, the IC provides 10 μs pulses at about a 7 kC rate. A TTL gate loaded only by this circuit is assumed since otherwise worst-case voltage swing may be insufficient. This trigger is not of the "Synchronized Zero Crossing" type since the first trigger pulse after gating on could occur at any time. However, the repetition rate is such that after the first cycle, a triac is triggered within 8 V of zero with a resistive load and a 115 VAC line.

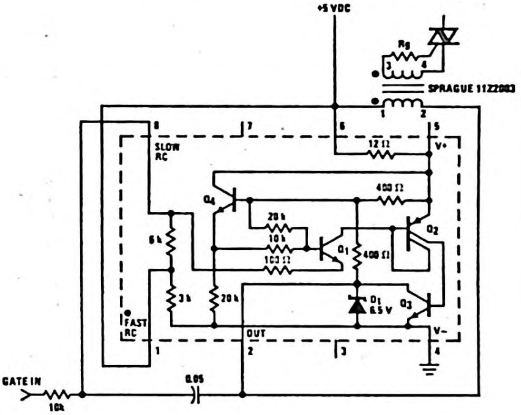


FIGURE 15. Triac Trigger

The standard Sprague PC mounting transformer provides a 2:1 current step-up, and suitable isolation between the low voltage circuitry and power lines up to 240 VAC. Resistor R_g, which includes transformer winding resistance, can be as little as 3 or 4 Ω for high current triacs. Low current types may need excessive "holding" current with such low R_g, so it may be raised to as much as 100 Ω with a sensitive gate triac.

Oscillation of the LM3909 will start when the DC bias at pin 8 is between 1.6 and 3.9 V. In figure 15, pin 8 is connected between the 10k input resistor and a 6k resistor to 5 V. With 3.8 V in, pin 8 is at 4.5 V so there is no oscillation. With 1 V, or less, in, pin 8 is at 3.5 V or below and oscillation occurs. From this example, it can be seen that other input resistors or bias dividers can be calculated to gate the LM3909 triac trigger from other logic levels.

A useful electronic lab device is a precision square wave generator/calibrator. If the output is held at a few tenths percent of 1 V, peak-to-peak, it is useful in calibrating oscilloscopes and adjusting 'scope probes. Many lower cost or battery-portable oscilloscopes do not have this feature built in. Also it is useful in checking gain and transient response of various amplifiers including "hi-fi" power amplifiers.

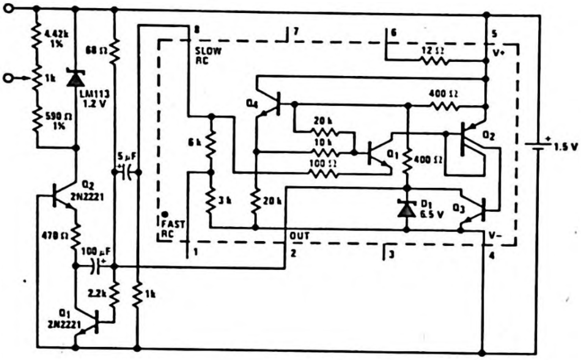


FIGURE 16. 'Scope Calibrator

Battery powered equipment is free from both the inconvenience of a line cord, and from some of the noise and hum effects of equipment attached to the power line. Operation for over five hundred hours from a single flashlight "D" cell is the bonus provided by the circuit below. The lowest reference voltage regulator available, the LM113, is used in conjunction with a current source, and the voltage boost characteristic of the LM3909.

Output is a clean rectangular wave which can be adjusted to exactly a 1 V amplitude. A rectangular wave of approximately 1.5 ms "on" and 5.5 ms "off" was chosen for circuit simplicity and low battery drain. Waveform clipping is virtually flat due to complete turn-off of the current switch Q_2 and the typical "on" impedance of 0.2 Ω provided by the LM113. The 0.01% temperature coefficient of the LM113 at room temperature allows negligible drift of the waveform amplitude under laboratory conditions. Loading by a 'scope probe will also be insignificant.

The circuit will work properly down to battery voltages of 1.2 V. This is because the 100 μF electrolytic capacitor drives the emitter of Q_2 below the supply minus terminal. At a battery voltage of 1.2 V, the collector of Q_2 can still swing more than 1.6 V. Q_1 uses the "off" periods of the LM3909 to insure that the 100 μF capacitor is charged to almost the entire battery voltage. Thus when the LM3909 turns on and pin 2 drives almost to the minus supply voltage, the negative side of the capacitor is driven 0.9 to 1.2 V below this terminal. Low battery voltage cannot lead to an undetected error in the 1 V squarewave. This is because the waveform becomes distorted rather than just decreasing in amplitude as battery voltage becomes too low.

Taking advantage of the versatility and the indestructability of the LM3909 by a 1.5 V battery, the IC can become an ideal teaching means, or experimental device for the young electronic hobbyist. As well as the circuits already presented, the LM3909 can be made to work as amplifier, radio, and even logic type circuits. The ideas of negative and positive feedback can be presented. The circuits presented below are intended as illustrations or demonstrations of circuitry concepts such as would be used in an experimenter's kit. They are not meant to be used as parts of finished commercial products with specific performance specifications. In other words, working circuits have been breadboarded, but no measurements of performance such as frequency range and distortion have been attempted.

Both tuned circuits above use standard AM radio ferrite antenna coils (loopsticks) with a tap 40% of the turns up from one end. The oscillator works up to 800 kHz or so, and the radio tunes the regular AM broadcast band. Both also use standard (360 pF) AM radio tuning capacitors.

The oscillator has the normal capacitive positive feedback used with LM3909 circuits, but with frequency determined by the tuned circuit loading the output circuit. Detailed operating descriptions of these experimenter's circuits will not be attempted in order to keep down the length of this note. Near the end, a discussion of teh IC's general theory of operation will be given, which should help in understanding the individual circuits.

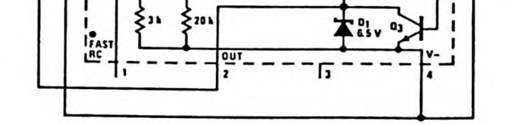


FIGURE 17. R.F. Oscillator

In the radio circuit of figure 18, the LM3909 acts as a detector amplifier. It does not oscillate because there is no positive feedback path from pin 2 to pin 8. The tuning ability is only as good as a simple "crystal set," but a local radio station can provide listenable volume

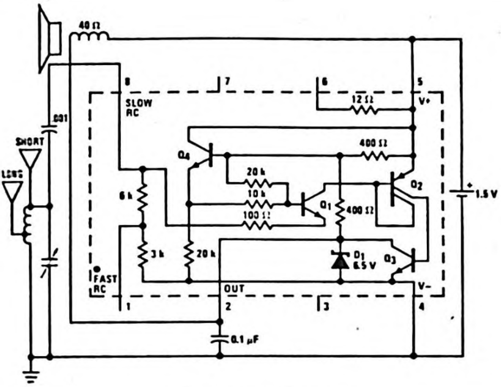

40 Ω
8
7
6
5
SLOW RC
12 Ω
V+
.001
SHORT
LONG
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
1.5 V
6 k
3 k
20 k
D1 6.5 V
Q3
FAST RC
OUT
V−
1
2
3
4
0.1 µF

FIGURE 18. Radio

with an efficient 6 inch loudspeaker. Extremely low power drain allows a month of continuous radio operation from a single "D" flashlight cell.

Antennae for the radio circuit can be short (10 to 20 feet) and connected directly to the end of the antenna coil as illustrated. Longer antennae (30 to 100 feet) work better if attached to the previously mentioned tap on the coil . . . also illustrated.

The following two circuits are examples of logic or computer type functions. They use 3 V power supplies (2 cells) because the LM3909 was designed not to have any stable or "latching" states with a 1.5 V supply.

Switches on both the above circuits are momentary types. In each case a small charge or impulse affects the circuit's state. The circuit of figure 19 switches to and *holds* its condition whenever the switch changes sides, even if contact is made only very briefly. The circuit of figure 20 delivers about a 1/2 second flash from the LED every time its pushbutton makes contact, whether briefly or for a much longer period of time. Such circuits are used with keyboards, limit switches, and other mechanical contacts that must feed data into electronic digital systems.

By again leaving out the positive feedback capacitor, the LM3909 can become a low power amplifier. This little audio amplifier can be used as a one-way intercom or for "listening in" on various situations. Operating current is only 12 to 15 mA. It can hear fairly faint sounds, and someone speaking directly into the microphone generates a full 1.4 V peak-to-peak at the loudspeaker.

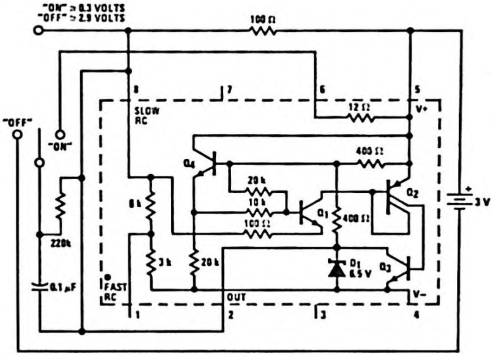

"ON" ≈ 0.3 VOLTS
"OFF" ≈ 2.9 VOLTS
100 Ω
"OFF"
"ON"
8
7
6
5
SLOW RC
12 Ω
V+
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
3 V
6 k
220k
3 k
20 k
D1 6.5 V
Q3
0.1 µF
FAST RC
OUT
V−
1
2
3
4

FIGURE 19. Latch Circuit

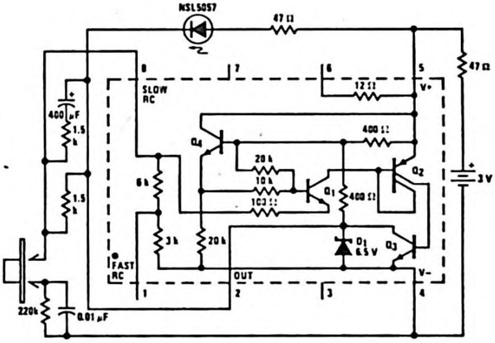

NSL5057
47 Ω
47 Ω
8
7
6
5
SLOW RC
12 Ω
V+
400 µF
1.5 k
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
3 V
6 k
1.5 k
3 k
20 k
D1 6.5 V
Q3
FAST RC
OUT
V−
1
2
3
4
220k
0.01 µF

FIGURE 20. Indicating One-Shot

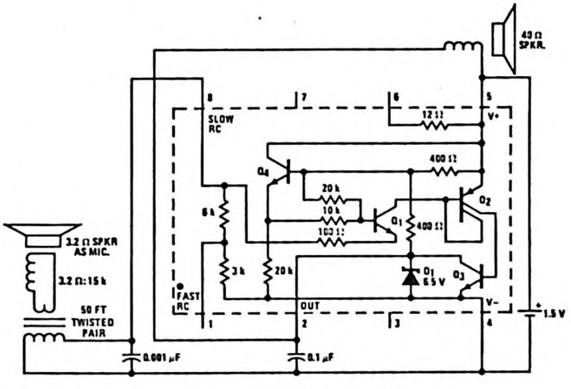

40 Ω SPKR.
8
7
6
5
SLOW RC
12 Ω
V+
400 Ω
Q4
20 k
10 k
100 Ω
Q1
400 Ω
Q2
6 k
3.2 Ω SPKR AS MIC.
3.2 Ω:15 k
3 k
20 k
D1 6.5 V
Q3
FAST RC
OUT
V−
1
2
3
4
1.5 V
50 FT TWISTED PAIR
0.001 µF
0.1 µF

FIGURE 21. Mini-Power Amplifier

APPLICATION HINTS

With 1.5 V supplies, certain problems can occur to stop oscillation or flashing. Due to the way gain is achieved and the type of feedback, too heavy a load may stop an LM3909 from oscillating. 20 Ω of pure resistive *load* will sometimes do it. Strangely enough, lamp filaments, probably because of some inductance, don't seem to follow this rule. Also in flasher circuits, an LED with *leakage* or conductivity between 0.9 and 1.2 V will stop the LM3909. Maybe 1% of LEDs will have this defect because they are not often tested for it.

Great frequency stability was not one of the design aims of the LM3909. In LED flasher circuits it is better than might be expected because the negative temperature coefficient of the LED partially compensates the IC. We planned it this way. Simple oscillators, without the LED, are uncompensated for temperature. This is due to using 1 2/3 of a silicon junction drop as the on-off trip point and the use of the integrated timing resistors with their positive temperature coefficient. Further, most capacitors of 1 μF or over, shown in the circuits, will usually be electrolytics for size reasons. These, however, are not particularly stable with temperature and their initial tolerances vary greatly with type of capacitor.

In most of the oscillator circuits, frequency is also proportional to battery voltage. This must be considered when starting with a completely unused cell at 1.54 V or so and deciding what the "end-of-life" voltage is to be. This can be in the range of 1.1 to 0.9 V, a drastic change. It helps to remember how bright flashlights are with a fresh set of batteries, and how dim they are when the batteries are finally changed.

Flashers and tone generators for alarms are not, however, demanding for stability. Flash rate changes of 50% or tone shifts of 1/2 an octave are not particularly annoying or even too noticeable.

One interesting point is that the low operating power of most of the circuits presented allows them to be powered by *solar cells* as well as regular batteries. In bright sunlight, 3 to 4 cells in series will be needed. In dimmer light, 4 to 6 cells will do the job. Current from cells way under an inch in area generally will be sufficient, but circuits drawing a high pulse current (such as SCR triggers) will need a surge storage capacitor across the solar cell array.

The LM3909 was designed to be inherently self-starting as an oscillator, and LED flasher circuits *are*, at any voltage, because the load is nonlinear. A load with sufficient self inductance will always self-start, although possibly at a higher than expected frequency. There is an exception for largely resistive loads on an oscillator operating with a supply larger than 2 or 2.5 V. A stable state exists with Q_3 turned completely "on" and the timing resistors from pin 8 to the supply minus still drawing current. A reliable solution is to bias pin 8 (for instance with a resistor to V+) so that its DC voltage is one half V less than half the supply voltage.

The duty cycle of the basic LED flasher is inherently low since the timing capacitor is also driving the very low LED "on" impedance. For other oscillators the "on" duty cycle can be stretched by adding resistance in series with the timing capacitor. Additionally, nonlinear resistance can be used as timing resistance. (See figure 14b.)

CONCLUSION

Applications covered in this note range in use from toys to the laboratory, and in frequency from DC to RF. The LM3909 can be used to amuse, teach, or even upon occasion to save a life. As a practical cost consideration the LM3909 IC can often replace a circuit having a number of transistors, associated parts, and high assembly cost.

Further, the LM3909 demonstrates the practicality of very low voltage electronic circuits. They can work at high efficiencies if ingenuity is used to design around transistor junction drops. In such circuits stresses on parts are so low that extremely long life can be predicted. Often transistors, capacitors, etc. that would be rejects at higher voltages can be used. Voltage dividers, protective diodes, etc. often needed at higher voltages can be left out of designs. Power drains are so low that circuits can be made that will last months to years on a single cell.

A single cell is more reliable and has a higher energy density than multiple cells. This is due to lack of cell interconnections and insulation as well as elimination of packaging to hold multiple cells in place.

Specifying A/D and D/A Converters

National Semiconductor
Application Note 156
Jim Sherwin
February 1976

AN-156 Specifying A/D and D/A Converters

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you insure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0245% of full scale. A converter with 10V full scale could resolve a 2.45mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0245% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in 2^{12+1} (±0.0122% of full scale due to finite resolution). This would be the case in figure 1 if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.

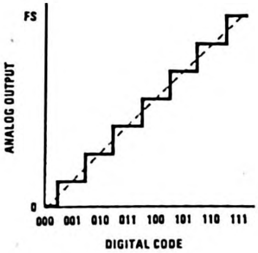


FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in figure 2, exhibits only ±½ LSB maximum output error. If not offset, the error will be $^{-1}_{+0}$ LSB as shown in figure 3. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

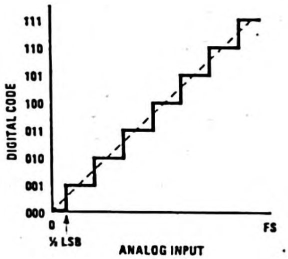


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero

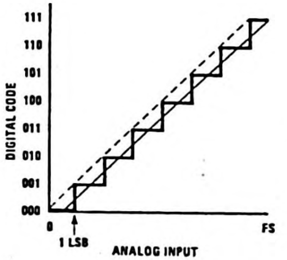


FIGURE 3. ADC Transfer Curve, No Offset

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See figure 4.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient.**) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of figure 7, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

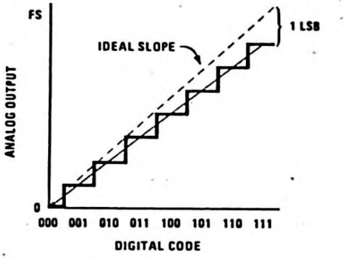


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See figure 5.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

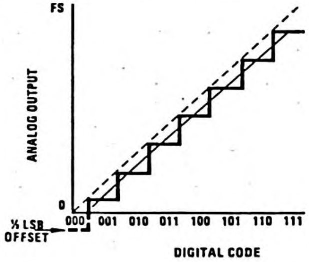


FIGURE 5. Linear, ½ LSB Offset Error

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specification of ±½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to figure 2, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ≤ ±1 LSB differential non-linearity (see below). In the example of figure 6, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. Figure 7 shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

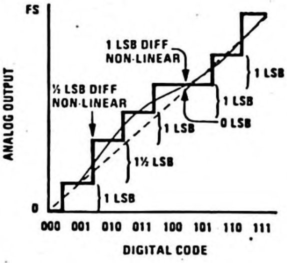


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

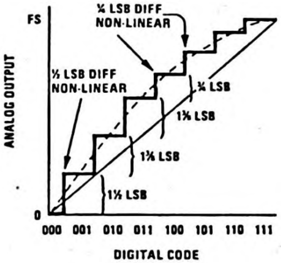


FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see figures 6 and 7). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. Figure 6 shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while figure 7 shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of figure 7 would be preferred over that of figure 6 because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in figure 8 where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in figure 8. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

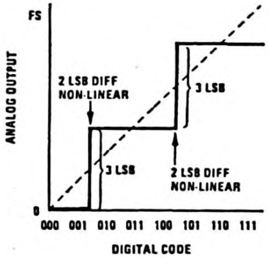


FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

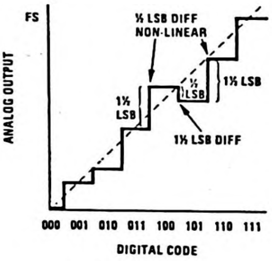
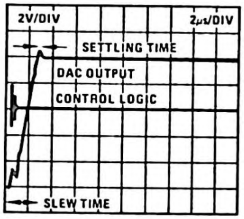
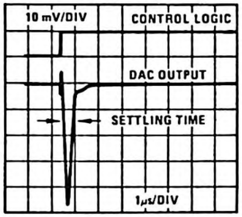


FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)



(a) Full-Scale Step



(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/µs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in figure 10.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

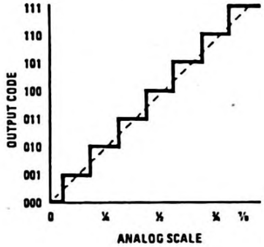
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

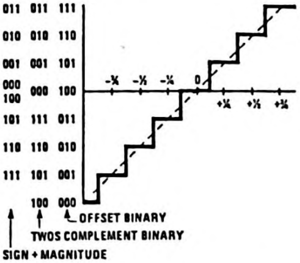
Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in figure 11.

Twos Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number −8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in figure 11. Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(a) Zero to + Full-Scale



(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in figure 11. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

Data Acquisition System Interface to Computers

National Semiconductor
Application Note 159
Jim Sherwin
April 1976

INTRODUCTION

The need of interfacing several analog data channels to computers has not escaped the attention of the data system firms. There are presently available a number of data acquisition units (DAUs) which will directly interface 8-64 analog data channels to one or more types of computers or microcomputers, and more appear on the market almost monthly. Some of these DAUs are even constructed to plug into the mainframe of the computer for which they are designed. Nearly all of these commercially available DAUs are of more or less conventional design, operating in either a random channel address or sequential address mode. Figure 1 shows a typical functional diagram of such a random channel address DAU. Its advantages are simplicity, straightforward design, and comparatively low cost (depending upon performance and special features). In operation, the computer addresses a specific channel, the analog multiplexer (MUX) is set to the desired channel, a sample and hold (S&H) circuit acquires and holds the analog signal, an analog-to-digital converter (ADC) digitizes the signal, a ready signal is returned to the computer, and the data is presented to the data bus via TRI-STATE® bus drivers. If the data is 12-bit and the data bus is 8-bit, the data word must be broken into two bytes and addressed separately. The prime disadvantage of these DAU designs is that the computer must either enter a wait mode while data is readied or it can proceed with its assigned task, watch for a data-ready flag signal, and return for the data.

From the standpoint of microprocessor system design, it is clearly desirable to access input data as if it were main memory. It is further desirable that input data access time be equivalent to that of main memory so that the processor need not enter a wait mode while data is readied for input. One attractive method of accomplishing this is to use one A/D converter (of a type containing TRI-STATE output data latches) on each input data channel. Henceforth I shall refer to this as parallel conversion. Figure 2 shows such a system containing only an address decoder and multiple A/D converters with all outputs wired in parallel onto the data bus. Note the absence of S&H modules.

The advantages of this DAU system are the immediate data access and its simplicity. However, one's first thought on considering a parallel-conversion system might be that the cost of ADCs would exclude their consideration on a one-per-channel basis. But, although this may have been true in the past, currently available monolithic and hybrid ADCs are priced such that this system concept is entirely feasible. Furthermore, the converter price trend is definitely downward as more monolithic units are released, so the economic feasibility can only improve in the next few years, thus extending the application to an ever larger segment of the market. The ideal converter for use in the system of Figure 1 includes converter, comparator, and buffered TRI-STATE output data latches in one package. The unit would

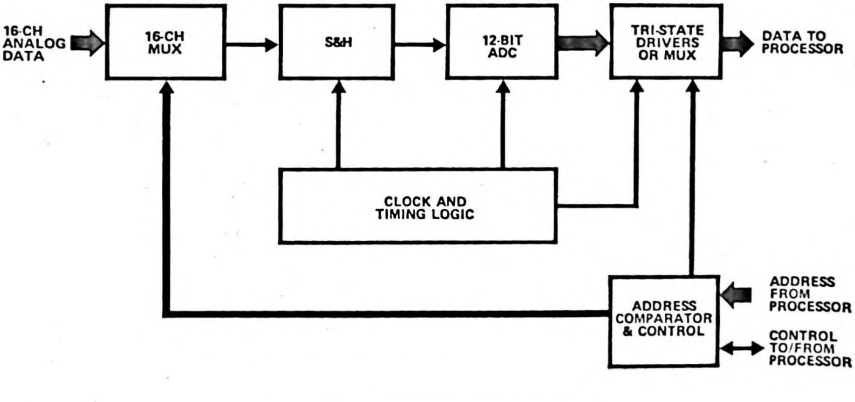


FIGURE 1. Random-Addressed Multiplexed DAU

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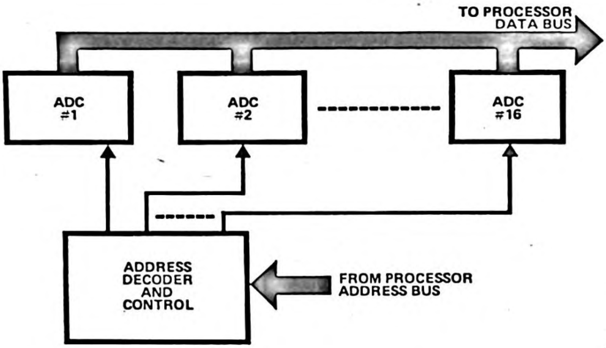


FIGURE 2. Parallel Data Conversion Concept

operate in the continuous convert mode with the last data remaining in the output latches until the next completed conversion shifts new data into the latches. Valid latest data is thus always available for readout on the data bus except for a brief period when the data is being updated. In contrast, a converter without buffered output latches does not hold data after a start-conversion signal and so must be operated in the command mode with a wait for data after the converter is started.

In spite of the advantages of the parallel-conversion DAU, there is (at present ADC prices) a more cost-effective way of providing the same immediate memory-access mode of operation, particularly for 12-bit data. Figure 3 shows a multiplexed DAU with self-contained memory which will interface to computer systems in the memory-access mode without a wait period.

The total package count of this system is lower than that of the parallel-conversion DAU, the cost/channel is lower, and the required space and power is lower. A disadvantage is that the accessed data may be as much as 800μs old, compared to a possible 1-4μs with parallel conversion. The key to the success of the system is the dedicated on-card 16x12 RAM. Neither does the system require a special ADC design with buffered output data latches. Main memory could, of course, be used instead, but then some machine time would be utilized as memory write time. This way, the latest data is always ready and waiting in the DAU (peripheral) memory, and software is considerably simplified.

Before exploring any of the three systems in more detail, it is worth considering the system limitations, the economics, and the probable market segment which could be served by the three types of DAU described.

The required data bandwidth has obvious strong effects on system cost and realization. The bandwidth of a sampled data system is limited by Shannon's sampling criterion and other practical considerations to, say,

$$f_{max} = \frac{1}{5\, t_{conversion}}$$

which is 4kHz for a 50μs conversion cycle time. However, when no S&H module is used ahead of the ADC, as in a parallel-conversion DAU, conversion must take place within the time it takes the input signal to change by ±½ LSB or 1 part in 2^{n+1}. For sine waves, the maximum rate of change is determined as follows:

$$\frac{\Delta v}{\Delta t} = \omega v_{pk},$$

but

$$v_{max} = \frac{2\, v_{pk}}{2^{n+1}}$$

therefore

$$\frac{2\, v_{pk}}{2^{n+1}\, \Delta t} = 2\pi f_{max} v_{pk}$$

and

$$f_{max} = \frac{2^{-(n+1)}}{\pi\, t_{conv}}.$$

For the same 50μs conversion time and an 8-bit accuracy requirement of ±½ LSB, f_{max} is 12Hz. Figure 4 compares data bandwidth of 8- to 14-bit systems with and without S&H. The economic effect of adding an S&H module ahead of each ADC in a parallel-conversion DAU is obvious (possibly doubling the cost per channel of an 8-bit system) as is the cost of significantly increasing conversion speed except by use of tracking converters (advantageous only in parallel-conversion systems).

The conventional random-addressed DAU can serve any part of the data acquisition market where the task of the computer is light enough that the system can afford to enter a wait mode at data request. This wait period can be as low as 10-20μs if sufficient money is available for fast S&H circuits and fast ADCs, as high-speed components are traditionally quite expensive. Lower cost systems may require a wait period of 100-200μs before data is available. At the expense of more complex software, the computer could remain busy during the period of data preparation, and would return for the data when it was made ready. The data bandwidth may be deter-

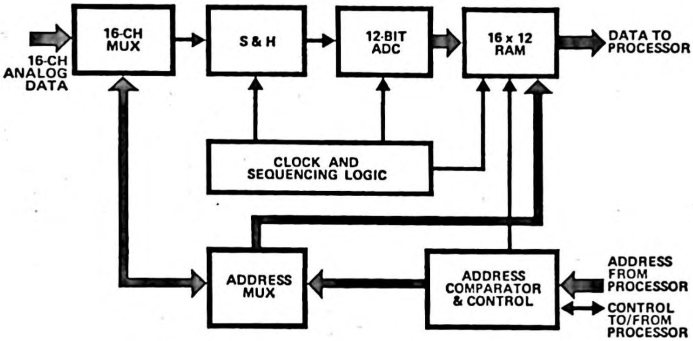


FIGURE 3. Multiplexed Immediate-Data-Access DAU

mined from Figure 4. Sixteen channels of 10 Hz data could be available if each channel were sampled once every 20 ms. This is a data throughput rate of 16 ch x 1/20 ms = 800 Hz. The higher cost DAUs of this type have capability of 50-100 kHz throughput rates. However, if the computer waits while data is made ready, it will be completely occupied with gathering data when the maximum throughput rate is utilized.

The parallel conversion DAU without S&H circuits is destined to operate on low-bandwidth data as indicated in Figure 4. To be economically feasible the ADCs must be of low cost. This means an 8- or 10-bit successive approximation register (SAR) or a 12-bit integrating monolithic ADC must be used. New ADC designs using tracking counters could increase data bandwidth capability over that possible with SAR counters. For purely economic reasons, then, use of parallel-conversion DAU systems will be limited to low bandwidth data — 10-30 Hz on 8-bit, 2-5 Hz on 10-bit, and less than 1 Hz on 12-bit systems. These bandwidth figures for 8- to 10-bit systems could be considerably improved, say by 8-10 times, if tracking converters were used in place of SAR converters. This definitely suggests that there is a need for low-cost tracking converters. Note that S&H circuits are not needed in the parallel-conversion systems.

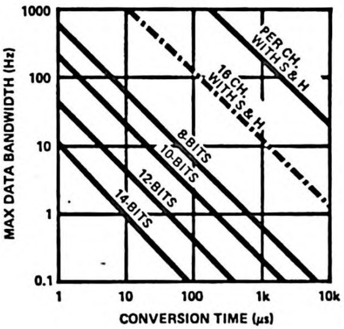


FIGURE 4. Data Bandwidth vs. Conversion Time

The multiplexed DAU with memory can serve any segment of the data market. It is limited in bandwidth or data throughput rate principally by the S&H and ADC operating times, its cost per channel is only slightly higher than that of the conventional DAU, and it allows the computer to operate in the most efficient manner.

A comparison of system costs must include the following for a 16-channel system.

Parallel Conversion	Random Addressed Multiplexed	Multiplexed with Memory
16 A/D Converters	1 A/D Converter	1 A/D Converter
16 Anti-Aliasing Filters	1 S&H Module	1 S&H Module
Control Circuits	1 16-Channel Multiplexer	1 16-Channel Multiplexer
Additional power for extra converters	16 Anti-Aliasing Filters	16 Anti-Aliasing Filters
Lower data bandwidth	More complex control circuits	1 16 x 12 RAM
Simple software	Longer data access time	More complex control circuits
	Possibly more complex software	High-speed data access
		Simple Software

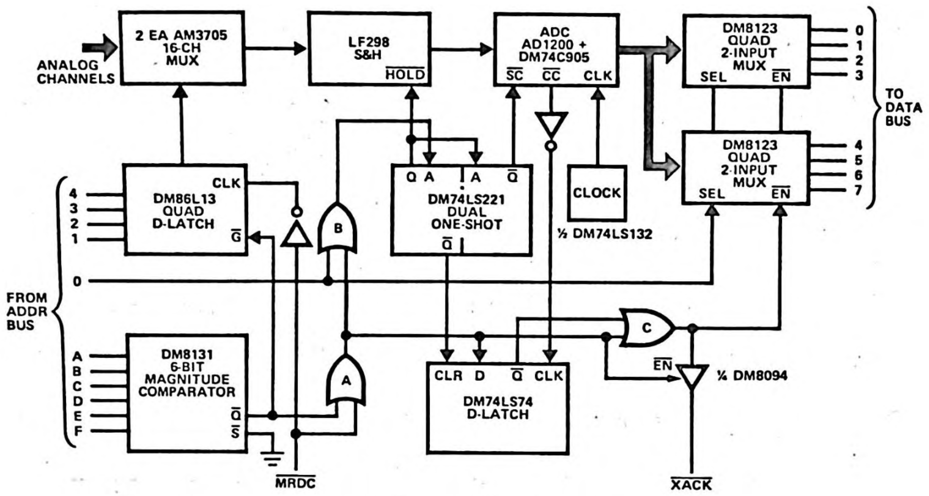


FIGURE 5. Conventional DAU for 8080

The future trends in DAU designs will include an increasing number of parallel-conversion DAUs, especially as cost reductions appear on monolithic ADCs with TRI-STATE output circuits (or latches). We should also start to see some tracking converters in the low-cost monolithics with TRI-STATE output data latches. Expect to see multiplexed DAUs with memory appearing in the near future. Its simplicity from a circuit and software standpoint cannot long go unnoticed.

RANDOM ADDRESSED DATA ACQUISITION UNIT

A conventional, random-addressed, 16-channel, 12-bit DAU is diagrammed in Figure 5. The analog section contains a 16-channel analog multiplexer, a sample-and-hold block, and a 12-bit ADC. A more complete system might contain a differential multiplexer and/or a differential (or instrumentation) amplifier preceding the S&H block. The data output circuits are arranged to interface an 8-bit data bus as found on an 8080 or 6800 microcomputer (μC). Since the data word is 12 bits, the μC must accept it in two 8-bit bytes. Normally the μC would address the DAU with two consecutive address locations corresponding to a 0 and a 1 at the address LSB to load the two bytes of data. The DM8123 multiplexers are ideally suited to this use. They have TRI-STATE output circuits, and the channel-select input may be directly driven from the address LSB. If a 16-bit address bus were being interfaced, such as in the PACE μC, the output multiplexers would be replaced with DM8097 or equivalent TRI-STATE output buffers (see Figure 11). In both instances, low-power versions of these parts, the DM81L23 and DM80L97, could be used to drive a lightly loaded data bus.

The address decoding is accomplished with a DM8161 6-bit magnitude comparator looking at the six most significant address bits. These 6 bits are compared with an address code hard wired into a DIP header which can be different for each DAU card in a system. Comparing only 6 address bits allows a possible 64 cards in a single system and uses up to 64 pages of memory position. If this is not satisfactory, two address comparators ORed together (DM8163) could select from 12 bits of address. The magnitude comparator(s) plus the four address lines to the 16-ch MUX make up the complete address decoding. The output of the magnitude comparator(s) indicates when this DAU has been addressed, and the four address lines to the MUX select the 1-of-16 channels of this DAU.

This circuit is designed to interface the 8080 μC. Thus, a memory read command $\overline{\text{MRDC}}$ must be received, and an acknowledgement $\overline{\text{XACK}}$ must be issued to indicate when data is ready. Operation is as follows: A valid address on address lines A-F causes comparator output $\overline{\text{Q}}$ to go low. This gates the inputs of the quad D latch to accept the 1-of-16 address word from address lines 1-4. At the occurrence of $\overline{\text{MRDC}}$ the address is clocked into the quad D latch and presented to the 16-ch MUX which selects the addressed channel. When $\overline{\text{Q}}$ and $\overline{\text{MRDC}}$ are both low, the output of OR gate A goes low, which enables the XACK signal buffer. If the address LSB is 0 (byte 1 of a 2-byte data request), OR gate B output goes low to trigger a one-shot.

The one-shot circuits are a simple means of timing the sample period and the converter start commands. There are other methods (see Figure 15) of accomplishing this timing without the hazards associated with one-shot circuits; however, the simplicity of this scheme lends itself to easy understanding of the timing required. The first one-shot generates a sample pulse of 5-30μs as required for the S&H to acquire and settle to 0.01% of value. Its $\overline{\text{Q}}$ output presets the single D latch ($\overline{\text{Q}}$ = 1). The trailing edge of this pulse returns the S&H to HOLD condition and triggers the next one-shot to generate a start conversion command of about 3μs. When the ADC completes conversion, its $\overline{\text{CC}}$ output goes low, thus clocking a 0 into the single D latch to reset its Q output low. Both inputs to OR gate C now being low will enable the output MUX and return a low on the $\overline{\text{XACK}}$

line indicating to the μC that data is ready. Address LSB = 0 selects the 8 LSB of the data word for presentation to the data bus. A subsequent address with LSB = 1 selects the 8 MSB of the data word, but will not trigger the one-shot or preset the D latch because the output of OR gate B will remain high. Since the output of OR gates A and C will be low, $\overline{\text{XACK}}$ is returned and the output MUXs are enabled to present byte 2 of the data word on the data bus. When $\overline{\text{MRDC}}$ returns high, the output circuits are disabled. If the 6-bit comparator does not see a valid address, no action is taken by the DAU.

This represents the simplest possible DAU for interfacing to computers. The interface to the 8080 is one of the simplest. Only minor modifications are required to interface, for example, the 6800 or PACE μCs (see Figures 9 and 11). The only timing anomaly in the logic system shown is that when the $\overline{\text{XACK}}$ buffer is enabled there will be a 10-40ns pulse of 0 output. The computer, however, does not act on an XACK signal at this time and so will enter a wait mode until $\overline{\text{XACK}}$ is returned later on.

The analog signal section has purposely been omitted from this discussion of interfacing to processors because its details will depend upon analog signal levels, the possible requirement for differential channels, the possible need of an instrumentation amplifier following the multiplexer, and S&H timing requirements. The analog section of the DAU may be made up of various components, depending upon the required performance and operating conditions. A pair of 8-channel multiplexers will give the flexibility of connecting as differential 8-channel or as single ended 16-channel whereas a single 16-channel MUX with space and wiring on the board for another 16-channel MUX would allow for either 32 channels or 16 differential channels. A pair of AM3705s could be used for lowest cost where analog signals are no greater than ±5V. The S&H circuit could be monolithic LF198, hybrid LH0023, LH0043 or LH0053, made up of individual discrete and integrated circuits, or it could be any of several available modules.

The ADC used in this system may be of a conventional design with speed and accuracy being the only important technical considerations. No special TRI-STATE output or output data latches are needed as the data is latched in the register until a new start conversion (SC) command is given. The ADC could be made up of an AD1200 ADC building block plus DM2504 or MM74C905 successive-approximation register, it could be an AD1210 plus LH0071 reference and appropriate MOS-TTL and TTL-MOS buffers, or it could be any one of a number of other ADCs on the market.

Total power is about 2.8 watts and cost is about $9.50 per channel for components as indicated in Table 1. Note that output drivers are standard TTL circuits whereas low power TTL may be used for lower power dissipation where a lightly loaded data bus is to be driven.

PARALLEL-CONVERSION DATA ACQUISITION UNIT

Parallel data conversion is likely the simplest possible μC data system concept which will effect immediate access to latest input data as if it were main memory. It may be treated as main memory by the processor and is only slightly more complex than the simplified system of Figure 2. The individual ADCs in Figure 2 include TRI-STATE output for direct wire ORing on the data bus. However, to make each capable of driving a heavily loaded system bus would require significant and unnecessary power dissipation in each ADC. Accordingly, except in minimally loaded systems, a separate set of TRI-STATE TTL output data buffers would be added to Figure 2. Small differences in the address decoder and control circuits will exist, depending upon which μC system will be used.

The control circuits are exceptionally simple, being required primarily to accept the memory read command and to return a memory ready signal. The most complex part of the control circuits is that required of μC systems which accept data in two 8-bit bytes rather than in one 16-bit byte, yet even this added complexity is minimal.

Table 1. Conventional DAU Power & Cost

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
2 – DM8123	Quad 2-Input MUX	800	2.56
1 – DM8161	Hex Comparator	250	2.56
1 – DM86L13	Quad D-Latch	30	1.28
1 – DM74LS221	Dual One-Shot	30	3.00
1 – DM74LS132	Quad Schmidt NAND	60	2.00
1 – DM7432	Quad OR Gate	100	.49
1 – DM74LS74	Dual D F-F	20	3.00
1 – DM8094	TRI-STATE 4 x Buffer	144	.71
		2834	150.05
			$9.38/Channel

back out to the μC on the XACK line (+300ns) in advance of the time required. A 0 is placed on the XACK line for the duration of the MRDC command. The MRDC signal also enables the output multiplexer enable lines (+300ns) via the DM8093. This signal also interrupts the clock drive to the ADCs to prevent a change in data output during the remainder of the memory read cycle. A desirable built-in design feature of the ADC for this application might be a clock inhibit or data transfer inhibit operating from the $\overline{EN}$ input. Valid data is present on the data bus (+460ns) at least 200ns before it is required. Valid data remains stable until the end of the MRDC command when XACK and data output lines return to their normal high-impedance states.

Data is placed on the data bus in two 8-bit bytes as controlled by the LSB address code. A 0 selects the 8 LSB data, and a 1 selects the MSB data. Two consecutive memory addresses will then read the entire data word in two bytes. As there are only 12 data bits, zeros are placed on the remaining data lines. For 2s complement binary data coding of ± input analog signals, the 12th bit would be inverted and extended to the remaining data lines so that signals would appear as valid data to the microprocessor.

Total address decode, control, clock, and output drive logic circuitry is contained in six DIP circuits (only one of 24 pins). To this must be added a code-select header, a reference, and 16 converters. Total power required is 4.2 watts for 16 channels of 12-bit data from ±5V analog signals of 10Hz bandwidth (see Table 3). Low Power TTL output drive capability would reduce power drain by 370mW. Total cost of parts (assuming a future price of $25/ADC) would run to about $26 per channel (see Table 4).

Table 3. Power Required, 16-Channel, 12-Bit

			P_D (mW)	
		8080	6800	PACE
16 –	ADC		3200	
1 – LH0071	Reference		45	
1 – DM74LS132	4 x 2-Input NAND Schmidt		60	
1 – DM74L154A	4:16 Decoder		24	
1 – DM8131	6-Bit Comparator		250	
1 – DM8093	4 x Buffer	170		
or 1 – DM8099	6 x NAND Buffer		175	
or 3 – DM8097	6 x Buffer			975
2 – DM8123	4 x 2-Input MUX	400	400	
or 1 – DM86L13	4 x D-Latch			30
		4199	4154	4584

Table 4. Cost of Components, 16-Channel, 12-Bit

			$ (100s)	
		8080	6800	PACE
16 –	ADC		400.00	
1 – LH0071	Reference		5.00	
1 – DM74LS132	4 x 2-Input NAND Schmidt		2.00	
1 – DM74L154A	4:16 Decoder		2.46	
1 – DM8131	6-Bit Comparator		2.56	
1 – DM8098	6 x Inverter	1.65		
or 1 – DM8099	6 x NAND Buffer		1.70	
or 3 – DM8097	6 x Buffer			5.55
2 – DM8123	4 x 2-Input MUX	2.56	2.56	
or 1 – DM86L13	4 x D-Latch			1.28
		416.23	416.28	418.85
			≈ $26/Channel	

6800 Interface

For other μC systems, the logic will change slightly. Figure 9 shows the logic section of the DAU of Figure 7 modified as necessary to interface with the 6800 μC. The 6800 timing and control signals are shown in Figure 10. With the 6800, the address information, the valid memory address VMA signal, and the read/write W/R signal all come up approximately simultaneously and remain for about one clock period of 1μs (min.). The data need not appear on the data bus until 100ns thereafter. The valid address decoding is accomplished by ANDing the VMA and R/W signals together in a TRI-STATE 2-input AND gate. When enabled by the comparator output, this gate returns a READY signal to the μC and enables the output multiplexers. The appropriate data byte is selected by the LSB address bit as with the 8080 system. The necessary 10ns data hold time is provided by the ADC and output multiplexer disable delays. The remainder of the DAU is identical to that of Figure 7. Cost and power required are also similar to those of the 8080 system interface.

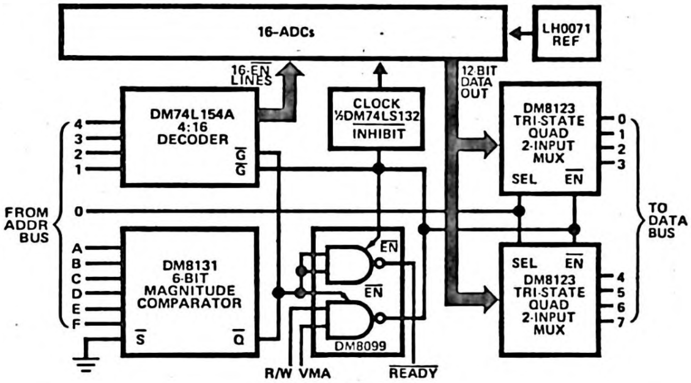

16-ADCs
LH0071 REF
16-$\overline{EN}$ LINES
12 BIT DATA OUT
DM74L154A 4:16 DECODER
$\overline{G}$
$\overline{G}$
CLOCK ½DM74LS132
$\overline{INHIBIT}$
DM8123 TRI-STATE QUAD 2-INPUT MUX
SEL
$\overline{EN}$
0
1
2
3
4
3
2
1
FROM ADDR BUS
0
A
B
C
D
E
F
DM8131 6-BIT MAGNITUDE COMPARATOR
$\overline{S}$
$\overline{Q}$
$\overline{EN}$
$\overline{EN}$
DM8099
R/W
VMA
$\overline{READY}$
TO DATA BUS
SEL
$\overline{EN}$
DM8123 TRI-STATE QUAD 2-INPUT MUX
4
5
6
7

FIGURE 9. 16-Ch, 12-Bit Parallel-Conversion DAU for 6800

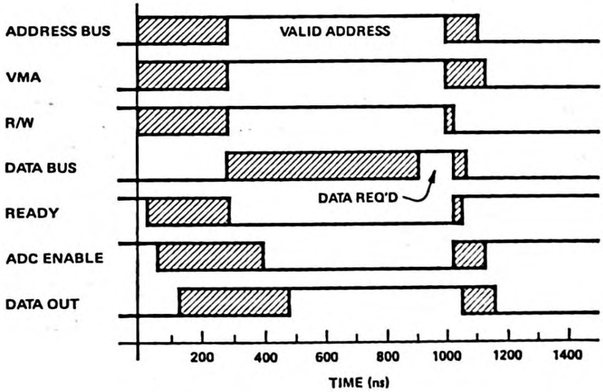


FIGURE 10. Timing and Control for 6800

PACE Interface

Figure 11 shows the logic section of the DAU of Figure 7 modified to interface with a PACE μC. The PACE timing is shown in Figure 12. Since the PACE μC has but a single address/data bus, address latches are required for address decoding. The DM8131 address comparator contains output latches, but the DM74L154A 4:16 decoder does not, so a quad latch is inserted ahead of the 4:16 decoder. The latches all set on the rising edge of the NADS signal provided by PACE during the time that address information is on the bus, and drop out on the next NADS signal. Comparator output applied to gate the 4:16 decoder provides an enable ADC signal lasting until the falling edge of the next NADS pulse. The IDS signal ANDed with the comparator output enables the TRI-STATE output buffers and inhibits the clock. An additional MSB inverter would be needed for ± analog signals in order to provide the 2s complement code. Total address decode, control, clock, and output drive circuitry is contained in seven DIP packages, one more than required for the 8080 system interface. Total power and cost are comparable to those given for the 8080 system interface.

ADC CHARACTERISTICS

The ADC for use on a parallel-conversion DAU must contain TRI-STATE output data latches. Otherwise it may be conventional. The MM5357 was designed for direct connection to a data bus, therefore it contains the necessary output latches. At this writing there are other ADCs with the TRI-STATE output latches appearing on the market, and more can be expected. The MM5357 is nearly ideal for use in an 8-bit parallel-conversion DAU. It would be even more suitable to this use if it were a tracking converter, and the polarity of its enable input and of its data output were of opposite polarity. The data polarity is of lesser importance as the bus drivers probably needed may as well be inverting as non-inverting except for common usage. The enable polarity should match the decoder output to obviate the need for 16 inverters (3 logic packages, though of little cost). See the later discussion of ADC hardware for additional thoughts on this subject.

This parallel-conversion data system has data bandwidth limited to about 10Hz for 8-bit SAR converters, but may be increased to 150-300Hz with 8-bit tracking

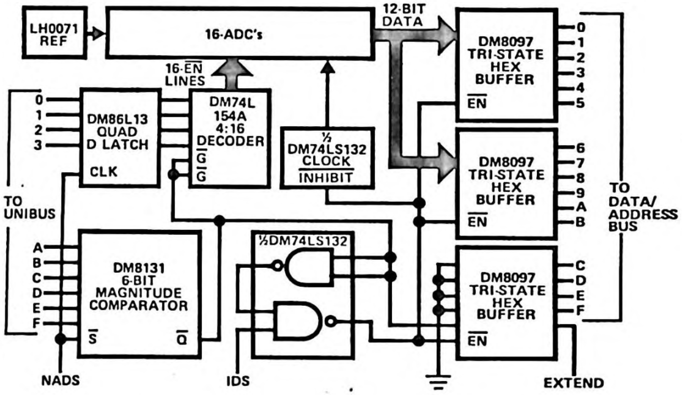

LH0071 REF
16-ADC's
12-BIT DATA
16-EN LINES
DM8097 TRI-STATE HEX BUFFER
EN
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
DM86L13 QUAD D LATCH
CLK
DM74L 154A 4:16 DECODER
G
G
½ DM74LS132 CLOCK INHIBIT
TO UNIBUS
DM8131 6-BIT MAGNITUDE COMPARATOR
S
Q
½DM74LS132
TO DATA/ ADDRESS BUS
NADS
IDS
EXTEND

FIGURE 11. 16-Ch, 12-Bit Parallel-Conversion DAU for PACE

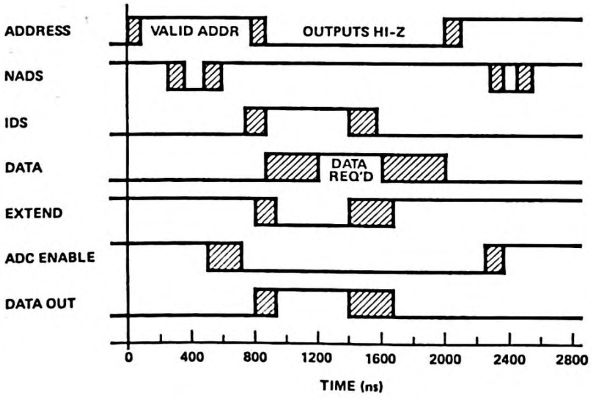

ADDRESS
NADS
IDS
DATA
EXTEND
ADC ENABLE
DATA OUT
VALID ADDR
OUTPUTS HI-Z
DATA REQ'D
0
400
800
1200
1600
2000
2400
2800
TIME (ns)

FIGURE 12. Timing and Control for PACE

converters. 12-bit data bandwidth will be 1/16 that of the 8-bit systems. On the other hand, no S&H module is required. Data rates could be considerably increased if S&H modules were added to each channel; however, costs per channel would more than double. For use with S&H modules, SAR logic converters would be faster than tracking types, allowing data bandwidths of over 600Hz/channel for 12-bit data.

MULTIPLEXED DATA ACQUISITION UNIT WITH MEMORY

A multiplexed data acquisition system containing memory is probably the most cost-effective way of providing an immediate data-access interface to processors. The processor may address the peripheral data-acquisition unit to obtain immediate data without entering a wait mode, just as if it were accessing main memory. Latest valid data is always present within the DAU memory which is updated at a rate determined by the channel multiplexer rate and ADC conversion speed. There is no need to write subroutines into processor software or firmware to address and request data from the peripheral, resume its assigned processing task while watching for a flag set by the peripheral indicating that data is ready, and returning to accept data from the peripheral.

The multiplexed DAU with memory shown in Figure 3 takes care of routinely updating its memory by sequentially sampling each data channel, digitizing the channel signals, and writing data into its self-contained memory. When the DAU is interrogated, the sequential process is momentarily interrupted, the RAMs are addressed by the processor, and data is read out to the data bus. The memory can be three each DM8599 16x4-bit RAMs. These have TRI-STATE outputs, so can connect directly to the data bus. Note that the RAM inverts the data bits from the ADC. The RAMs are available in low-power TTL to drive a lightly loaded data bus, or they are available in Schottky versions for driving higher speed systems. In fact, almost the entire logic system could be realized in Schottky circuits, which should allow interfacing even the new fast bipolar μCs without a wait cycle.

The MUX sequencing circuits are shown in Figure 13. When the μC is not accessing memory on the DAU, the 16 data channels are scanned in continuous sequence.

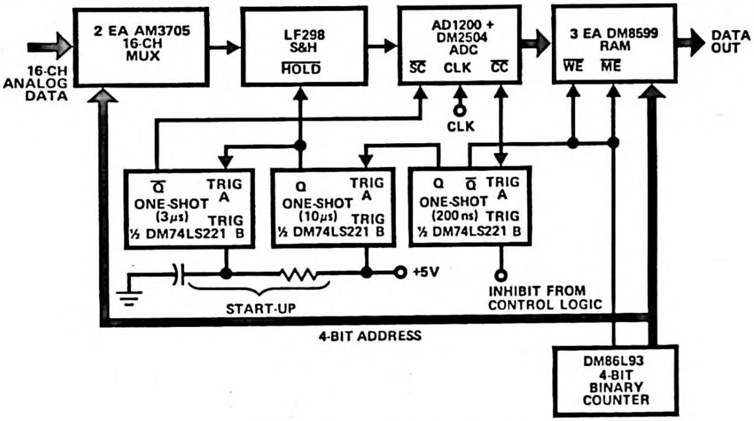

16-CH ANALOG DATA
2 EA AM3705 16-CH MUX
LF298 S&H
$\overline{\text{HOLD}}$
AD1200 + DM2504 ADC
$\overline{\text{SC}}$ CLK $\overline{\text{CC}}$
3 EA DM8599 RAM
$\overline{\text{WE}}$ $\overline{\text{ME}}$
DATA OUT
CLK
$\overline{\text{Q}}$ TRIG A ONE-SHOT (3μs) TRIG B ½ DM74LS221
Q TRIG A ONE-SHOT (10μs) TRIG B ½ DM74LS221
Q $\overline{\text{Q}}$ TRIG A ONE-SHOT (200 ns) TRIG B ½ DM74LS221
+5V
START-UP
INHIBIT FROM CONTROL LOGIC
4-BIT ADDRESS
DM86L93 4-BIT BINARY COUNTER

FIGURE 13. Sequencing Logic with OS

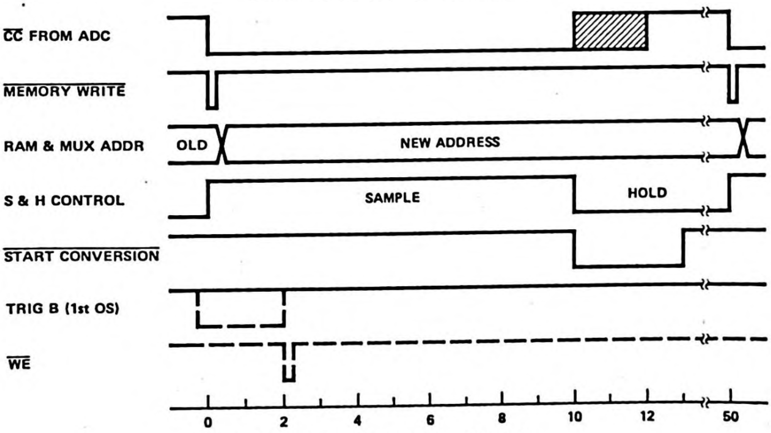


FIGURE 14. Timing for One-Shot Sequencing

Data on each channel is sampled and held in the S&H module while the ADC converts the analog data to digital. At the completion of conversion, the digital output of the ADC is written into the RAMs before the multiplexer selects the next channel. The timing and sequencing of channels is accomplished with a 4-bit binary (÷ 16) counter and three one-shot pulse generators. Where one-shots are undesirable, an alternate approach using shift register timing could provide the same function. A valid address output from the address comparator switches the RAM address input from the ÷16 counter to the address bus input, thereby addressing the RAM to the desired channel for data readout. If the data conversion sequence is in the memory write condition, the gate applied to WE prevents switching the MUX to the address bus or returning an XACK signal until the memory has been loaded. Thereupon, the sequence is interrupted as outlined above. The interruption of the sequence lasts for about 1300ns (8080 system) while the address is valid.

The sequential data conversion cycle is shown in the timing signals of Figure 14. The conversion-complete $\overline{\text{CC}}$ output of the ADC triggers a one-shot to generate a 200ns memory write pulse. The trailing edge of this pulse advances the address ÷ 16 counter to the next channel and triggers a second one-shot to produce a 10μs sample period. At the completion of the sample period, the S&H goes into hold mode and a third one-shot generates a 3μs start conversion $\overline{\text{SC}}$ pulse. When the DAU is in the command read mode, a 0 appears at B trigger input to the first one-shot. If a $\overline{\text{CC}}$ signal occurs during the time the 0 is present on the B input, the one-shot will not be triggered until the B input returns to a 1.

An alternate sequencing circuit without one-shot circuits is shown in Figure 15 with timing relationships in Figure 16. It makes use of a shift register and exclusive-OR gates to generate the gates needed to write into memory, sample and hold, and start conversion. The ADC clock is generated at twice the desired clock frequency and divided by 2 in a D flip-flop. In this manner, the minimum gate width is 1/4 of the ADC clock period (620ns in this example). The $\overline{\text{CC}}$ signal is clocked into a D flip-flop with a delay of 620ns. The delayed output clears the shift register (SR) and is clocked into the SR after an additional 620ns delay. An exclusive-OR of the SR input and Q1 output generates a 620ns gate to write data into the RAMs. The trailing edge of this $\overline{\text{WE}}$ gate clocks the ÷ 16 counter to advance the MUX and RAM address to the next channel. Exclusive-ORing of SR Q1 and Q7 produces an 8.75μs sample gate. (If the acquisition and settling time of the S&H is greater than 8.75μs, additional circuit complexity is required.) Exclusive-ORing of Q7 and Q8 produces a synchronized 1.25μs gate to start the ADC. This circuit may not be the most versatile or elegant for the purpose. For those applications with longer S&H acquisition times or other requirements, some alternate circuit may be designed if that of Figure 15 is unacceptable.

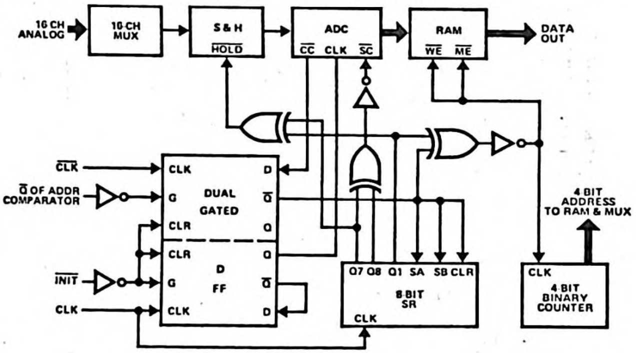


FIGURE 15. Sequencing Logic with SR

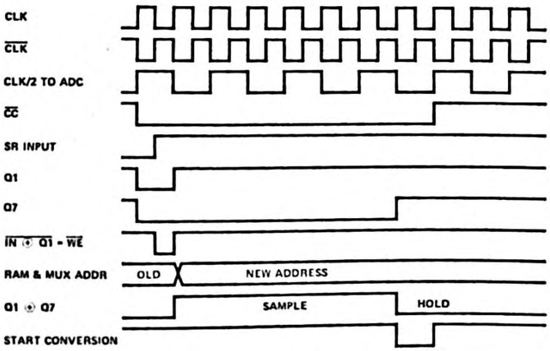


FIGURE 16. Timing for S-R Sequencing

The μ-computer interfaces shown in Figures 17 and 18 are similar to that of Figure 5. The PACE interface is seen to be slightly less complex than that of Figure 17 for 8-bit data-bus machines. A single DAU card with plug-in or strap options could be built to interface any of the three μCs considered. Such a universal circuit is shown in Figure 19. This circuit also includes an option to provide binary output for unipolar analog signals or complementary binary output for ± signals. In the case of binary output, the 13-16th data bits are set to 0. In the case of complementary binary, the sign bit is extended to the 13-16thdata bitsfor valid recognition by the μC.

The total dissipation is 3.5 watts and cost is $11 per channel as shown in Table 5. Both are only slightly greater than those for the conventional DAU.

The ADC desired for this application is similar to the conventional ADC except that the ADC data output should be complementary to compensate for the data inversion within the RAMs. The AD1210 or AD1200 are thus ideal choices for an ADC in the multiplexed DAU with memory.

CONVERTER CHARACTERISTICS

Each approach to the DAU requires different characteristics of the ADC. Table 6 summarizes the requirements for each of the three DAU types. The sequential or addressed DAU types require similar ADCs. If the conventional addressed DAU must utilize bus drivers, the desired ADC characteristics are identical to those for the sequential DAU with memory. Only the parallel-conversion DAU is seen to require buffered TRI-STATE output latches.

By far the most important characteristic of an ADC for use in a parallel-conversion DAU is that it have buffered TRI-STATE output latches. It is desirable that it also have the other characteristics checked in Table 6. Items 1 and 2 are by far the most important of the desired characteristics. The need for item 1 has been discussed. TTL compatible control and data signals are desirable so that TTL-MOS and MOS-TTL interface buffers are not required between the ADC and the rest of the system. Dual output strobing makes it possible to wire-OR interface directly to an 8-bit data bus or to use only an 8-line buffer without the need for the output multi-

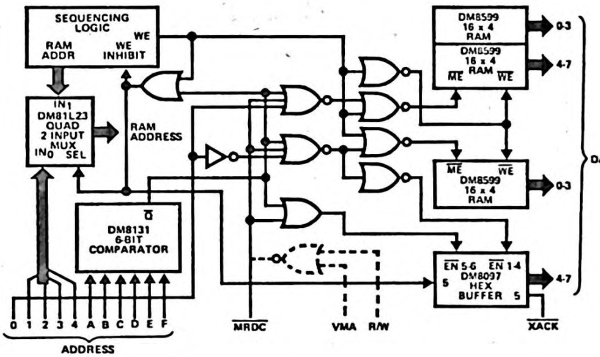

SEQUENCING LOGIC
WE
RAM ADDR
WE INHIBIT
IN1
DM81L23 QUAD 2 INPUT MUX
IN0
SEL
RAM ADDRESS
$\overline{Q}$
DM8131 6-BIT COMPARATOR
DM8599 16 x 4 RAM
DM8599 16 x 4 RAM
$\overline{ME}$
$\overline{WE}$
0-3
4-7
$\overline{ME}$
$\overline{WE}$
DM8599 16 x 4 RAM
0-3
$\overline{EN}$ 5-6
$\overline{EN}$ 1-4
5
DM8097 HEX BUFFER
5
4-7
DATA
0 1 2 3 4 A B C D E F
ADDRESS
$\overline{MRDC}$
VMA
R/W
$\overline{XACK}$

FIGURE 17. Address Comparator and Control for 8080 (6800)

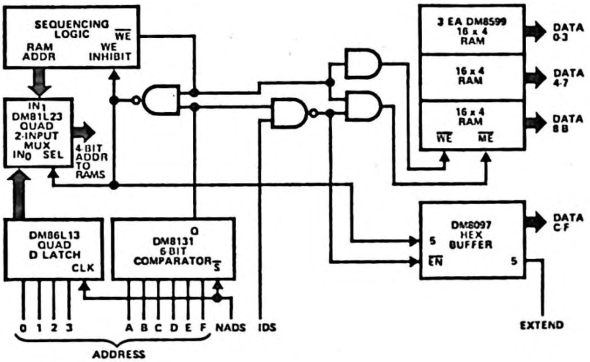

SEQUENCING LOGIC
$\overline{WE}$
RAM ADDR
WE INHIBIT
IN1
DM81L23 QUAD 2-INPUT MUX
IN0
SEL
4 BIT ADDR TO RAMS
DM86L13 QUAD D LATCH
CLK
Q
DM8131 6 BIT COMPARATOR
$\overline{S}$
3 EA DM8599 16 x 4 RAM
16 x 4 RAM
16 x 4 RAM
$\overline{WE}$
$\overline{ME}$
DATA 0-3
DATA 4-7
DATA 8-B
DM8097 HEX BUFFER
5
$\overline{EN}$
5
DATA C-F
0 1 2 3
A B C D E F
NADS
IDS
EXTEND
ADDRESS

FIGURE 18. Address Comparator & Control for PACE

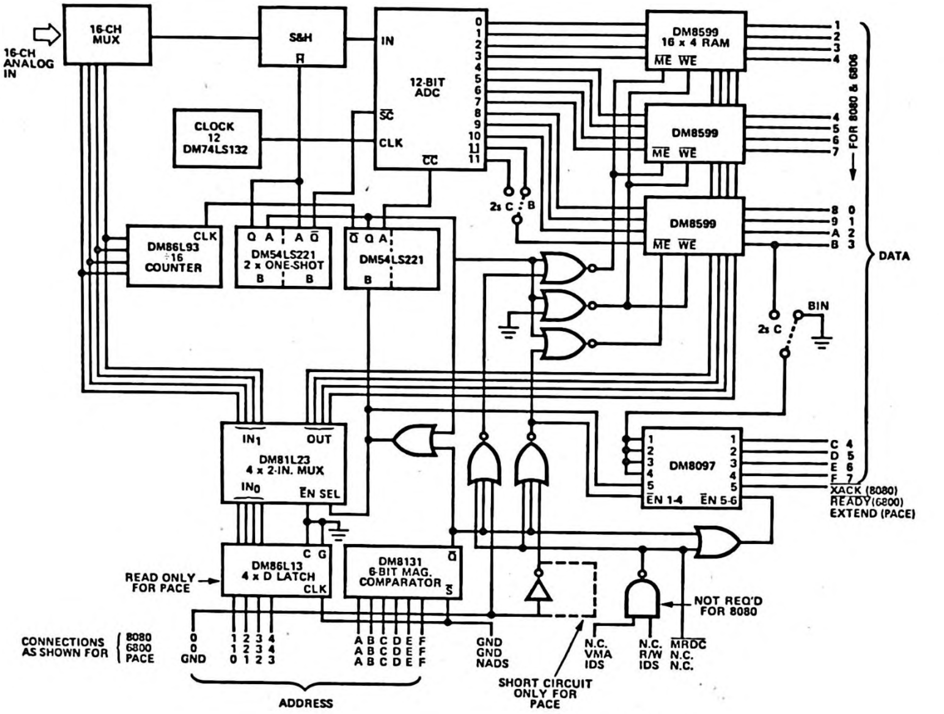

16-CH ANALOG IN
16-CH MUX
S&H
H
IN
12-BIT ADC
SC
CLK
CC
0
1
2
3
4
5
6
7
8
9
10
11
11
CLOCK 12 DM74LS132
DM8599 16 x 4 RAM
ME WE
DM8599
ME WE
DM8599
ME WE
1
2
3
4
4
5
6
7
8 0
9 1
A 2
B 3
FOR 8080 & 6800
DATA
2s C
B
BIN
2s C
CLK
DM86L93 ÷16 COUNTER
Q A A Q̄
DM54LS221 2 x ONE-SHOT
B B
Q̄ Q A
DM54LS221
B
IN1 OUT
DM81L23 4 x 2-IN. MUX
IN0 EN SEL
DM8097
1 2 3 4 5
1 2 3 4 5
EN 1-4 EN 5-6
C 4
D 5
E 6
F 7
XACK (8080)
READY (6800)
EXTEND (PACE)
C G
DM86L13 4 x D LATCH
CLK
DM8131 6-BIT MAG. COMPARATOR
Q̄
S
READ ONLY FOR PACE
CONNECTIONS AS SHOWN FOR 8080 6800 PACE
0 0 GND
1 1 0
2 2 1
3 3 2
4 4 3
A A A
B B B
C C C
D D D
E E E
F F F
ADDRESS
GND GND NADS
SHORT CIRCUIT ONLY FOR PACE
N.C. VMA IDS
N.C. R/W IDS
MRDC N.C. N.C.
NOT REQ'D FOR 8080

FIGURE 19. Multiplexed Immediate-Data-Access DAU

Table 5. Power & Cost, 16-Channel, 12-Bit Sequential with Memory

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
1 – LH0070	Reference	45	5.00
3 – DM8599	256-Bit RAM	1200	15.36
1 – DM8097	6 x Buffer	325	1.65
1 – DM8131	6-Bit Comparator	250	2.56
1 – DM81L23	4 x 2-Input MUX	20	2.00
1 – DM74LS27	3 x 3-Input NOR	17	3.00
1 – DM7402	4 x 2-Input NOR	55	.35
1 – DM74L32	4 x 2-Input OR	12	.64
1 – DM86L93	÷16 Counter	25	2.11
2 – DM74LS221	2 x One-Shot	60	6.00
1 – DM74LS132	4 x NAND Schmidt	60	2.00
1 – DM86L13	4 x D-Latch	30	1.28
		3500	176.00
			$11/Channel

plexers shown in Figure 5 et. al., although a separate buffer is required in most systems. Tracking operation provides the higher speed useful in a conversion circuit without an S&H. Inhibiting data transfer to output data latches when the output is enabled prevents changing the output code while data is being read from the data bus. This function can be accomplished with an external gate, but could be convenient if handled within the ADC logic. Straight binary (not complemented) output is desired for all μC interfaces (except the 8080 when operating with Intel system bus drivers and receivers). As it may be necessary to add TRI-STATE line drivers to drive the data bus, data inversion can be handled by inverting buffers when required. The availability of both Q and $\overline{\text{Q}}$ outputs on the MSB simplifies data readout as binary or 2s complement without adding an external inverter. Table 6 has been arranged in the approximate order of preference for parallel-conversion DAU use; the preference will be different for multiplexed data.

The National MM5357 is the choice for an 8-bit ADC having buffered TRI-STATE output latches and TTL compatibility when converting ±5 or 0-5V analog inputs. If converting 0-10V inputs, it becomes 10V CMOS compatible. Several monolithic ADCs of 8 to 12 bits have been announced. These monolithic converters and future versions of them promise to bring converter prices down to a level which will make parallel-conversion economically feasible. Several hybrid converters have also been announced with attractive prices; however, it is the monolithics which promise the lowest ultimate cost. Features of several of these new products are compared in Table 7. Although only the MM5357 and the AD7550 are suitable in present form, their prices and characteristics show that the desired attributes are and will be possible at the needed prices.

The future ADC most suited for use in a parallel-conversion DAU might appear as in Figure 20. This

Table 6. Desired A/D Converter Characteristics

	Parallel Conversion	Sequential w/ Memory	Addressed w/o Memory
Buffered TRI-STATE Output Data Latches	x		?
TTL-Compatible Control & Data Signals	x	x	x
Dual Output-Enable (Bits 0-7 & Bits 8-11)	x		x
Counter Logic	UP/DN	SAR	SAR
Internal Comparator	x	x	x
Both Q & $\overline{\text{Q}}$ Outputs on MSB	x	x	x
Binary Output Polarity	Data*	$\overline{\text{Data}}$	Data*
Busy Output (TRI-STATE w/ Enable)	?		x
Internal Clock		x	x
Continuous Recycle when CC = SC	x		
Inhibit Data XFR to Latches when Enabled	x		

* Unimportant if Buss drivers used.

Table 7. Low-Cost Monolithic and Hybrid ADCs

	National MM5357	Analog Devices AD7570L	Teledyne 8702	National AD1210 (Hybrid)	Analog Devices AD7550
Number of Bits	8	10	12	12	13
Cost (in 100s)	$7.95	$69.00 (1-49)	$29.50	$24.95	$25.00
Conversion Method	Potentiometric	R-2R	Differential Charge Balancing	R-2R	Integrating
Logic Type	PMOS SAR	CMOS SAR	CMOS Integrating	CMOS SAR	CMOS Quad Slope
Conversion Time	25μs	20μs + Comp. Settling	20ms	130μs	40ms
Logic Interface at 5V	TTL	TTL	TTL	TTL	TTL
Analog Sig. 0-10V	CMOS	TTL/CMOS	TTL	CMOS	TTL/CMOS
External Circuits Required	Ref + Clock	Ref + Comparator	Ref	Ref + Clock	Ref
Output Buffered Latch?	Yes	No	Yes	No	Yes
TRI-STATE Output?	Yes	Yes	No	No	Yes
Separate Output Enables?	NA	Yes	Not Strobed	No	Yes
Output Code	Inverted	Normal	Normal	Inverted	2s Complement
Power Dissipation	170mW Dynamic	10mW Standby + Dynamic + Comparator	20mW Dynamic	140mW Dynamic	10mW Dynamic

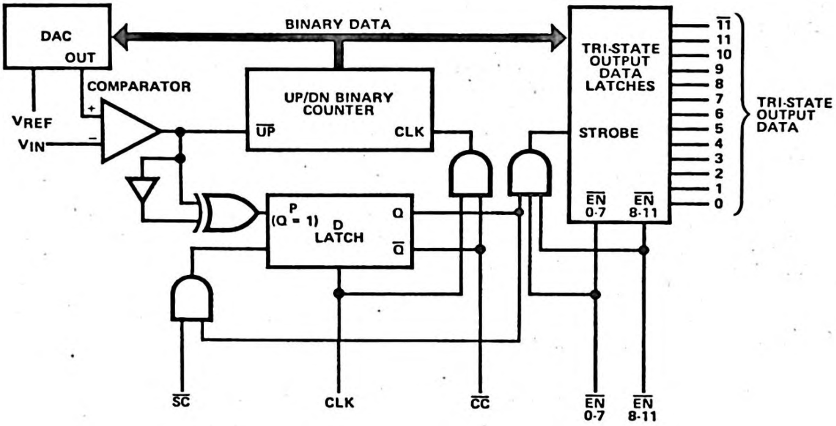


FIGURE 20. Tracking ADC for Parallel-Conversion DAU

design meets all the goals of Table 6. It could run at a clock rate of 0.25-1 MHz (1-4 μs conversion time) because it is a tracking converter, it contains TRI-STATE buffered output data latches, the separate high and low bit-enable lines allow two-byte operation of an 8-bit data bus, the output latches will not change state when the output is enabled, and the $\overline{CC}$ and $\overline{SC}$ terminals may be strapped for continuous conversion without missing a clock period. An 8- or 10-bit converter and possibly a 12-bit converter of this type could be built on a single chip without much difficulty. If not, a hybrid or two-chip design is practical. Where speed is not of importance, monolithic 10- or 12-bit converters can be built with integrating or voltage-to-frequency conversion techniques. The integrating technique possibly allows the greatest accuracy with the least circuitry, and is a prime contender for the application. As the integrating ADC utilizes both linear and digital circuits, it is normally of multi-chip design. However, as technology advances, it will become increasingly practical to produce the low-drift, low-offset amplifiers, integrators, and current sources required of a 12-bit ADC on a single reasonably small chip along with the necessary logic. A two-chip approach would likely be the choice today. We will certainly see some of these desired design features appearing on ADCs in the near future.

As far as ADCs and DACs are concerned, the entire makeup of their internal logic sections is different from that of conventional converters of today (except for the MM5357 and AD7550). Tables 6 and 8 outline the desired characteristics of ADCs and DACs for parallel-conversion and multiplexed systems. Figures 20 and 21 indicate the logic required. The ADC of Figure 20 is suitable for relatively high speed data acquisition without S&H circuits, while that of Figure 21 is suitable for slowly varying data only.

DATA DISTRIBUTION SYSTEMS

Until now, the discussion has centered entirely around the data acquisition end of the system. At first thought, the data distribution may seem almost trivial. However, there is still the address recognition and decoding plus the control functions. The conventional data distribution unit (DDU) has used a single DAC, a multi-channel analog demultiplexer, low-pass filters and possibly S&H

Table 8. Desired D/A Converter Characteristics

	Parallel Conversion	Multiplexed System
Hi-Z Digital Input Circuits	x	x
Strobed Data Input Latches	x	x
Dual Input Data Strobes (Bits 0-7 & Bits 8-11)	x	x
Optional Internal Inversion of MSB	x	x
Internal Output Amp & FB Resistors	x	?
Internal Reference	?	x

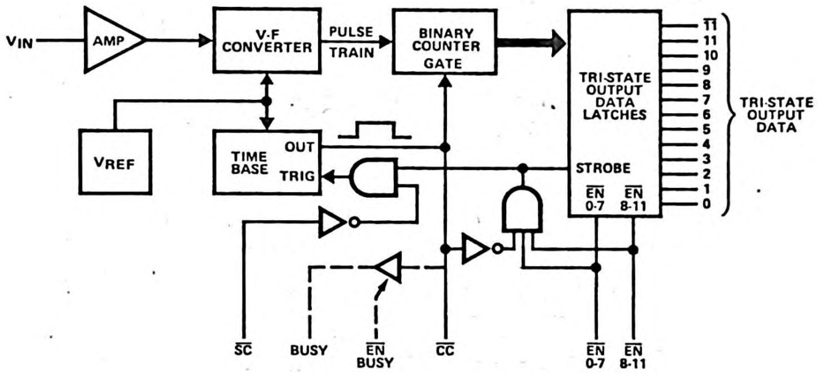


FIGURE 21. V-F ADC for Parallel-Conversion DAU

circuits on each channel reconverted to analog form. Such a system could benefit from a DAC with input data latches and separate (double-byte) input gating or strobing controls while a parallel-conversion DDU has even more need of these input characteristics.

The parallel-conversion DDU shown in Figure 22 would, if constructed with available DACs, require 12-bit input data latches ahead of each DAC. The characteristics desired of a DAC for this use are listed in Table 8. High impedance digital inputs prevent loading the data bus while a strobed input data latch allows entering data only in the addressed DAC and holding it until updated (thus performing the function of DAC and S&H). Separate input data strobes for low and high bits are used for the same reason as with the ADC, for alternate enabling on successive input data bytes. Figure 23 outlines the desired DAC for use in a parallel-conversion DDU.

The DDU address decoding and complexity is similar to that of the DAU. Input data strobing separated as 8 LSB and the remaining MSB is an advantage when used on 8-bit data bus systems. The cost per channel is essentially that of the DAC used. Likewise, for power dissipation. Practicality will be entirely dependent on ultimate cost of the converters. Advantages over a demultiplexed system are that only minimal output filters are required and that an output amplifier per channel is not required (already exists in each DAC).

CONCLUSION

Each type of DAU described exhibits unique advantages as indicated in the comparisons of Table 9.

Further reduction in the costs of monolithic converters will make the parallel-conversion type of DAU attractive where low-speed data is handled. For 8-bit data, this type of DAU is extremely attractive at this time because the DAU cost per channel is essentially that of an ADC which is as low as $8 in lots of 100.

It would seem that the multiplexed DAU with memory exhibits all of the advantages of the conventional random-addressed DAU plus all those of the parallel data conversion DAU except that the data in any specific channel may be older. Offsetting this single comparative disadvantage are significantly lower cost per channel, lower power requirements, and no requirement for special ADCs with buffered output latches. The multiplexed approach with memory is only slightly more complex or costly than a standard DAU, yet it brings the great advantage of high-speed immediate data access with significant cost savings over the parallel conversion technique.

Although the character of an ADC or DAC used in a parallel-conversion data system differs markedly from those used in the usual multiplexed data system, the processor interface requirements are similar or identical. The sense of µC bus control signals is of relatively minor importance so long as they are standardized among the several µC units available. Positive-true data and address signals are possibly a slight advantage over zero-true signals when TRI-STATE circuits are used. For the multiplexed system described, data inversion through the RAM would suggest the advantage of complementary binary output data from an ADC.

Conventional ADCs and DACs available today (except the MM5357 and AD7550) do not have the characteristics needed for parallel-conversion systems. However, this picture is changing as more units are designed for direct data bus interface. Fortunately, however, the multiplexed DAU with memory does not require the bus oriented type of ADC. There is at least one available DAC which includes the dual-strobed input data latches suggested for direct data bus interface; I would expect to see others appearing in future designs, both monolithic and hybrid.

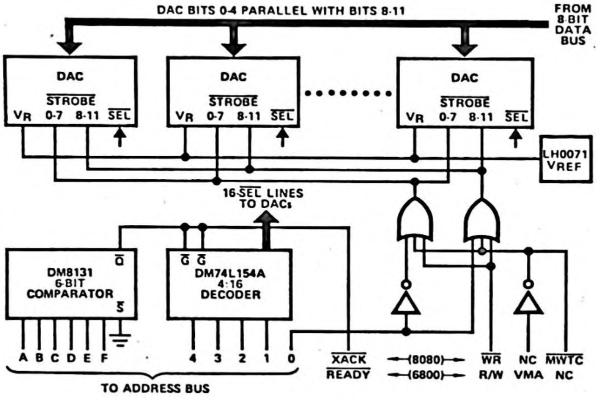

DAC BITS 0-4 PARALLEL WITH BITS 8-11
FROM 8-BIT DATA BUS
DAC
STROBE
VR 0-7 8-11 SEL
LH0071 VREF
16-SEL LINES TO DACs
DM8131 6-BIT COMPARATOR
Q
S
G G
DM74L154A 4:16 DECODER
A B C D E F
4 3 2 1 0
TO ADDRESS BUS
XACK ←(8080)→ WR NC MWTC
READY ←(6800)→ R/W VMA NC

FIGURE 22. Parallel-Conversion DDU for 6800 or 8080

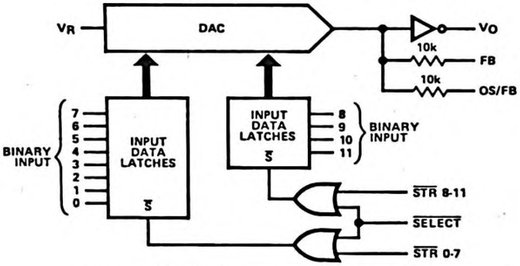

VR
DAC
VO
10k
FB
10k
OS/FB
7
6
5
4
3
2
1
0
BINARY INPUT
INPUT DATA LATCHES
S
INPUT DATA LATCHES
S
8
9
10
11
BINARY INPUT
STR 8-11
SELECT
STR 0-7

FIGURE 23. DAC for Parallel-Conversion DAU

Table 9. Comparison of Three Types of DAU

Features of DAU 16-Channel, 12-Bit	Conventional Random-Addressed	Parallel-Conversion Without S&H	Multiplexed With Memory
Approx. Component Cost (100s) (based on a $25 ADC)	$9.38	$26	$11
Approx. Power Dissipation	2.8W	4.3W	3.5W
Data Bandwidth/Channel $t_{conv} = 50\mu s$ t_{acq} (S&H) = $10\mu s$	200 Hz	10 Hz (tracking: $t_{conv} = 4\mu s$)	200 Hz
Data Access Time	$60\mu s$	$< 0.5\mu s$	$< 0.5\mu s$
Software	$60\mu s$ delay or subroutine and return on flag	as memory access	as memory access
Logic Interface Complexity	9 DIP	6 DIP	13 DIP
No. of IC Packages			
ADC Requirement		TRI-STATE buffered output data latches	

IC Voltage Reference has 1 ppm per Degree Drift

National Semiconductor
Application Note 161
Robert C. Dobkin
June 1976

A new linear IC now provides the ultimate in highly stable voltage references. Now, a new monolithic IC the LM199, out-performs zeners and can provide a 6.9V reference with a temperature drift of less than 1 ppm/° and excellent long term stability. This new IC, uses a unique subsurface zener to achieve low noise and a highly stable breakdown. Included is an on-chip temperature stabilizer which holds the chip temperature at 90°C, eliminating the effects of ambient temperature changes on reference voltage.

The planar monolithic IC offers superior performance compared to conventional reference diodes. For example, active circuitry buffers the reverse current to the zener giving a dynamic impedance of 0.5Ω and allows the LM199 to operate over a 0.5 mA to 10 mA current range with no change in performance. The low dynamic impedance, coupled with low operating current significantly simplifies the current drive circuitry needed for operation. Since the temperature coefficient is independent of operating current, usually a resistor is all that is needed.

Previously, the task of providing a stable, low temperature coefficient reference voltage was left to a discrete zener diode. However, these diodes often presented significant problems. For example, ordinary zeners can show many millivolts change if there is a temperature gradient across the package due to the zener and temperature compensation diode not being at the same temperature. A 1°C difference may cause a 2 mV shift in reference voltage. Because the on-chip temperature stabilizer maintains constant die temperature, the IC reference is free of voltage shifts due to temperature gradients. Further, the temperature stabilizer, as well as eliminating drift, allows exceptionally fast warm-up over conventional diodes. Also, the LM199 is insensitive to stress on the leads—another source of error with ordinary glass diodes. Finally, the LM199 shows virtually no hysteresis in reference voltage when subject to temperature cycling over a wide temperature range. Temperature cycling the LM199 between 25°C, 150°C and back to 25°C causes less than 50μV change in reference voltage. Standard reference diodes exhibit shifts of 1 mV to 5 mV under the same conditions.

SUB SURFACE ZENER IMPROVES STABILITY

Previously, breakdown references made in monolithic IC's usually used the emitter-base junction of an NPN transistor as a zener diode. Unfortunately, this junction breaks down at the surface of the silicon and is therefore susceptible to surface effects. The breakdown is noisy, and cannot give long-term stabilities much better than about 0.3%. Further, a surface zener is especially sensitive to contamination in the oxide or charge on the surface of the oxide which can cause short-term instability or turn-on drift.

The new zener moves the breakdown below the surface of the silicon into the bulk yielding a zener that is stable with time and exhibits very low noise. Because the new zener is made with well-controlled diffusions in a planar structure, it is extremely reproducible with an initial 2% tolerance on breakdown voltage.

A cut-away view of the new zener is shown in *Figure 1.* First a small deep P+ diffusion is made into the surface of the silicon. This is then covered by the standard base diffusion. The N+ emitter diffusion is then made completely covering the P+ diffusion. The diode then breaks down where the dopant concentration is greatest, that is, between the P+ and N+. Since the P+ is completely covered by N+ the breakdown is below the surface and at about 6.3V. One connection to the diode is to the N+ and the other is to the P base diffusion. The current flows laterally through the base to the P+ or cathode of the zener. Surface breakdown does not occur since the base P to N+ breakdown voltage is greater than the breakdown of the buried device. The buried zener has been in volume production since 1973 as the reference in the LX5600 temperature transducer.

CIRCUIT DESCRIPTION

The block diagram of the LM199 is shown in *Figure 2.* Two electrically independent circuits are included on the same chip—a temperature stabilizer and a floating active zener. The only electrical connection between the two

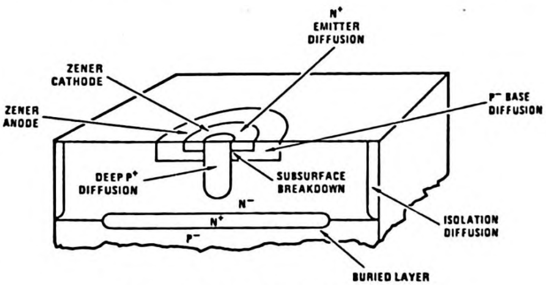


FIGURE 1. Subsurface Zener Construction

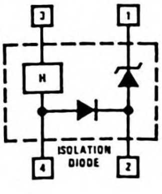


FIGURE 2. Functional Block Diagram

circuits is the isolation diode inherent in any junction-isolated integrated circuit. The zener may be used with or without the temperature stabilizer powered. The only operating restriction is that the isolation diode must never become forward biased and the zener must not be biased above the 40V breakdown of the isolation diode.

The actual circuit is shown in *Figure 3.* The temperature stabilizer is composed of Q1 through Q9. FET Q9 provides current to zener D2 and Q8. Current through Q8 turns a loop consisting of D1, Q5, Q6, Q7, R1 and R2. About 5V is applied to the top of R1 from the base of Q7. This causes 400μA to flow through the divider R1, R2. Transistor Q7 has a controlled gain of 0.3 giving Q7 a total emitter current of about 500μA. This flows through the emitter of Q6 and drives another controlled gain PNP transistor Q5. The gain of Q5 is about 0.4 so D1 is driven with about 200μA. Once current flows through Q5, Q8 is reverse biased and the loop is self-sustaining. This circuitry ensures start-up.

The resistor divider applies 400 mV to the base of Q4 while Q7 supplies 120μA to its collector. At temperatures below the stabilization point, 400 mV is insufficient to cause Q4 to conduct. Thus, all the collector current from Q7 is provided as base drive to a Darlington composed of Q1 and Q2. The Darlington is connected across the supply and initially draws 140 mA (set by current limit transistor Q3). As the chip heats, the turn on voltage for Q4 decreases and Q4 starts to conduct. At about 90°C the current through Q4 appreciably increases and less drive is applied to Q1 and Q2. Power dissipation decreases to whatever is necessary to hold the chip at the stabilization temperature. In this manner, the chip temperature is regulated to better than 2°C for a 100°C temperature range.

The zener section is relatively straight-forward. A buried zener D3 breaks down biasing the base of transistor Q13. Transistor Q13 drives two buffers Q12 and Q11. External current changes through the circuit are fully absorbed by the buffer transistors rather than D3. Current through D3 is held constant at 250μA by a 2k resistor across the emitter base of Q13 while the emitter-base voltage of Q13 nominally temperature compensates the reference voltage.

The other components, Q14, Q15 and Q16 set the operating current of Q13. Frequency compensation is accomplished with two junction capacitors.

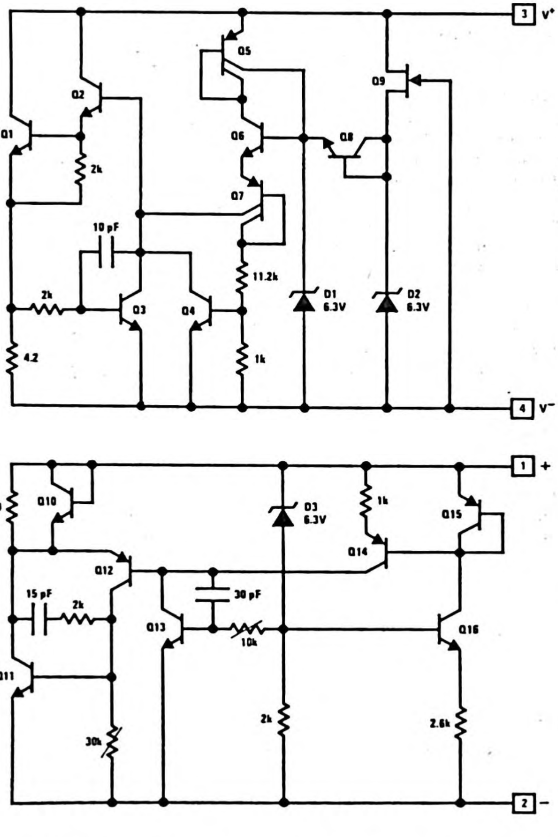


FIGURE 3. Schematic Diagram of LM199 Precision Reference

PERFORMANCE

A polysulfone thermal shield, shown in *Figure 4,* is supplied with the LM199 to minimize power dissipation and improve temperature regulation. Using a thermal shield as well as the small, high thermal resistance TO-46 package allows operation at low power levels without the problems of special IC packages with built-in thermal isolation. Since the LM199 is made on a standard IC assembly line with standard assembly techniques, cost is significantly lower than if special techniques were used. For temperature stabilization only 300 mW are required at 25°C and 660 mW at −55°C.

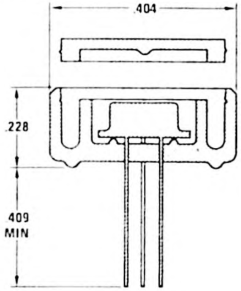


FIGURE 4. Polysulfone Thermal Shield

Temperature stabilizing the device at 90°C virtually eliminates temperature drift at ambient temperatures less than 90°C. The reference is nominally temperature compensated and the thermal regulator further decreases the temperature drift. Drift is typically only 0.3 ppm/°C. Stabilizing the temperature at 90°C rather than 125°C significantly reduces power dissipation but still provides very low drift over a major portion of the operating temperature range. Above 90°C ambient, the temperature coefficient is only 15 ppm/°C.

A low drift reference would be virtually useless without equivalent performance in long term stability and low noise. The subsurface breakdown technology yields both of these. Wideband and low frequency noise are both exceptionally low. Wideband noise is shown in *Figure 5* and low frequency noise is shown over a 10 minute period in the photograph of *Figure 6.* Peak to peak noise over a 0.01 Hz to 1 Hz bandwidth is only about 0.7μV.

Long term stability is perhaps one of the most difficult measurements to make. However, conditions for long-term stability measurements on the LM199 are considerably more realistic than for commercially available certified zeners. Standard zeners are measured in ±0.05°C temperature controlled both at an operating current of 7.5 mA ±0.05μA. Further, the standard devices must have stress-free contacts on the leads and the test must not be interrupted during the measurement interval. In contrast, the LM199 is measured in still air of 25°C to 28°C at a reverse current of 1 mA ±0.5%. This is more typical of actual operating conditions in instruments.

When a group of 10 devices were monitored for long-term stability, the variations all correlated, which indicates changes in the measurement system (limitation of 20 ppm) rather than the LM199.

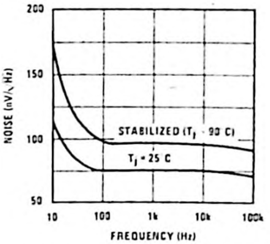


FIGURE 5. Wideband Noise of the LM199 Reference

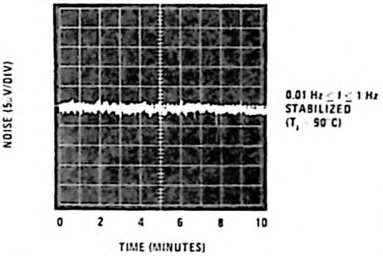


FIGURE 6. Low Frequency Noise Voltage

Because the planar structure does not exhibit hysteresis with temperature cycling, long-term stability is not impaired if the device is switched on and off.

The temperature stabilizer heats the small thermal mass of the LM199 to 90°C very quickly. Warm-up time at 25°C and −55°C is shown in *Figure 7.* This fast warm-up is significantly less than the several minutes needed by ordinary diodes to reach equilibrium. Typical specifications are shown in Table I.

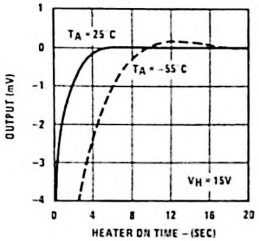


FIGURE 7. Fast Warmup Time of the LM199

Table I. Typical Specifications for the LM199

Reverse Breakdown Voltage	6.95V
Operating Current	0.5 mA to 10 mA
Temperature Coefficient	0.3 ppm/°C
Dynamic Impedance	0.5Ω
RMS Noise (10 Hz to 10 kHz)	7μV
Long-Term Stability	≤20 ppm
Temperature Stabilizer Operating Voltage	9V to 40V
Temperature Stabilizer Power Dissipation (25°C)	300 mW
Warm-up Time	3 Seconds

APPLICATIONS

The LM199 is easier to use than standard zeners, but the temperature stability is so good—even better than precision resistors—that care must be taken to prevent external circuitry from limiting performance. Basic operation only requires energizing the temperature stabilizer from a 9V to 40V power source and biasing the reference with between 0.5 mA to 10 mA of current. The low dynamic impedance minimizes the current regulation required compared to ordinary zeners.

The only restriction on biasing the zener is the bias applied to the isolation diode. Firstly, the isolation diode must not be forward biased. This restricts the voltage at either terminal of the zener to a voltage equal to or greater than the V^-.

A dc return is needed between the zener and heater to insure the voltage limitation on the isolation diodes are not exceeded. *Figure 8* shows the basic biasing of the LM199.

The active circuitry in the reference section of the LM199 reduces the dynamic impedance of the zener to about 0.5Ω. This is especially useful in biasing the reference. For example, a standard reference diode such as a 1N829 operates at 7.5 mA and has a dynamic impedance of 15Ω. A 1% change in current (75μA) changes the reference voltage by 1.1 mV. Operating the LM199 at 1 mA with the same 1% change in operating current (10μA) results in a reference change of only 5μV. *Figure 9* shows reverse voltage change with current.

Biasing current for the reference can be anywhere from 0.5 mA to 10 mA with little change in performance. This wide current range allows direct replacement of most zener types with no other circuit changes besides the temperature stabilizer connection. Since the dynamic impedance is constant with current changes regulation is better than discrete zeners. For optimum regulation, lower operating currents are preferred since the ratio of source resistance to zener impedance is higher, and the attenuation of input changes is greater. Further, at low currents, the voltage drop in the wiring is minimized.

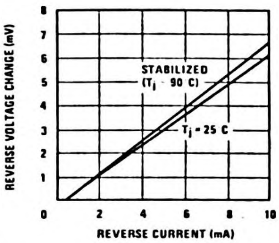


FIGURE 9. The LM199 Shows Excellent Regulation Against Current Changes

Mounting is an important consideration for optimum performance. Although the thermal shield minimizes the heat low, the LM199 should not be exposed to a direct air flow such as from a cooling fan. This can cause as much as a 100% increase in power dissipation degrading the thermal regulation and increasing the drift. Normal conviction currents do not degrade performance.

Printed circuit board layout is also important. Firstly, four wire sensing should be used to eliminate ohmic drops in pc traces. Although the voltage drops are small the temperature coefficient of the voltage developed along a copper trace can add significantly to the drift. For example, a trace with 1Ω resistance and 2 mA current flow will develop 2 mV drop. The TC of copper is 0.004%/°C so the 2 mV drop will change at 8μV/°C, this is an additional 1 ppm drift error. Of course, the effects of voltage drops in the printed circuit traces are eliminated with 4-wire operation. The heater current also should not be allowed to flow through the voltage reference traces. Over a –55°C to +125°C temperature

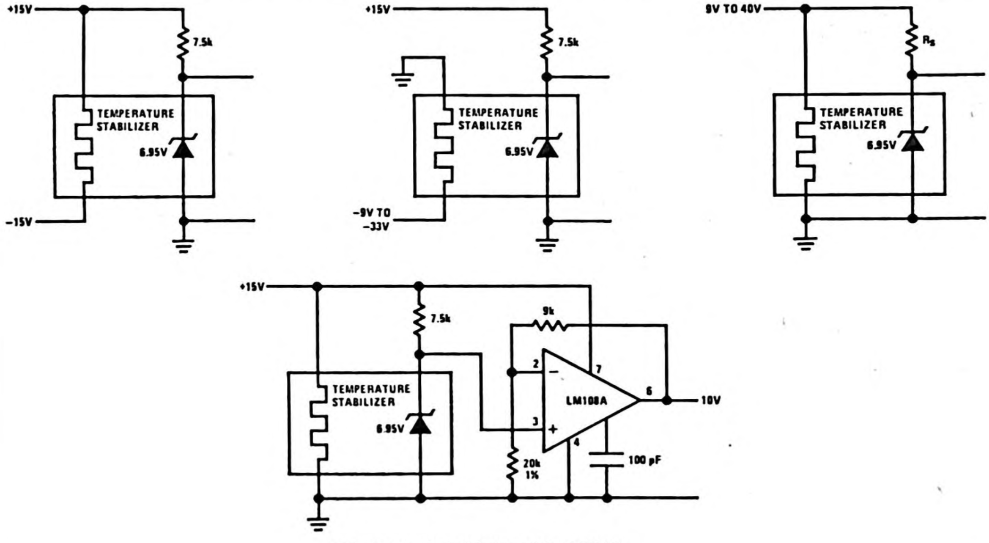


FIGURE 8. Basic Biasing of the LM199

range the heater current will change from about 1 mA to over 40 mA. These magnitudes of current flowing reference leads or reference ground can cause huge errors compared to the drift of the LM199.

Thermocouple effects can also cause errors. The kovar leads from the LM199 package form a thermocouple with copper printed circuit board traces. Since the package of the 199 is heated, there is a heat flow along the leads of the LM199 package. If the leads terminate into unequal sizes of copper on the p.c. board greater heat will be absorbed by the larger copper trace and a temperature difference will develop. A temperature *difference* of 1°C between the two leads of the reference will generate about 30μV. Therefore, the copper traces to the zener should be equal in size. This will generally keep the errors due to thermocouple effects under about 15μV.

The LM199 should be mounted flush on the p.c. board with a minimum of space between the thermal shield and the boards. This minimizes air flow across the kovar leads on the board surface which also can cause thermocouple voltages. Air currents across the leads usually appear as ultra-low frequency noise of about 10μV to 20μV amplitude.

It is usually necessary to scale and buffer the output of any reference to some calibrated voltage. *Figure 10* shows a simple buffered reference with a 10V output. The reference is applied to the non-inverting input of the LM108A. An RC rolloff can be inserted in series with the input to the LM108A to roll-off the high frequency noise. The zener heater and op amp are all powered from a single 15V supply. About 1% regulation on the input supply is adequate contributing less than 10μV of error to the output. Feedback resistors around the LM308 scale the output to 10V.

Although the absolute values of the resistors are not extremely important, tracking of temperature coefficients is vital. The 1 ppm/°C drift of the LM199 is easily exceeded by the temperature coefficient of most resistors. Tracking to better than 1 ppm is also not easy to obtain. Wirewound types made of Evenohm or Mangamin are good and also have low thermoelectric effects. Film types such as Vishay resistors are also good. Most potentiometers do not track fixed resistors so it is a good idea to minimize the adjustment range and therefore minimize their effects on the output TC. Overall temperature coefficient of the circuit shown in *Figure 10* is worst case 3 ppm/°C. About 1 ppm is due to the reference, 1 ppm due to the resistors and 1 ppm due to the op amp.

Figure 11 shows a standard cell replacement with a 1.01V output. A LM321 and LM308 are used to minimize op amp drift to less than 1μV/°C. Note the adjustment connection which minimizes the TC effects of the pot. Set-up for this circuit requires nulling the offset of the op amp first and then adjusting for proper output voltage.

The drift of the LM321 is very predictable and can be used to eliminate overall drift of the system. The drift changes at 3.6μV/°C per millivolt of offset so 1 mV to 2 mV of offset can be introduced to minimize the overall TC.

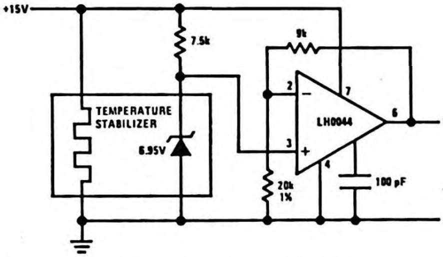


FIGURE 10. Buffered 10V Reference

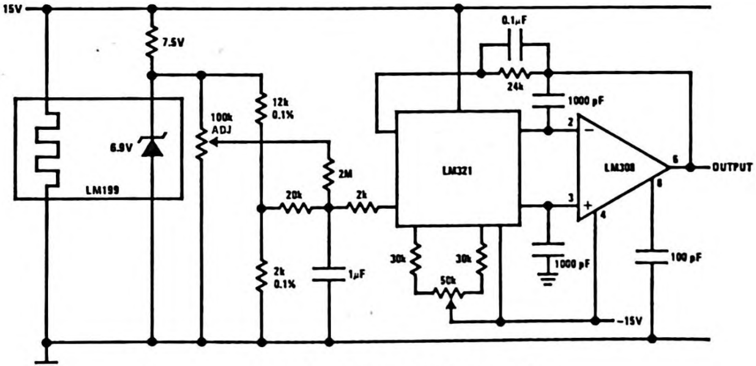


FIGURE 11. Standard Cell Replacement

For circuits with a wide input voltage range, the reference can be powered from the output of the buffer as is shown in *Figure 12.* The op amp supplies regulated voltage to the resistor biasing the reference minimizing changes due to input variation. There is some change due to variation of the temperature stabilizer voltage so extremely wide range operation is not recommended for highest precision. An additional resistor (shown 80 kΩ) is added to the unregulated input to insure the circuit starts up properly at the application of power.

A precision power supply is shown in *Figure 13.* The output of the op amp is buffered by an IC power transistor the LM395. The LM395 operates as an NPN power device but requires only 5μA base current. Full overload protection inherent in the LM395 includes current limit, safe-area protection, and thermal limit.

A reference which can supply either a positive or a negative continuously variable output is shown in *Figure 14.* The reference is biased from the ±15V input supplies as was shown earlier. A ten-turn pot will adjust the output from $+V_Z$ to $-V_Z$ continuously. For negative output the op amp operates as an inverter while for positive outputs it operates as a non-inverting connection.

Op amp choice is important for this circuit. A low drift device such as the LM108A or a LM108-LM121 combination will provide excellent performance. The pot should be a precision wire wound 10 turn type. It should be noted that the output of this circuit is not linear.

CONCLUSIONS

A new monolithic reference which exceeds the performance of conventional zeners has been developed. In fact, the LM199 performance is limited more by external components than by reference drift itself. Further, many of the problems associated with conventional zeners such as hysteresis, stress sensitivity and temperature gradient sensitivity have also been eliminated. Finally, long-term stability and noise are equal of the drift performance of the new device.

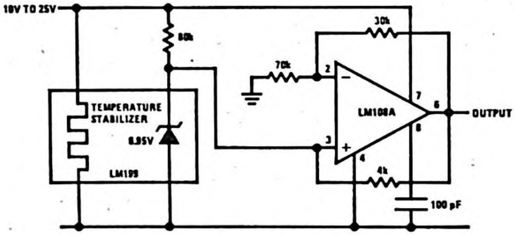

18V TO 25V
80k
30k
70k
TEMPERATURE STABILIZER
6.95V
LM199
2
3
7
6
8
4
LM108A
OUTPUT
4k
100 pF

FIGURE 12. Wide Range Input Voltage Reference

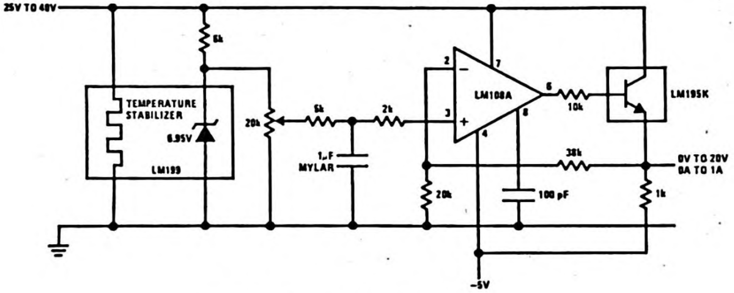

25V TO 40V
5k
TEMPERATURE STABILIZER
6.95V
LM199
20k
5k
2k
1μF MYLAR
2
3
7
6
8
4
LM108A
10k
LM195K
38k
0V TO 20V
0A TO 1A
20k
100 pF
1k
-5V

FIGURE 13. Precision Power Supply

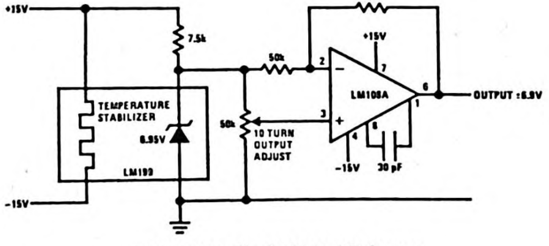

+15V
7.5k
50k
50k
+15V
2
3
7
6
1
8
4
LM108A
OUTPUT ±6.9V
TEMPERATURE STABILIZER
6.95V
LM199
50k
10 TURN OUTPUT ADJUST
-15V
30 pF
-15V

FIGURE 14. Bipolar Output Reference

LM2907 Tachometer/ Speed Switch Building Block Applications

National Semiconductor
Application Note 162
Dave Long
June 1976

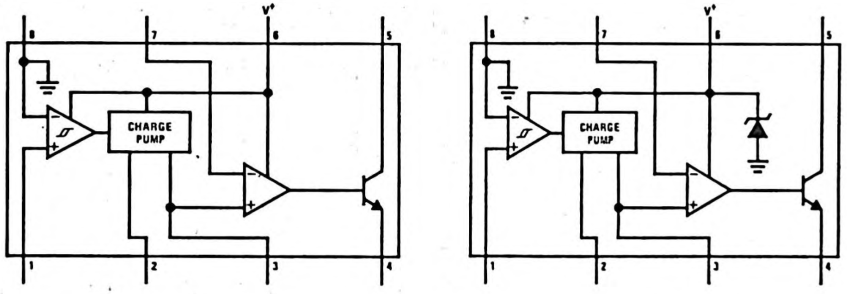
INTRODUCTION

Frequency to voltage converters are available in a number of forms from a number of sources, but invariably require significant additional components before they can be put to use in a given situation. The LM2907, LM2917 series of devices was developed to overcome these objections. Both input and output interface circuitry is included on chip so that a minimum number of additional components is required to complete the function. In keeping with the systems building block concept, these devices provide an output voltage which is proportional to input frequency and provide zero output at zero frequency. In addition, the input may be referred to ground. The devices are designed to operate from a single supply voltage, which makes them particularly suitable for battery operation.

PART I — GENERAL OPERATION PRINCIPLES

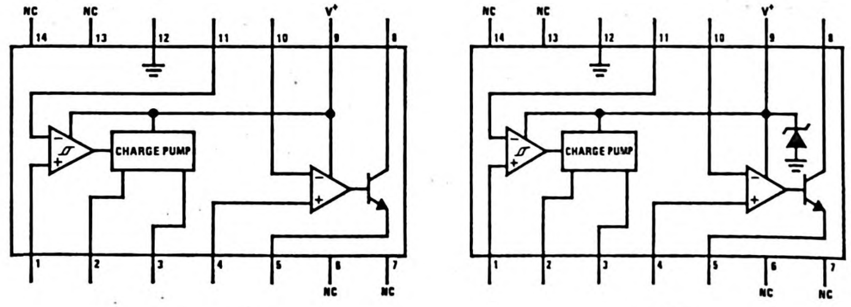
Circuit Description

Referring to *Figure 1,* the family of devices all include three basic components: an input amplifier with built-in hysteresis; a charge pump frequency to voltage converter; and a versatile op amp/comparator with an uncommitted output transistor. LM2917 incorporates an active zener regulator on-chip. LM2907 deletes this option. Both versions are obtainable in 14-pin and in 8-pin dual-in-line molded packages, and to special order in other packages.



LM2907N-8

LM2917N-8



LM2907N

LM2917N

FIGURE 1. Block Diagrams

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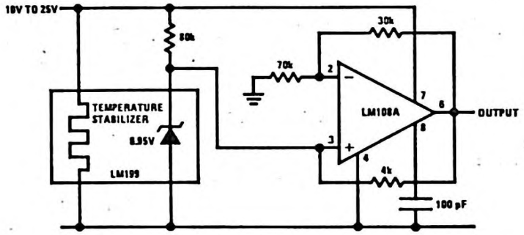
18V TO 25V
80k
30k
70k
2
7
6
LM108A
OUTPUT
3
8
4
4k
100 pF
TEMPERATURE STABILIZER
6.95V
LM199

FIGURE 12. Wide Range Input Voltage Reference

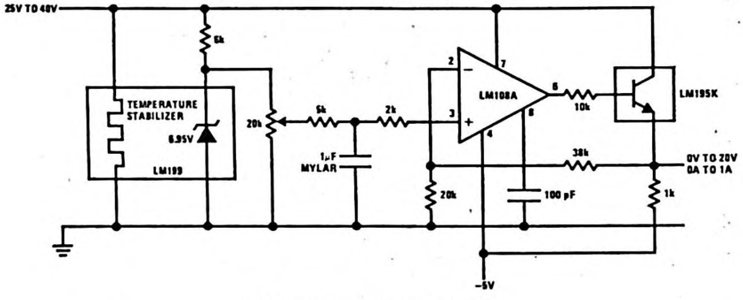
25V TO 40V
5k
TEMPERATURE STABILIZER
6.95V
LM199
20k
5k
2k
1μF
MYLAR
2
7
LM108A
6
10k
LM195K
3
8
4
38k
0V TO 20V
0A TO 1A
20k
100 pF
1k
−5V

FIGURE 13. Precision Power Supply

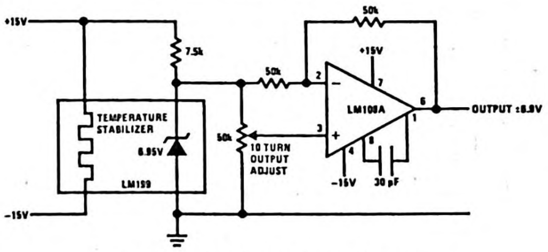
+15V
7.5k
50k
+15V
50k
2
7
LM108A
6
OUTPUT ±6.9V
1
3
50k
10 TURN
OUTPUT
ADJUST
4
8
−15V
30 pF
TEMPERATURE STABILIZER
6.95V
LM199
−15V

FIGURE 14. Bipolar Output Reference

LM2907 Tachometer/ Speed Switch Building Block Applications

National Semiconductor
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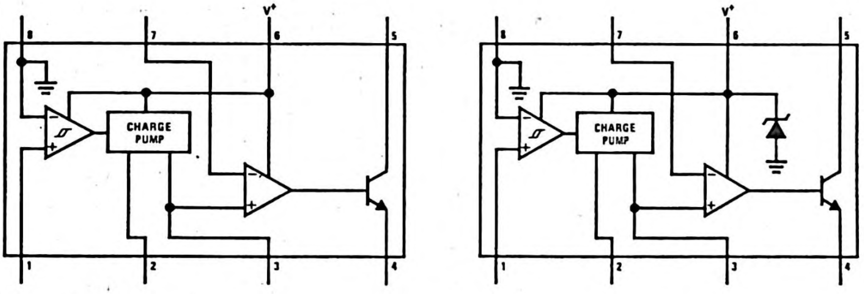
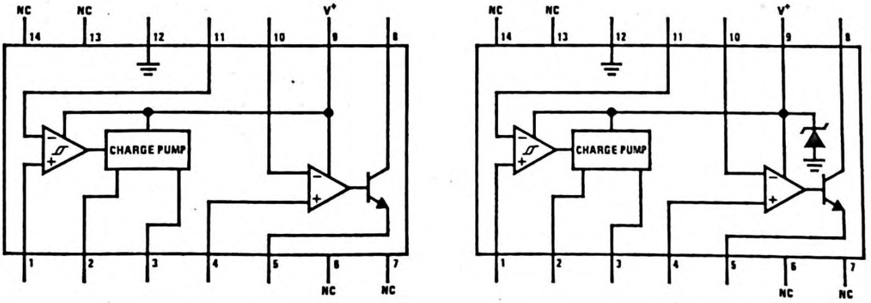


LM2907N-8

LM2917N-8



LM2907N

LM2917N

FIGURE 1. Block Diagrams

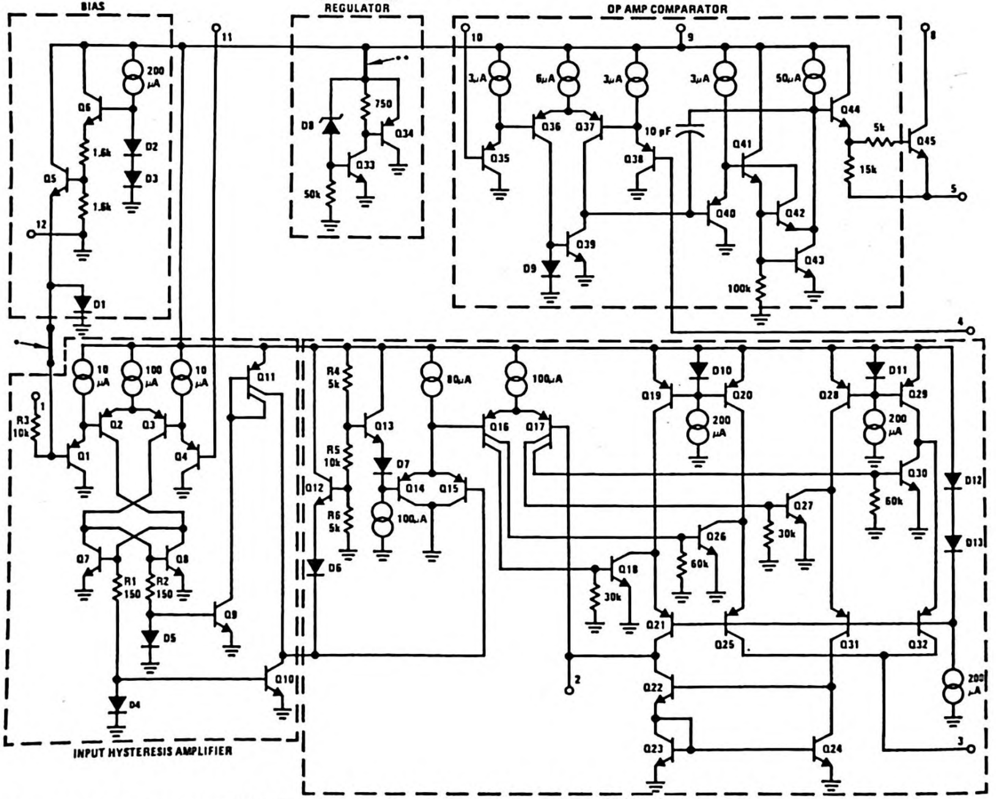
AN162-1

Input Hysteresis Amplifier

The equivalent schematic diagram is shown in *Figure 2.* Q1 through Q11 comprise the input hysteresis amplifier. Q1 through Q4 comprise an input differential amplifier which, by virtue of PNP level shifting, enables the circuit to operate with signals referenced to ground. Q7, Q8, D4, and D5 comprise an active load with positive feedback. This load behaves as a bi-stable flip-flop which may be set or reset depending upon the currents supplied from Q2 and Q3. Consider the situation where Q2 and Q3 are conducting equally, i.e. the input differential voltage is zero. Assuming Q7 to be conducting, it will be noted that the current from Q3 will be drawn by Q7 and Q8 will be in the "OFF" state. This allows the current from Q2 to drive Q7 in parallel with D4 and a small resistor. D4 and Q7 are identical geometry devices, so that the resistor causes Q7 to be biased at a higher level than D4. Thus Q7 will be able to conduct more current than Q3 provides. In order to reverse the state of Q7 and Q8, it will be necessary to reduce the current from Q2 below that provided by Q3 by an amount which is established by R1. It can be shown that this requires a differential input to Q1 and Q4, of approximately 15 mV. Since the circuit is symmetrical, the threshold voltage to reverse the state is 15 mV in the other direction. Thus the input amplifier has built-in hysteresis at ±15 mV. This provides clean switching where noise may be present on the input signal, and allows total rejection of noise below this amplitude where there is no input signal.

Charge Pump

The charge pump is composed of Q12 through Q32. R4, R5, and R6 provide reference voltages equal to 1/4 and 3/4 of supply voltage to Q12 and Q13. When Q10 turns "ON" or "OFF," the base voltage at Q16 changes by an amount equal to the voltage across R5, that is 1/2 V_{CC}. A capacitor connected between Pin 2 and ground is either charged by Q21 or discharged by Q22 until its voltage matches that on the base of Q16. When the voltage on Q16 base goes low, Q16 turns "ON," which results in Q18 and Q26 turning on, which causes the current, sourced by Q19 and Q20, to be shunted to ground. Thus Q21 is unable to charge pin 2. Meanwhile, Q27 and Q30 are turned off permitting the $200\mu A$ sourced by Q28 and Q29 to enter the emitters of Q31 and Q32 respectively. The current from Q31 is mirrored by Q22 through Q24 resulting in a $200\mu A$ discharge current through pin 2. The external capacitor on pin 2 is thus


BIAS
ACTIVE ZENER REGULATOR
OP AMP COMPARATOR
INPUT HYSTERESIS AMPLIFIER
CHARGE PUMP
11
10
9
8
12
5
4
1
2
3
200 µA
100 µA
10 µA
80µA
100µA
50µA
3µA
6µA
10 pF
1.6k
750
50k
5k
15k
100k
R1 150
R2 150
R3 10k
R4 5k
R5 10k
R6 5k
60k
30k
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
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Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q42
Q43
Q44
Q45
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13

•Note: This connection made on LM2907-8 and LM2917-8 only.

••Note: This connection made on LM2917 and LM2917-8 only.

Note: Pin numbers refer to 14-pin package.

FIGURE 2. Equivalent Schematic Diagram

discharged at a constant rate until it reaches the new base voltage on Q16. The time taken for this discharge to occur is given by:

$$t = \frac{CV}{I} \tag{1}$$

where C = capacitor on pin 2
V = change in voltage on Q16 base
I = current in Q22

During this time, Q32 sources an identical current into pin 3. A capacitor connected to pin 3 will thus be charged by the same current for the same amount of time as pin 2. When the base voltage on Q16 goes high, Q18 and Q26 are turned off while Q27 and Q3 are turned "ON." In these conditions, Q21 and Q25 provide the currents to charge the capacitors on pins 2 and 3 respectively. Thus the charge required to return the capacitor on pin 2 to the high level voltage is duplicated and used to charge the capacitor connected to pin 3. Thus in one cycle of input the capacitor on pin 3 gets charged twice with a charge of CV.

Thus the total charge pumped into the capacitor on pin 3 per cycle is:

$$Q = 2\,CV \tag{2}$$

Now, since $V = V_{CC}/2$

then
$$Q = CV_{CC} \tag{3}$$

A resistor connected between pin 3 and ground causes a discharge of the capacitor on pin 3, where the total charge drained per cycle of input signal is equal to:

$$Q1 = \frac{V3\,.\,T}{R}$$

where V3 = the average voltage on pin 3
T = period of input signal
R = resistor connected to pin 3

In equilibrium Q = Q1

$$\text{i.e., } CV_{CC} = \frac{V3\,.\,T}{R} \tag{4}$$

and
$$V3 = V_{CC} \cdot \frac{RC}{T} \tag{5}$$

or
$$V3 = V_{CC} \cdot R \cdot C \cdot f \tag{6}$$

where f = input frequency

Op Amp/Comparator

Again referring to *Figure 2*, the op amp/comparator includes Q35 through Q45. A PNP input stage again provides input common-mode voltages down to zero, and if pin 8 is connected to V_{CC} and the output taken from pin 5, the circuit behaves as a conventional, unity-gain-compensated operational amplifier. However, by allowing alternate connections of Q45 the circuit may be used as a comparator in which loads to either V_{CC} or ground may be switched. Q45 is capable of sinking 50 mA. Input bias current is typically 50 nA, and voltage gain is typically 200V/mV. Unity gain slew rate is 0.2V/μs. When operated as a comparator Q45 emitter will switch at the slew rate, or the collector of Q45 will switch at that rate multiplied by the voltage gain of Q45, which is user selectable.

Active Zener Regulator

The optional active zener regulator is also shown in *Figure 2.* D8 provides the voltage reference in conjunction with Q33. As the supply voltage rises, D8 conducts and the base voltage on Q33 starts to rise. When Q33 has sufficient base voltage to be turned "ON," it in turn causes Q34 to conduct current from the power source. This reduces the current available for D8 and the negative feedback loop is thereby completed. The reference voltage is therefore the zener voltage on D8 plus the emitter base voltage of Q33. This results in a low temperature coefficient reference voltage.

Input Levels and Protection

In 8-pin versions of the LM2907, LM2917, the non-inverting input of the op amp/comparator is connected to the output of the charge pump. Also, one input to the input hysteresis amplifier is connected to ground. The other input (pin 1) is then protected from transients by, first a 10 kΩ series resistor, R3 *(Figure 2)* which is located in a floating isolation pocket, and secondly by clamp diode D1. Since the voltage swing on the base of Q1 is thus restricted, the only restriction on the allowable voltage on pin 1 is the breakdown voltage of the 10 kΩ resistor. This allows input swings to ±28V. In 14-pin versions the link to D1 is opened in order to allow the base of Q1 to be biased at some higher voltage.

Q5 clamps the negative swing on the base of Q1 to about 300 mV. This prevents substrate injection in the region of Q1 which might otherwise cause false switching or erroneous discharge of one of the timing capacitors.

The differential input options (LM2907-14, LM2917-14), give the user the option of setting his own input switching level and still having the hysteresis around that level for excellent noise rejection in any application.

HOW TO USE IT

Basic f to V Converter

The operation of the LM2907, LM2917 series is best understood by observing the basic converter shown in *Figure 3.* In this configuration, a frequency signal is applied to the input of the charge pump at pin 1. The voltage appearing at pin 2 will swing between two values which are approximately 1/4 $(V_{CC}) - V_{BE}$ and 3/4 $(V_{CC}) - V_{BE}$. The voltage at pin 3 will have a value equal to $V_{CC} \cdot f_{IN} \cdot C1 \cdot R1 \cdot K$, where K is the gain constant (normally 1.0).

The emitter output (pin 4) is connected to the inverting input of the op amp so that pin 4 will follow pin 3 and provide a low impedance output voltage proportional to input frequency. The linearity of this voltage is typically better than 0.3% of full scale.

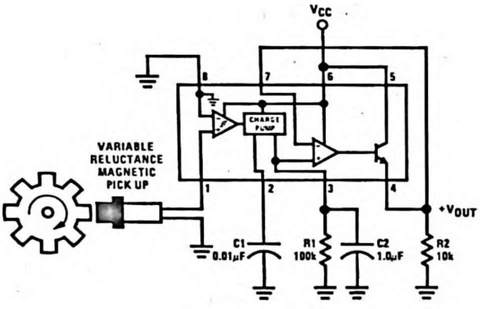


FIGURE 3. Basic f to V Converter

Choosing R1, C1 and C2

There are some limitations on the choice of R1, C1 and C2 *(Figure 3)* which should be considered for optimum performance. C1 also provides internal compensation for the charge pump and should be kept larger than 100 pF. Smaller values can cause an error current on R1, especially at low temperatures. Three considerations must be met when choosing R1.

First, the output current at pin 3 is internally fixed and therefore V3 max, divided by R1, must be less than or equal to this value.

$$\therefore \quad R1 \geq \frac{V3\ \text{max}}{I_{3MIN}}$$

where V3 max is the full scale output voltage required
I_{3MIN} is determined from the data sheet (150µA)

Second, if R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Finally, ripple voltage must be considered, and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1, C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \cdot \frac{C1}{C2} \left(1 - \frac{V_{CC} \cdot f_{IN} \cdot C1}{I_2}\right) \text{p-p}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new frequency increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully. R1 should be selected according to the following relationship:

C1 is selected according to:

$$C1 = \frac{V3\ \text{Full Scale}}{R1 \cdot V_{CC} \cdot f_{FULL\ SCALE}}$$

Next decide on the maximum ripple which can be accepted and plug into the following equation to determine C2:

$$C2 = \frac{V_{CC}}{2} \cdot \frac{C1}{V_{RIPPLE}} \left(1 - \frac{V_3}{2}\right)$$

The kind of capacitor used for timing capacitor C1 will determine the accuracy of the unit over the temperature range. *Figure 15* illustrates the tachometer output as a function of temperature for the two devices. Note that the LM2907 operating from a fixed external supply has a negative temperature coefficient which enables the device to be used with capacitors which have a positive temperature coefficient and thus obtain overall stability. In the case of the LM2917 the internal zener supply voltage has a positive coefficient which causes the overall tachometer output to have a very low temperature coefficient and requires that the capacitor temperature coefficient be balanced by the temperature coefficient of R1.

Using Zener Regulated Options (LM2917)

For those applications where an output voltage or current must be obtained independently of the supply voltage variations, the LM2917 is offered. The reference typically has an 11Ω source resistance. In choosing a dropping resistor from the unregulated supply to the device note that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages, there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize these zener voltage variations to 160 mV. If the resistor goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation. Take care also that the power dissipation of the IC is not exceeded at higher supply voltages. *Figure 4* shows suitable dropping resistor values.

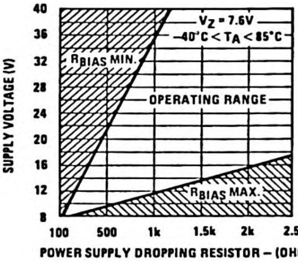


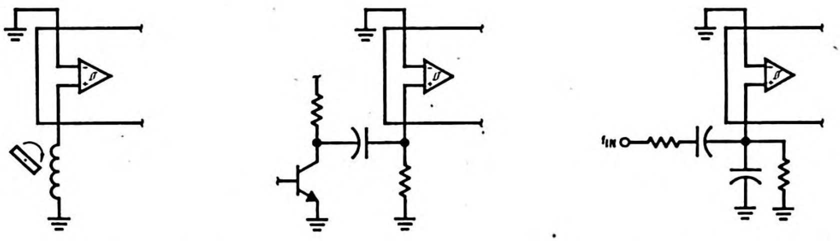
FIGURE 4. Zener Regular Bias Resistor Range

Input Interface Circuits

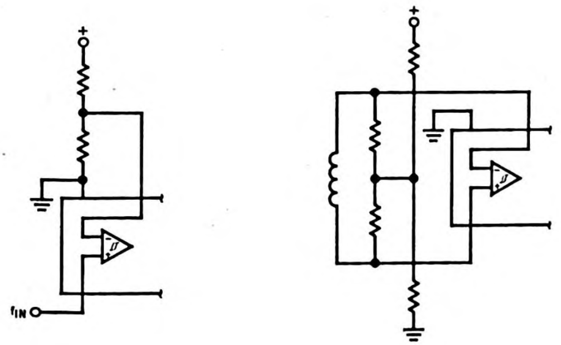
The ground referenced input capability of the LM2907-8 allows direct coupling to transformer inputs, or variable reluctance pickups. *Figure 5(a)* illustrates this connection. In many cases, the frequency signal must be obtained from another circuit whose output may not go below ground. This may be remedied by using ac coupling to the input of the LM2907 as illustrated in *Figure 5(b)*. This approach is very suitable for use with phototransistors for optical pickups. Noisy signal sources may be coupled as shown in *Figure 5*(c). The signal is bandpass filtered. This can be used, for example, for tachometers operating from breakerpoints on a conventional Kettering ignition system. Remember that the minimum input signal required by the LM2907 is only 30 mVp-p, but this signal must be able to swing at least 15 mV on either side of the inverting input. The maximum signal which can be applied to the LM2907 input, is ±28V. The input bias current is a typically 100 nA. A path to ground must be provided for this current through the source or by other means as illustrated. With 14-pin package versions of LM2907, LM2917, it is possible to bias the inverting input to the tachometer as illustrated in *Figure 5(d)*. This enables the circuit to operate with input signals that do not go to ground, but are referenced at higher voltages. Alternatively, this method increases the noise immunity where large signal levels are available but large noise signals on ground are also present. To take full advantage of the common-mode rejection of the input differential stage, a balanced bias configuration must be provided. One such circuit is illustrated in *Figure 5(e)*. With this arrangement, the effective common-mode rejection may be virtually infinite, owing to the input hysteresis.

Output Configurations

LM2907, LM2917 series devices incorporate an unusually flexible op amp/comparator device on-chip for interfacing with a wide variety of loads. This flexibility results from the availability of both the collector and emitter of the output transistor which is capable of driving up to 50 mA of load current. When the non-inverting input is higher than the inverting input, this output transistor is turned "ON." It may be used to drive loads to either the positive or the negative supply with the emitter or collector respectively connected to the other supply. For example, *Figure 6(a)*, a simple speed switch can be constructed in which the speed signal derived from the frequency to voltage converter is compared to a reference derived simply by a resistive divider from the power supply. When the speed signal exceeds the reference, the output transistor turns on the light emitting diode in the load. A small current limiting resistor should be placed in series with the output to protect the LED and the output transistor.

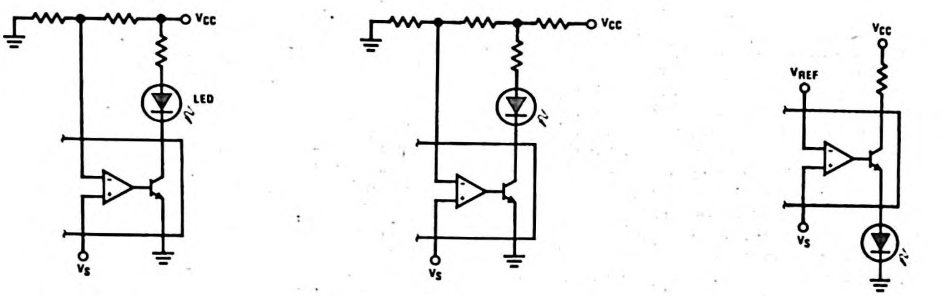


(a) Ground Referenced Inputs **(b) AC Coupled Input** **(c) Bandpass Filtered Input Reduces Noise**

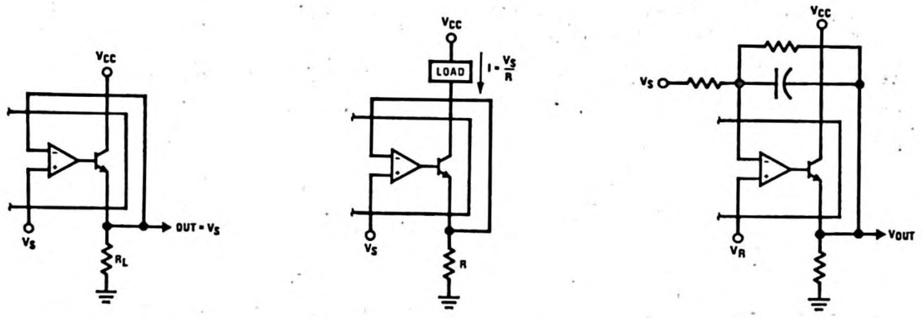


(d) Above Ground Sensing **(e) High Common-Mode Rejection Input Circuit**

FIGURE 5. Tachometer Input Configurations



(a) Switching an LED (b) Adding Hysteresis to LED Switch (c) Switching a Grounded Load



(d) Voltage Follower (e) Voltage to Current Converter (f) Integrator

FIGURE 6. Output Configurations

This circuit has no hysteresis in it, i.e., the turn "ON" and turn "OFF" speed voltages are essentially equal. In cases where speed may be fluctuating at a high rate and a flashing LED would be objectionable, it is possible to incorporate hysteresis so that the switch-on speed is above the switch-off speed by a controlled amount. Such a configuration is illustrated in *Figure 6(b)*. *Figure 6(c)* shows how a grounded load can also be switched by the circuit. In this case, the current limiting resistor is placed in the collector of the power transistor. The base current of the output transistor (Q45) is limited by a 5 kΩ base resistor (see *Figure 2*). This raises the output resistance so that the output swing will be reduced at full load.

The op amp/comparator is internally compensated for unity gain feedback configurations as in *Figure 6(d)*. By directly connecting the emitter output to the non-inverting input, the op amp may be operated as a voltage follower. Note that a load resistor is required externally. The op amp can also be operated, of course, as an amplifier, integrator, active filter, or in any other normal operational amplifier configuration.

One unique configuration which is not available with standard operational amplifiers, is shown in *Figure 6(e)*. Here the collector of the output transistor is used to drive a load with a current which is proportional to the input voltage. In other words, the circuit is operating as a voltage to current converter. This is ideal for driving remote signal sensors and moving coil galvanometers. *Figure 6(f)* shows how an active integrator can be used to provide an output which falls with increasing speed.

These are the basic configurations obtainable with the op amp/comparator. Further combinations can be seen in the applications shown in Part II of this application note.

Transient Protection

Many application areas use unregulated power supplies which tend to expose the electronics to potentially damaging transients on the power supply line. This is particularly true in the case of automotive applications where two such transients are common.[1] First is the load dump transient. This occurs when a dead battery is being charged at a high current and the battery cable comes loose, so that the current in the alternator inductance produces a positive transient on the line in the order of 60V to 120V. The second transient is called field decay. This occurs when the ignition is turned "OFF" and the energy stored in the field winding of the alternator causes a negative 75V transient on the ignition line.

Figure 7 illustrates methods for protecting against these and other transients. *Figure 7(a)* shows a typical situation in which the power supply to the LM2907 can be provided through a dropping resistor and regulated by an external zener diode Z1, but the output drive is required to operate from the full available supply voltage. In this case, a separate protection zener Z2 must be provided if the voltage on the power supply line is expected to exceed the maximum rated voltage of the LM2907.

In *Figure 7(b)* and *7(c)*, the output transistor is required only to drive a simple resistive load and no secondary protection circuits are required. (Note that the dropping resistor to the zener also has to supply current to the output circuit). With the foregoing circuits, reverse supply protection is supplied by the forward biased zener diode. This device should be a low forward resistance unit in order to limit the maximum reverse voltage applied to the integrated circuit. Excessive reverse voltage on the IC can cause high currents to be conducted by the substrate diodes with consequent danger of permanent damage. Up to 1V negative can generally be tolerated. Versions with internal zeners may be self-protecting depending on the size of dropping resistor used. In applications where large negative voltage transients may be anticipated, a blocking diode may be connected in the power supply line to the IC as illustrated in *Figure 7(d)*. During these negative transients, the diode D1 will be reverse biased and prevent reverse currents flowing in the IC. If these transients are short and the capacitor C1 is large enough, then the power to the IC can be sustained. This is useful to prevent change of state or change of charge in systems connected to it.

Temperature Ranges and Packaging Considerations

The LM2907, LM2917 series devices are specified for operation over the temperature range −40°C to +85°C.

The devices are normally packaged in molded epoxy, dual-in-line packages. Other temperature ranges and other packages are available to special order. For reliability requirements beyond those of normal commercial application where the cost of military qualification is not bearable, other programs are available such as B+.

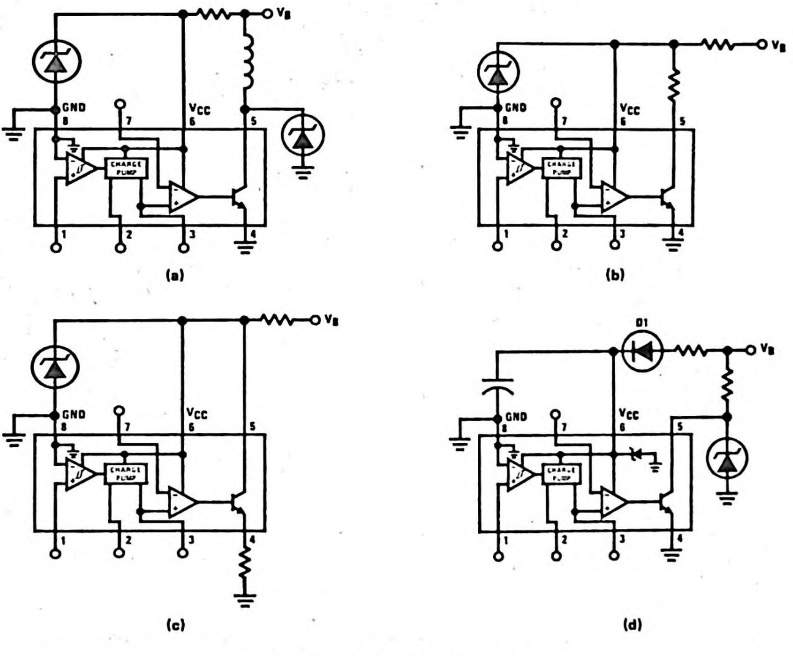
PART II – APPLICATIONS

INTRODUCTION

The LM2907, LM2917 series devices were designed not only to perform the basic frequency to voltage function required in many systems, but also to provide the input and output interface so often needed, so that low cost implementations of complete functions are available.

The concept of building blocks requires that a function be performed in the same way as it can be mathematically defined. In other words, a frequency to voltage converter will provide an output voltage proportional to frequency which is independent of the input voltage or other input parameters, except the frequency. In the same way, the output voltage will be zero when the input frequency is zero. These features are built into the LM2907.

Applications for the device range from simple speed switch for anti-pollution control device functions in automobiles, to motor speed controls in industrial



(a) (b) (c) (d)

FIGURE 7. Transient Protection Schemes

applications. The applications circuits which follow are designed to illustrate some of the capabilities of the LM2907. In most cases, alternative input or output configurations can be mixed and matched at will and other variations can be determined from the description in Part I of this application note. For complete specifications, refer to the data sheet.

Speed Switches

Perhaps the most natural application of the LM2907 is in interfacing with magnetic pickups, such as the one illustrated in *Figure 8* to perform speed switching functions. As an example, New York taxies are required to change the intensity of the warning horn above and below 45 mph. Other examples include an over-speed warning, where a driver may set the desired maximum speed and have an audible or visual warning of speeds in excess of that level. Many anti-pollution devices included on several recent automobile models have included a speed switch to disable the vacuum advance function until a certain speed is attained[2]. A circuit which will perform these kind of functions is shown in *Figure 9*. A typical magnetic pickup for automotive applications will provide a thousand pulses per mile so that at 60 mph the incoming frequency will be 16.6 Hz. If the reference level on the comparator is set by two equal resistors R1 and R2 then the desired value of C1 and R1 can be determined from the simple relationship:

$$\frac{V_{CC}}{2} = V_{CC} \cdot C1 \cdot R1 \cdot f.$$

or $$C1R1f = 0.5$$

and hence $$C1R1 = 0.03$$

From the RC selection chart in *Figure 10* we can choose suitable values for R1 and C1. Examples are 100 kΩ and 0.3µF. The circuit will then switch at approximately 60 mph with the stated input frequency relationship to speed. To determine the ripple voltage refer back to the equation for ripple voltage (under "Choosing R1, C1 and C2"). From this we can determine that there will be about 10 mV of ripple at the switching level. To prevent this from causing chattering of the load a certain amount of hysteresis is added by including R3. This will provide typically 1% of supply as a hysteresis or 1.2 mph in the example. Note that since the reference to the comparator is a function of supply voltage as is the output from the charge pump there is no need to regulate the power supply. The frequency at which switching occurs is independent of supply voltage.

In some industrial applications it is useful to have an indication of past speed excesses, for example in notifying the need for checking of bearings. The LM2907 can be made to latch until the power supply is turned "OFF" in the case where the frequency exceeds a certain limit,

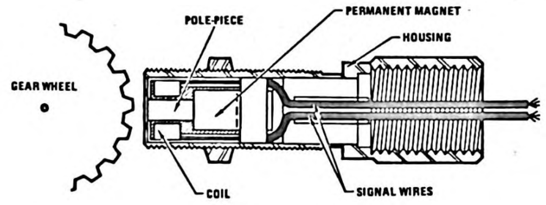


FIGURE 8. Typical Magnetic Pickup

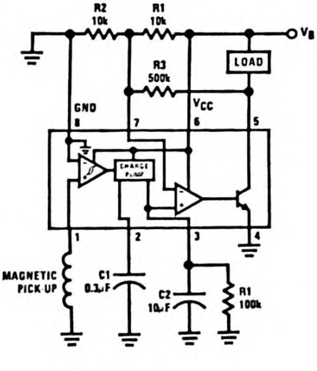


FIGURE 9. Simple Speed Switch Load is Energized when $f_{IN} > \frac{1}{2C1R1}$

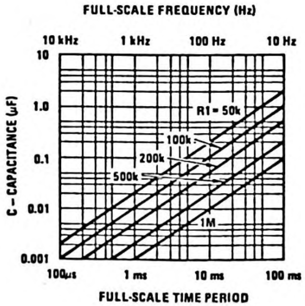
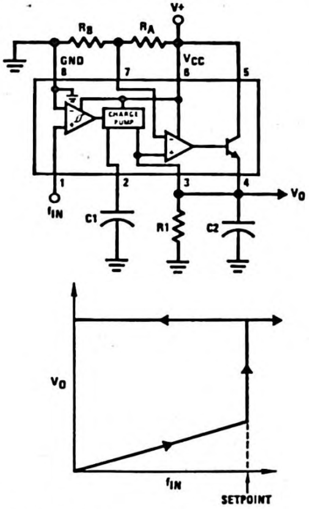


FIGURE 10. RC Selection Chart

by simply connecting the output transistor emitter back to the non-inverting input of the comparator as shown in *Figure 11.* It can also serve to shut off a tape recorder or editing machine at the end of a rewind cycle. When the speed suddenly increases, the device will sense the condition and shut down the motor.



$V_O = F_{IN}\, V+\, R1\, C1$

$\text{SETPOINT} = V+ \dfrac{RB}{RB + RA}$

Latchup occurs when $F_{IN} = \dfrac{RB}{RA + RB}\ \dfrac{1}{R1\, C1}$

Independent of V+!

FIGURE 11. Overspeed Latch

Analog Displays

The LM2907, LM2917 series devices are particularly useful for analog display of frequency inputs. In situations where the display device is a moving coil instrument the advantages of the uncommitted output transistor can be realized by providing a current drive to the meter. This avoids temperature tracking problems with the varying meter resistance and enables high resistance instruments to be driven accurately with relatively large voltages as illustrated in *Figure 12.* The LM2917 version is employed here to provide a regulated current to the instrument. The onboard 7.6V zener is compatible with car and boat batteries and enables the moving coil instrument to employ the full battery voltage for its deflection. This enables high torque meters to be used. This is particularly useful in high vibration environments such as boats and motorcycles. In the case of boats, the most common speed pickup for the knot meter employs a rotating propeller driving a magnetic pickup device. Meteorologists employ a large number of anemometers for measuring wind velocities and these are frequently coupled by a magnetic pickup. In examples like these, where there is frequently a large distance between the display device and the sensor, the configuration of *Figure 13* can be usefully employed to cut down on the number of wires needed. Here the output current is conducted along the supply line so that a local current sensing device in the supply line can be used to get a direct reading of the frequency at the remote location where the electronics may also be situated. The small zero speed offset due to the device quiescent current may be compensated by offsetting the zero on the display device. This also permits one display device to be shared between several inputs.

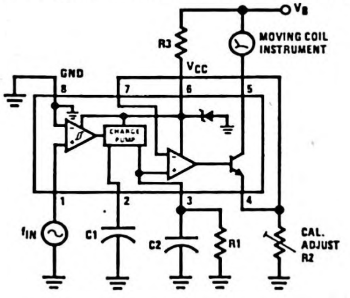


FIGURE 12. Analog Display of Frequency

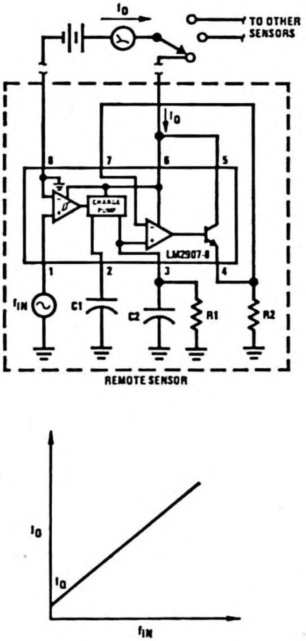


FIGURE 13. Two Wire Remote Speed Sensor

Automotive Tachometer

Not all inputs are derived from variable reluctance magnetic pickups; for example, in spark ignition engines the tachometer is generally driven from the spark coil. An interface circuit for this situation is shown in

Figure 14. This tachometer can be set up for any number of cylinders by linking the appropriate timing resistor as illustrated. A 500Ω trim resistor can be used to set up final calibration. A protection circuit composed of a 10Ω resistor and a zener diode is also shown as a safety precaution against the transients which are to be found in automobiles.

Motor Speed Controls

DC motors with or without brushes can be purchased with ac tachometer outputs already provided by the manufacturer.[3] With these motors in combination with the LM2907, a very low cost speed control can be constructed. In *Figure 16* the most simple version is illustrated where the tachometer drives the non-inverting input of the comparator up towards the preset reference level. When that level is reached, the output is turned off and the power is removed from the motor. As the motor slows down, the voltage from the charge pump output falls and power is restored. Thus speed is maintained by operating the motor in a switching mode. Hysteresis can be provided to control the rate of switching. An alternative approach which gives proportional control is shown in *Figure 17*. Here the charge pump integrator is shown in a feedback connection around the operational amplifier. The output voltage for zero speed is equal to the reference voltage set up on the potentiometer on the non-inverting input. As speed increases,

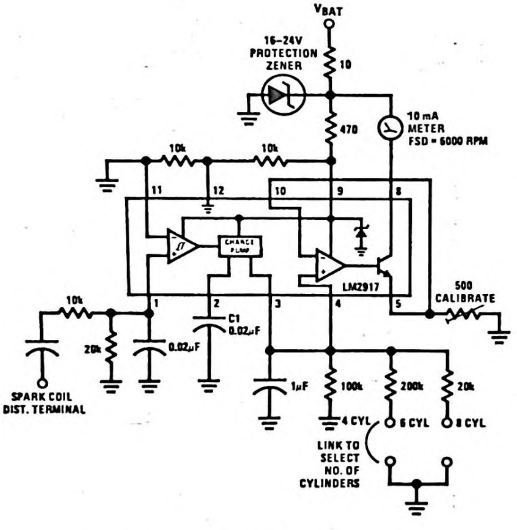

V_BAT
16–24V PROTECTION ZENER
10
470
10 mA METER FSD = 6000 RPM
10k
10k
11
12
10
9
8
CHARGE PUMP
LM2917
1
2
3
4
5
500 CALIBRATE
10k
20k
0.02µF
C1 0.02µF
1µF
100k
200k
20k
4 CYL
6 CYL
8 CYL
LINK TO SELECT NO. OF CYLINDERS
SPARK COIL DIST. TERMINAL

FIGURE 14. Gasoline Engine Tachometer

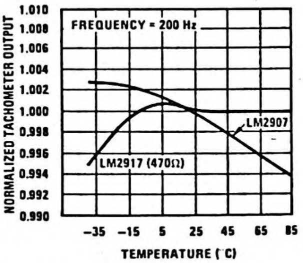


FIGURE 15. Normalized Tachometer Output vs Temperature

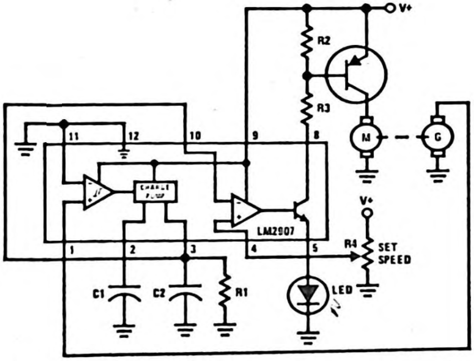

V+
R2
R3
11
12
10
9
8
CHARGE PUMP
LM2907
1
2
3
4
5
M
G
V+
R4
SET SPEED
LED
C1
C2
R1

FIGURE 16. Motor Speed Control

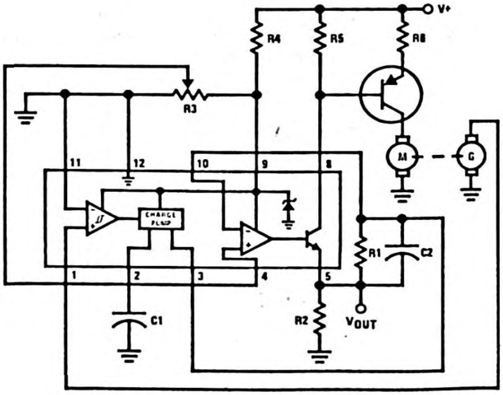

V+
R4
R5
R6
R3
11
12
10
9
8
CHARGE PUMP
M
G
R1
C2
1
2
3
4
5
C1
R2
V_OUT

FIGURE 17. Motor Speed Control with Proportional Drive

the charge pump puts charge into capacitor C2 and causes the output V_{OUT} to fall in proportion to speed. The output current of the op amp transistor is used to provide an analog drive to the motor. Thus as the motor speed approaches the reference level, the current is proportionately reduced to the motor so that the motor gradually comes up to speed and is maintained without operating the motor in a switching mode. This is particularly useful in situations where the electrical noise generated by the switching mode operation is objectionable. This circuit has one primary disadvantage in that it has poor load regulation. A third configuration is shown in *Figure 18.* This employs an LM2907-8 acting as a shunt mode regulator. It also features an LED to indicate when the device is in regulation.

Position Sensing

In addition to their use to complete tachometer feedback loops, used in position transducer circuits, the LM2907, LM2917 devices can also be used as position transducers. For example, the timing resistor can be removed from pin 3 so that the output current produces a staircase instead of a fixed dc level. If the magnetic pickup senses passing notches or items, a staircase signal is generated which can then be compared with a reference to initiate a switching action when a specified count is reached. For example, *Figure 19* shows a circuit which will count up a hundred input pulses and then switch on the output stage. Examples of this application can be found in automated packaging operations or in line printers.

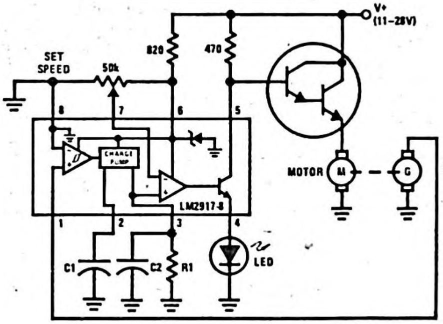


FIGURE 18. Motor Speed Control

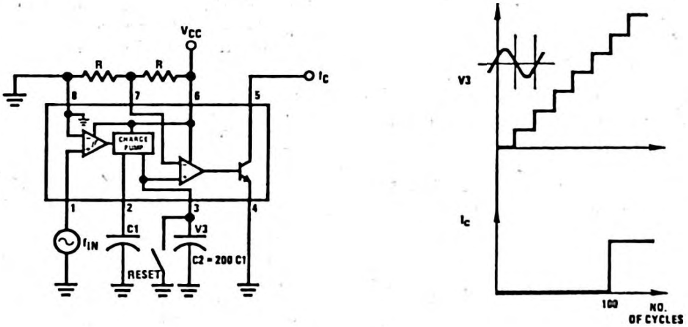


FIGURE 19. Staircase Counter

The output of the tachometer is proportional to the product of supply voltage, input frequency, a capacitor and a resistor. Any one of these may be used as the input variable or they may be used in combination to produce multiplication. An example of a capacitive transducer is illustrated in *Figure 20,* where a fixed input frequency is employed either from the 60 Hz line as a convenient source or from a stable oscillator. The capacitor is a variable element mechanically coupled to the system whose position is to be sensed. The output is proportional to the capacitance value, which can be arranged to have any desired relationship to the mechanical input by suitable shaping of the capacitor electrodes.

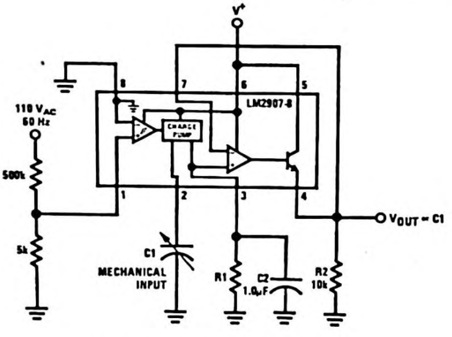


FIGURE 20. Capacitive Transducer

Analog Systems Building Block

The LM2907, LM2917 series characterize systems building block applications by the feature that the output from the device is proportional only to externally programmed inputs. Any or all of these inputs may be controlled inputs to provide the desired output. For example, in *Figure 20* the capacitance transducer can be operated as a multiplier. In flow measurement indicators, the input frequency can be a variable depending on the flow rate, such as a signal generated from a paddle wheel, propeller or vortex sensor[4]. The capacitor can be an indication of orifice size or aperture size, such as in a throttle body. The product of these two will indicate volume flow. A thermistor could be added to R1 to convert the volume flow to mass flow. So a combination of these inputs, including control voltage on the supply, can be used to provide complex multiplicative analog functions with independent control of the variables.

Phase-locked loops (PLL) are popular today now that low cost monolithic implementations are available off the shelf. One of their limitations is the narrow capture range and hold-in range. The LM2907 can be employed as a PLL helper. The configuration is shown in *Figure 21*. The LM2907 here serves the function of a frequency-to-voltage converter which puts the VCO initially at approximately the right frequency to match the input frequency. The phase detector is then used to close the gap between VCO and input frequency by exerting a control on the summing point. In this way, given proper tracking between the frequency-to-voltage converter and the VCO, (which is a voltage-to-frequency converter), a wide-range phase loop can be developed.

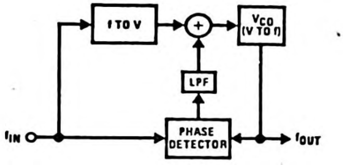


FIGURE 21. Phase-Locked Loop Helper Added f to V Greatly Increases Capture and Hold Range

The linearity of voltage controlled oscillators can be improved by employing the LM2907 as a feedback control element converting the frequency back to voltage and comparing with the input voltage. This can often be a lower cost solution to linearizing the VCO than by working directly on the VCO itself in the open loop mode. The arrangement is illustrated in *Figure 22.*

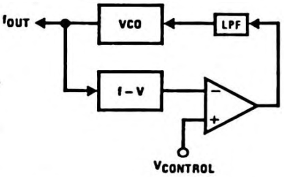
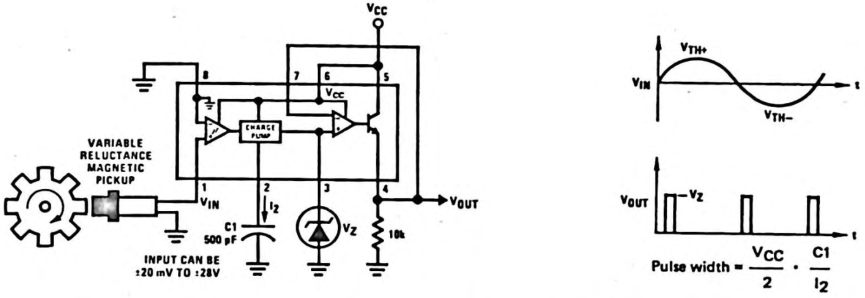


FIGURE 22. Feedback Controlled VCO

Digital Interface

A growing proportion of the complex control systems today are being controlled by microprocessors and other digital devices. Frequently they require inputs to indicate position or time from some mechanical input. The LM2907 can be used to provide zero crossing datum to a digital system using the circuits illustrated in *Figure 23.* At each zero crossing of the input signal the charge pump changes the state of capacitor C1 and provides a one-shot pulse into the zener diode at pin 3. The width of this pulse is controlled by the internal current of pin 2 and the size of capacitor C1 as well as by the supply voltage. Since a pulse is generated by each zero crossing of the input signal we call this a "two-shot" instead of a "one-shot" device and this can be used for doubling the frequency that is presented to the microprocessor control system. If frequency doubling is not required and a square wave output is preferred, the circuit of *Figure 24* can be employed. In this case, the output swing is the same as the swing on pin 2 which is a swing of half supply voltage starting at 1 V_{BE} below one quarter of supply and going to 1 V_{BE} below three-quarters of supply. This can be increased up to the full output swing capability by reducing or removing the negative feedback around the op amp.

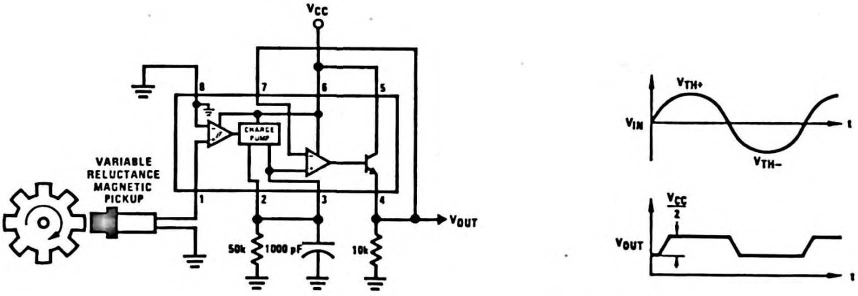
The staircase generator shown in *Figure 19* can be used as an A-D converter. A suitable configuration is shown in *Figure 25.* To start a convert cycle the processor generates a reset pulse to discharge the integrating capacitor C2. Each complete clock cycle generates a charge and discharge cycle on C1. This results in two steps per cycle being added to C2. As the voltage on C2 increases, clock pulses are returned to the processor. When the voltage on C2 steps above the analog input voltage the data line is clamped and C2 ceases to charge. The processor, by counting the number of clock pulses received after the reset pulse, is thus loaded with a digital measure of the input voltage. By making C2/C1 = 1024 an 8-bit A-D is obtained.



VCC
8
7
6
5
VCC
CHARGE PUMP
VARIABLE RELUCTANCE MAGNETIC PICKUP
1
VIN
2
I2
3
4
VOUT
C1 500 pF
VZ
10k
INPUT CAN BE ±20 mV TO ±28V
VTH+
VIN
t
VTH−
VOUT
VZ
t
Pulse width = VCC/2 · C1/I2

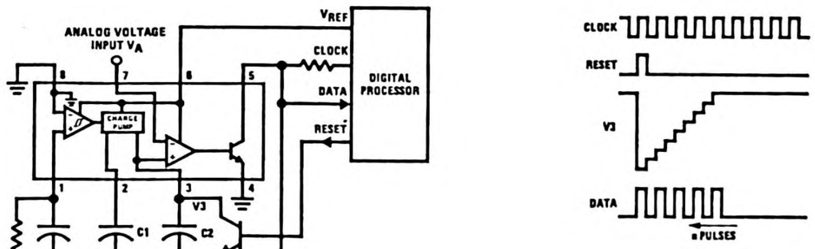
Output frequency equal twice input frequency. Pulse width $= \frac{V_{CC}}{2} \cdot \frac{C1}{I_2}$. Pulse height = V_{ZENER}

FIGURE 23. "Two-Shot" Zero Crossing Detector



VCC
8
7
6
5
CHARGE PUMP
VARIABLE RELUCTANCE MAGNETIC PICKUP
1
2
3
4
VOUT
50k
1000 pF
10k
VTH+
VIN
t
VTH−
VCC/2
VOUT
t

FIGURE 24. Zero Crossing Detector and Line Drivers



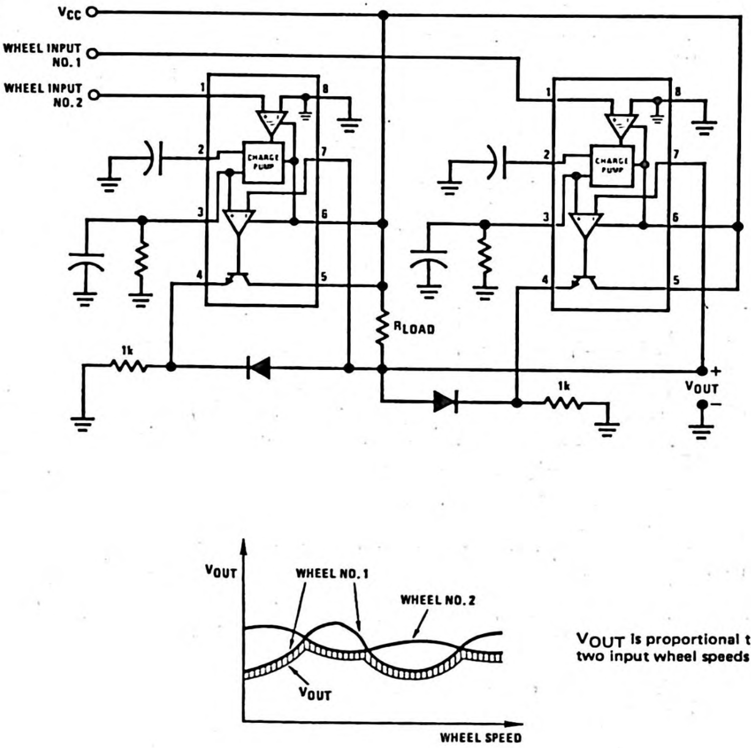
ANALOG VOLTAGE INPUT VA
VREF
CLOCK
DATA
RESET
DIGITAL PROCESSOR
8
7
6
5
CHARGE PUMP
1
2
3
4
V3
C1
C2
CLOCK
RESET
V3
DATA
n PULSES

$$n = \frac{C2}{C1} \cdot \frac{V_A}{V_{REF}}$$

FIGURE 25. A-D Converter

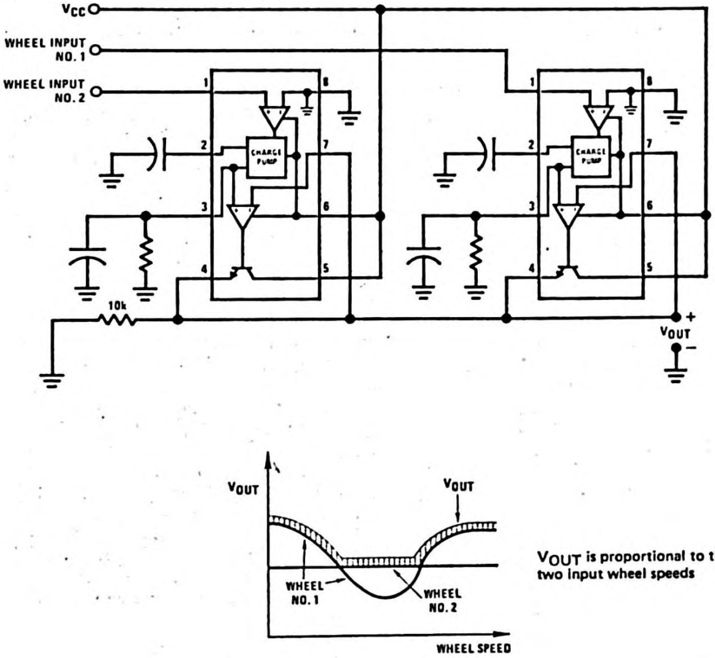
Anti-Skid Circuit Functions

Motor Vehicle Standards 121 place certain stopping requirements on heavy vehicles which require the use of electronic anti-skid control devices.[5] These devices generally use variable reluctance magnetic pickup sensors on the wheels to provide inputs to a control module. One of the questions which the systems designer must answer is whether to use the average from each of the two wheels on a given axle or to use the lower of the two speeds or to use the higher of the two speeds. Each of the three functions can be generated by a single pair of LM2907-8 as illustrated in *Figures 26–28.* In *Figure 26* the input frequency from each wheel sensor is converted to a voltage in the normal manner. The op amp/comparator is connected with negative feedback with a diode in the loop so that the amplifier can only pull down on the load and not pull up. In this way, the outputs from the two devices can be joined together and the output will be the lower of the two input speeds. In *Figure 27* the output emitter of the onboard op amp provides the pullup required to provide a select-high situation where the output is equal to the higher of two speeds. The select average circuit in *Figure 28* saves components by allowing the two charge pumps to operate into a single RC network. One of the amplifiers is needed then to buffer the output and provide a low impedance output which is the average of the two input frequencies. The second amplifier is available for other applications.



V_{OUT} is proportional to the lower of the two input wheel speeds

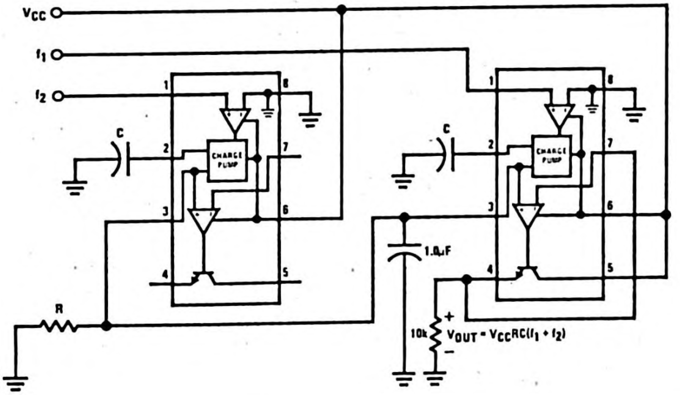
FIGURE 26. "Select-Low" Circuit



V_{CC}
WHEEL INPUT NO. 1
WHEEL INPUT NO. 2
1
2
3
4
5
6
7
8
CHARGE PUMP
10k
+
V_{OUT}
−
V_{OUT}
V_{OUT}
WHEEL NO. 1
WHEEL NO. 2
WHEEL SPEED

V_{OUT} is proportional to the higher of the two input wheel speeds

FIGURE 27. "Select-High" Circuit



V_{CC}
f_1
f_2
C
C
1
2
3
4
5
6
7
8
CHARGE PUMP
R
1.0µF
10k
+
$V_{OUT} = V_{CC}RC(f_1 + f_2)$
−

FIGURE 28. "Select-Average" Circuit

Transmission and Clutch Control Functions

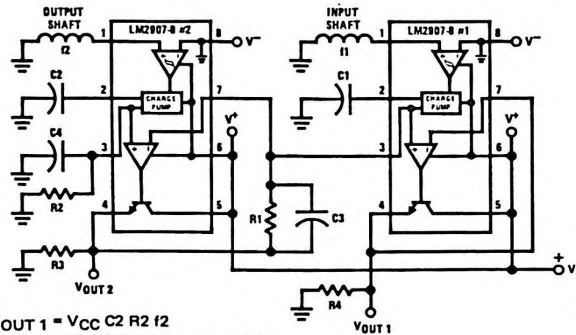
Electric clutches can be added to automotive transmissions to eliminate the 6% slip which typically occurs during cruise and which results in a 6% loss in fuel economy. These devices could be operated by a pair of LM2907's as illustrated in *Figure 29.* Magnetic pickups are connected to input and output shafts of the transmission respectively and provide frequency inputs f_1 and f_2 to the circuit. Frequency, f_2, being the output shaft speed, is also a measure of vehicle road speed. Thus the LM2907-8 No. 2 provides a voltage proportional to road speed at pin 3. This is buffered by the op amp in LM2907-8 No. 1 to provide a speed output V_{OUT1} on pin 4. The input shaft provides charge pulses at the rate of $2f_1$ into the inverting node of op amp 2. This node has the integrating network R1, C3 going back to the output of the op amp so that the charge pulses are integrated and provide an inverted output voltage proportional to the input speed. Thus the output V_{OUT2} is proportional to the difference between the two input frequencies. With these two signals— the road speed and the difference between road speed and input shaft speed—it is possible to develop a number of control functions including the electronic clutch and a complete electronic transmission control. (In the configuration shown, it is not possible for V_{OUT2} to go below zero so that there is a limitation to the output swing in this direction. This may be overcome by returning R3 to a negative bias supply instead of to ground.)

CONCLUSION

The applications presented in this note indicate that the LM2907, LM2917 series devices offer a wide variety of uses ranging from very simple low cost frequency to voltage conversion to complex systems building blocks. It is hoped that the ideas contained here have given suggestions which may help provide new solutions to old problems. Additional applications ideas are included in the data sheet, which should be referred to for all specifications and characteristics.

REFERENCES

1. Society of Automotive Engineers: Preliminary Recommended Environmental Practices for Electronic Equipment Design. October 1974.
2. See for example: Pollution Control Installers Handbook—California Bureau of Automotive Repair No. BAR H-001 § 5.5.4 NOX control systems.
3. TRW Globe Motors, 2275 Stanley Avenue, Dayton, Ohio 45404.
4. S.A.E. Paper #760018 Air Flow Measurement for Engine Control—Robert D. Joy.
5. Code of Federal Regulations. Title 49 Transportation; Chapter V—National Highway Traffic Safety Administration, Dept. of Transportation; Part 571—Federal Motor Vehicle Safety Standards; Standard No. 121.



$V_{OUT\,1} = V_{CC}\ C2\ R2\ f2$

$V_{OUT\,2} = V_{CC}\ (C2\ R2\ f2 - C1\ R1\ f1)$

FIGURE 29. Transmission or Clutch Control Functions

IC Zener Eases Reference Design

National Semiconductor
Application Note 173
Robert C. Dobkin
November 1976

description

A new IC Zener with low dynamic impedance and wide operating current range significantly simplifies reference or regulator circuit design. The low dynamic impedance provides better regulation against operating current changes, easing the requirements on the biasing supply. Further, the temperature coefficient is independent of operating current, so that the LM129 can be used at any convenient current level. Other characteristics such as temperature coefficient, noise and long term stability are equal to or better than good quality discrete Zeners.

The LM129 uses a new subsurface breakdown IC Zener combined with a buffer circuit to lower dynamic impedance. The new subsurface Zener has low noise and excellent long term stability since the breakdown is in the bulk of the silicon. Circuitry around the Zener supplies internal biasing currents and buffers external current changes from the Zener. The overall breakdown is about 6.9 V with devices selected for temperature coefficients.

The Zener is relatively straightforward. A buried Zener D1 breaks down biasing the base of transistor Q1. Transistor Q1 drives two buffers Q2 and Q3. External current changes through the circuit are fully absorbed by the buffer transistors rather than by D1. Current through D1 is held constant at 250 μA by a 2k resistor across the emitter base of Q1 while the emitter-base voltage of Q1 nominally temperature compensates the reference voltage.

The other components, Q4, Q5 and Q6, set the operating current of Q1. Frequency compensation is accomplished with two junction capacitors.

All that is needed for biasing in most applications is a resistor as shown in figure 2. Biasing current can be anywhere from 0.6 mA to 15 mA with little change in performance. Optimally, however, the biasing current should be as low as possible for the best regulation. The dynamic impedance of the LM129 is about 1 Ω and is independent of current. Therefore, the regulation of the LM129 against voltage changes is 1/Rs.

Lower currents or higher Rs give better regulation. For example, with a 15 V supply and 1 mA operating current, the reference change for a 10% change in the 15 V supply is 180 μV. If the LM129 is run at 5 mA, the change is 900 μV or 5 times worse. By comparison, a standard IN821 Zener will change about 17 mV. All discrete Zeners have about the same regulation since their dynamic impedance is inversely proportional to operating current.

If the Zener does not have to be grounded, a bridge compensating circuit can be used to get virtually perfect regulation, as shown in figure 3. A small compensating voltage is generated across R1, which matches the dynamic impedance of the LM129. Since the dynamic impedance of the LM129 is linear with current, this circuit will work even with large changes in the unregulated input voltage.

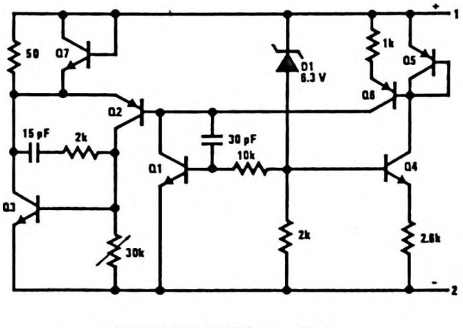


FIGURE 1. IC Reference Zener

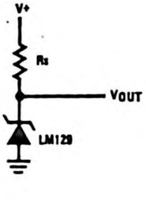


FIGURE 2. Basic Biasing

Other output voltages are easily obtained with the simple op-amp circuit shown in figure 4. A simple non-inverting amplifier is used to boost and buffer the Zener to 10 V. The reference is run directly from the input power rather than the output of the op-amp. When the Zener is powered from the op-amp, special starting circuitry is sometimes necessary to insure the output comes up in the right polarity. For outputs lower than the breakdown of the LM129 a divider can be connected across the Zener to drive the op-amp.

An AC square wave or bipolarity output reference can easily be made with an op-amp and FET switch as shown in figure 5. When Q1 is "ON," the LM108 functions as a normal inverting op-amp with a gain of −1 and an output of −6.9 V. With Q1 "OFF" the op-amp acts as a giving 6.9 V at the output. Some non-symmetry will occur from loading change on the LM129 in the different states and mismatch of R1 and R2. Trimming either R1 or R2 can make the output exactly symmetrical around ground.

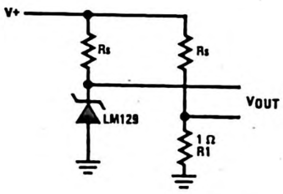

V+
Rs
Rs
LM129
VOUT
1 Ω
R1

FIGURE 3. Bridge Compensation for Line Changes

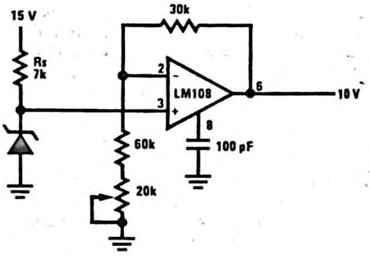

15 V
Rs
7k
30k
2
3
−
+
LM108
6
10 V
8
100 pF
60k
20k

FIGURE 4. 10 Volt Buffered Output Reference

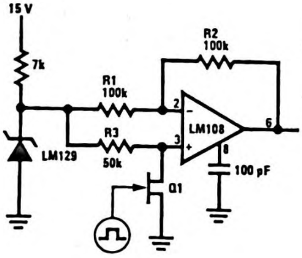

15 V
7k
R2
100k
R1
100k
R3
50k
2
3
−
+
LM108
6
8
100 pF
LM129
Q1

FIGURE 5. Bipolar Output Reference

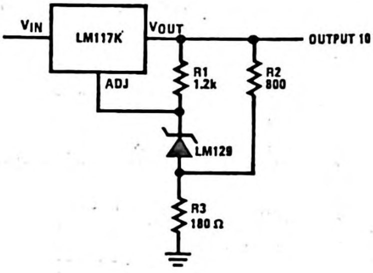

VIN
LM117K
VOUT
ADJ
OUTPUT 10 V
R1
1.2k
R2
800
LM129
R3
180 Ω

FIGURE 6. High Stability 10 V Regulator

By combining the LM129 with an LM117 three-terminal regulator a high stability power regulator can be made. This is shown in figure 6. Resistor R1 biases the LM129 at about 1 mA from the 1.25 V reference in the LM117. The voltage of the LM129 is added to the 1.25 V of the LM117 to make a total reference voltage of 8.1 V. The output voltage is then set at 10 V by R2 and R3. Since the internal reference of the LM117 contributes only about 20% of the total reference voltage, regulation and drift are essentially those of the external Zener. The regulator has 0.2% load and line regulation and if a low drift Zener such as the LM129A is used overall temperature coefficient is less than 0.002%/°C.

The new Zener can be used as the reference for conventional IC voltage regulators for enhanced performance. Noise is lower, time stability is better, and temperature coefficient can be better depending on the device selected. Further, the output voltage is independent of power changes in the regulator.

Figure 7 shows an LM723 using an external LM129 reference. The internal 7 V reference is not used and a single resistor biases the LM129 as the reference. The 5k resistor chosen provides sufficient operating current for the Zener over the 10 V to 40 V input voltage range of the LM723. Since the dynamic impedance of the LM129 is so low, the reference regulation against line changes is only 0.02%/V. This is small compared to the regulation of 0.1%/V for the LM723; however, the resistor can be replaced by a 1 mA to 5 mA FET used as a constant current source for improved regulation. When the FET is used reference regulation is easily 0.001%/V. Output voltage is set in the standard manner except that for low output voltages sufficient current must be run through the Zener to power the voltage divider supplying the reference to the LM723.

An overload protected power shunt regulator is shown in figure 8. The output voltage is about 7.8 V — the 7 V breakdown of the LM129 plus the 0.8 V emitter-base voltage of the LM395. The LM395 is an IC, 1.5 A power transistor with complete overload protection on the chip. Included on the chip are current limiting and thermal limiting, making the device virtually blowout-proof. Further, the base current is only 5 μA, making it easy to drive as a shunt regulator. As the input voltage rises, more drive is applied to the base of the LM395, turning it on harder and dropping more voltage across the series resistance. Should the input voltage rise too high, the LM395 will current limit or thermal limit, protecting itself.

The new IC Zener can replace existing Zeners in just about any application with improved performance and simpler external circuitry. As with any Zener reference, devices are selected for temperature coefficient and operating temperature range. Since the devices are made by a standard integrated circuit process, cost is low and good reproducibility is obtained in volume production.

Finally, since the device is actually an IC, it is packaged in a rugged TO-46 metal can package or a 3-lead plastic transistor package.

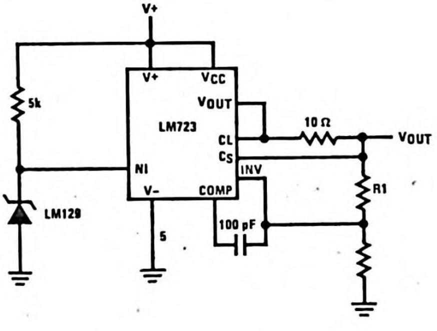


FIGURE 7. External Reference For IC

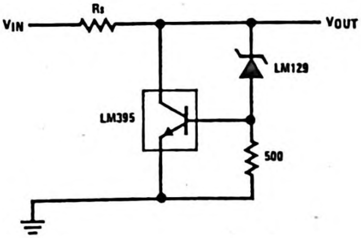


FIGURE 8. Power Shunt Regulator

Applications for an Adjustable IC Power Regulator

National Semiconductor
Application Note 178
Robert C. Dobkin
January 1977

A new 3-terminal adjustable IC power regulator solves many of the problems associated with older, fixed regulators. The LM117, a 1.5A IC regulator is adjustable from 1.2V to 40V with only 2 external resistors. Further, improvements are made in performance over older regulators. Load and line regulation are a factor of 10 better than previous regulators. Input voltage range is increased to 40V and output characteristics are fully specified for loads of 1.5A. Reliability is improved by new overload protection circuitry as well as *100% burn-in* of all parts. The table below summarizes the typical performance of the LM117.

TABLE I.

Output Voltage Range	1.25V–40V
Line Regulation	0.01%/V
Load Regulation $I_L = 1.5A$	0.1%
Reference Voltage	1.25V
Adjustment Pin Current	50 μA
Minimum Load Current (Quiescent Current)	3.5 mA
Temperature Stability	0.01%/°C
Current Limit	2.2A
Ripple Rejection	80 dB

The overload protection circuitry on the LM117 includes current limiting, safe-area protection for the internal power transistor and thermal limiting. The current limit is set at 2.2A and, unlike presently available positive regulators, remains relatively constant with temperature. Over a −55°C to +150°C temperature range, the current limit only shifts about 10%.

At high input-to-output voltage differentials the safe-area protection decreases the current limit. With the LM117, full output current is available to 15V differential and, even at 40V, about 400 mA is available. With some regulators, the output will shut completely off when the input-to-output differential goes above 30V, possibly causing start-up problems. Finally, the thermal limiting is always active and will protect the device even if the adjustment terminal should become accidentally disconnected.

Since the LM117 is a floating voltage regulator, it sees only the input-to-output voltage differential. This is of benefit, especially at high output voltage. For example, a 30V regulator nominally operating with a 38V input can have a 70V input transient before the 40V input-to-output rating of the LM117 is exceeded.

BASIC OPERATION

The operation of how a 3-terminal regulator is adjusted can be easily understood by referring to *Figure 1*, which shows a functional circuit. An op amp, connected as a unity gain buffer, drives a power Darlington. The op amp and biasing circuitry for the regulator is arranged so that all the quiescent current is delivered to the regulator output (rather than ground) eliminating the need for a separate ground terminal. Further, all the circuitry is designed to operate over the 2V to 40V input-to-output differential of the regulator.

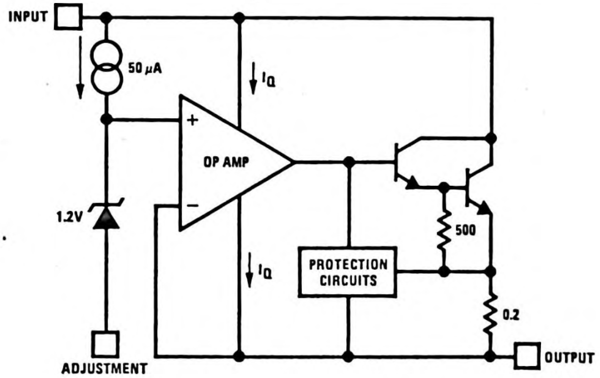


FIGURE 1. Functional Schematic of the LM117

A 1.2V reference voltage appears inserted between the non-inverting input of the op amp and the adjustment terminal. About 50 μA is needed to bias the reference and this current comes out of the adjustment terminal. In operation, the output of the regulator is the voltage of the adjustment terminal plus 1.2V. If the adjustment terminal is grounded, the device acts as a 1.2V regulator. For higher output voltages, a divider R1 and R2 is connected from the output to ground as is shown in *Figure 2*. The 1.2V reference across resistor R1 forces 10 mA of current to flow. This 10 mA then flows through R2, increasing the voltage at the adjustment terminal and therefore the output voltage. The output voltage is given by:

$$V_{OUT} = 1.2V \times \left(1 + \frac{R2}{R1}\right) + 50\ \mu A\ R2$$

The 50 μA biasing current is small compared to 5 mA and causes only a small error in actual output voltages. Further, it is extremely well regulated against line voltage or load current changes so that it contributes virtually no error to dynamic regulation. Of course, programming currents other than 10 mA can be used depending upon the application.

Since the regulator is floating, all the quiescent current must be absorbed by the load. With too light of a load, regulation is impaired. Usually, a 5 mA programming current is sufficient; however, worst case minimum load for commercial grade parts requires a minimum load of 10 mA. The minimum load current can be compared to the quiescent current of standard regulators.

APPLICATIONS

An adjustable lab regulator using the LM117 is shown in *Figure 2* and has a 1.2V to 25V output range. A 10 mA program current is set by R1 while the output voltage is set by R2. Capacitor C1 is optional to improve ripple rejection so that 80 dB is obtained at any output voltage. The diode, although not necessary in this circuit since the output is limited to 25V, is needed with outputs over 25V to protect against the capacitors discharging through low current nodes in the LM117 when the input or output is shorted.

The programming current is constant and can be used to bias other circuitry, while the regulator is used as the power supply for the system. In *Figure 3*, the LM117 is used as a 15V regulator while the programming current powers an LM129 zener reference. The LM129 is an IC zener with less than 1Ω dynamic impedance and can operate over a range of 0.5 mA to 15 mA with virtually no change in performance.

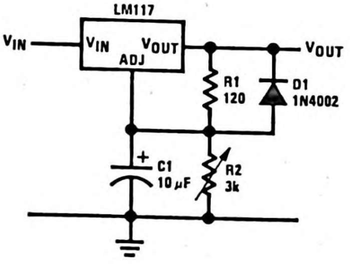


FIGURE 2. Basic Voltage Regulator

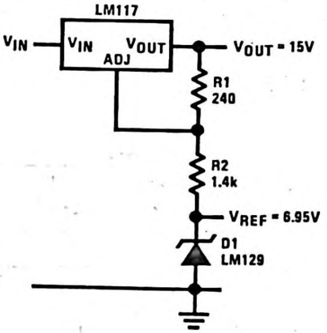


FIGURE 3. Regulator and Voltage Reference

Another example of using the programming current is shown in *Figure 4* where the output setting resistor is tapped to provide multiple output voltage to op amp buffers. An additional transistor is included as part of the overload protection. When any of the outputs are shorted, the op amp will current limit and a voltage will be developed across its inputs. This will turn "ON" the transistor and pull down the adjustment terminal of the LM117, causing all outputs to decrease, minimizing possible damage to the rest of the circuitry.

Ordinary 3-terminal regulators are not especially attractive for use as precision current regulators. Firstly, the quiescent current can be as high as 10 mA, giving at least 1% error at 1A output currents, and more error at lower currents. Secondly, at least 7V is needed to operate the device. With the LM117, the only error current is 50 μA from the adjustment terminal, and only 4.2V is needed for operation at 1.5A or 3.2V at 0.5A. A simple 2-terminal current regulator is shown in *Figure 5* and is usable anywhere from 10 mA to 1.5A.

Figure 6 shows an adjustable current regulator in conjunction with the voltage regulator from *Figure 2* to make constant voltage/constant current lab-type supply. Current sensing is done across R1, a 1Ω resistor,

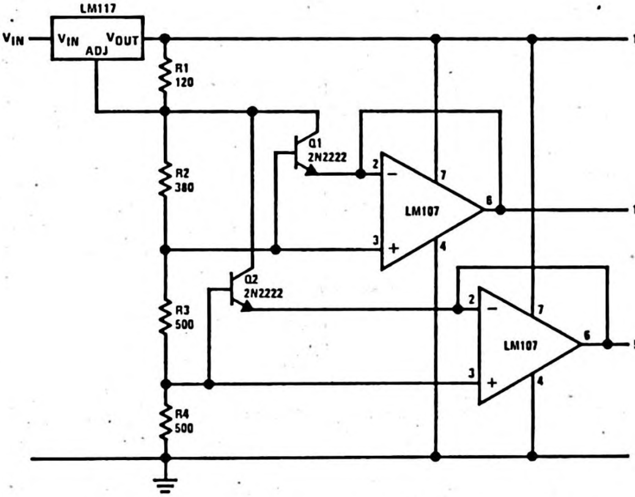
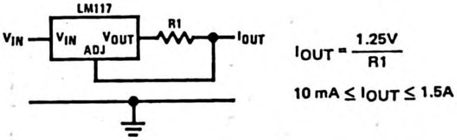

LM117
VIN
VIN
ADJ
VOUT
R1
120
R2
380
R3
500
R4
500
Q1
2N2222
Q2
2N2222
LM107
LM107
2
3
7
4
6
2
3
7
4
6
15V
10V
5V

FIGURE 4. Regulator with Multiple Outputs


LM117
VIN
VIN
ADJ
VOUT
R1
IOUT

$$I_{OUT} = \frac{1.25V}{R1}$$

$$10\text{ mA} \le I_{OUT} \le 1.5A$$

FIGURE 5. 2-Terminal Current Regulator

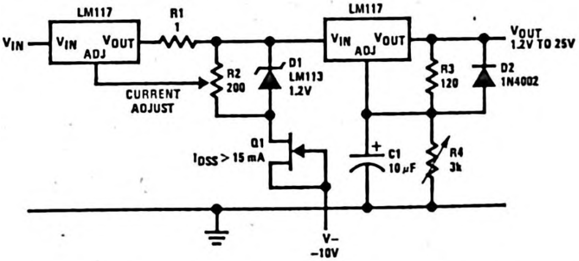
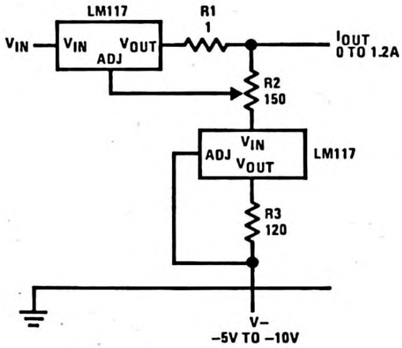

LM117
VIN
VIN
ADJ
VOUT
R1
1
R2
200
CURRENT
ADJUST
D1
LM113
1.2V
Q1
IDSS > 15 mA
LM117
VIN
ADJ
VOUT
C1
10 μF
R3
120
R4
3k
D2
1N4002
VOUT
1.2V TO 25V
V−
−10V

FIGURE 6. Adjustable Regulator. Constant Voltage/Constant Current, 10 mA to 1.2A

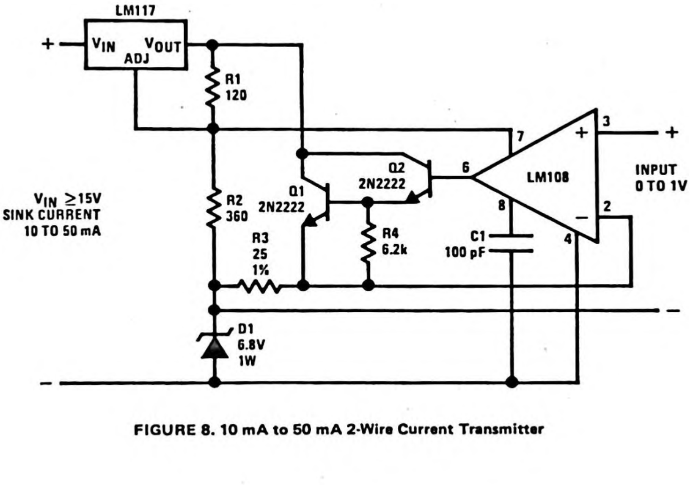
while R2 sets the current limit point. When the wiper of R2 is connected, the 1Ω sense resistor current is regulated at 1.2A. As R2 is adjusted, a portion of the 1.2V reference of the LM117 is cancelled by the drop across the pot, decreasing the current limit point. At low output currents, current regulation is degraded since the voltage across the 1Ω sensing resistor becomes quite low. For example, with 50 mA output current, only 50 mV is dropped across the sense resistor and the supply rejection of the LM117 will limit the current regulation to about 3% for a 40V change across the device. An alternate current regulator is shown in *Figure 7* using an additional LM117 to provide the reference, rather than an LM113 diode. Both current regulators need a negative supply to operate down to ground.

Figure 8 shows a 2-wire current transmitter with 10 mA to 50 mA output current for a 1V input. An LM117 is biased as a 10 mA current source to set the minimum current and provide operating current for the control circuitry. Operating off the 10 mA is an LM108 and an LM129 zener. The zener provides a common-mode voltage for operation of the LM108 as well as a 6.9V reference, if needed. Input signals are impressed across R3, and the current through R3 is delivered to the output of the regulator by Q1 and Q2. For a 25Ω resistor, this gives a 40 mA current change for a 1V input. This circuit can be used in 4 mA to 20 mA applications, but the LM117 must be selected for low quiescent current. Minimum operating voltage is about 12V.



LM117
R1
1
V_{IN}
V_{IN}
V_{OUT}
ADJ
I_{OUT}
0 TO 1.2A
R2
150
V_{IN}
ADJ
V_{OUT}
LM117
R3
120
V−
−5V TO −10V

FIGURE 7. Adjustable Current Regulator



LM117
+
V_{IN}
V_{OUT}
ADJ
R1
120
7
3
+
+
Q2
2N2222
6
LM108
INPUT
0 TO 1V
V_{IN} ≥15V
SINK CURRENT
10 TO 50 mA
R2
360
Q1
2N2222
8
2
−
R3
25
1%
R4
6.2k
C1
100 pF
4
−
D1
6.8V
1W
−

FIGURE 8. 10 mA to 50 mA 2-Wire Current Transmitter

Analog-to-Digital Converter Testing

National Semiconductor
Application Note 179
Dennis Dauenhauer
Doug Falco
April 1977

Attempting to test an analog-to-digital converter can be a challenging and rewarding experience. The recent increased interest in converter products has spawned renewed interest in test equipment dedicated to testing converters. Unfortunately, the broad range of converter products available makes testing by a single piece of equipment difficult at best.

A crude method of testing would be to monitor an analog signal at the converter input using a precision DVM and compare that with the converter output. This is simple enough to do, but in most cases this would prove impractical. For a 10-bit converter, this would require plotting 1,024 such readings. Automatic equipment can be used, but in all cases will require some sophisticated interface hardware and software routines. A person favoring auto test equipment can expect to pay around $10,000 for the hardware and at least that much for the software. What will be described is a method which costs a couple hundred dollars in components and which gives a device characteristic in a relatively short time period.

Because very little standardization has occurred for converter products, the user must adhere to the old adage "caveat emptor" or "buyer beware". The only universal statement that can be made for definitions of terms characterizing converter products is that they are universally inconsistent. For this reason, this application note will provide a simple method of providing a very graphic means of testing several of National's A/D converter products. It is also recommended that the reader refer to Application Note AN-156 for additional information concerning converter products definitions. Specific parameters which will be focused on in this paper are zero error, scale error, non-linearity error, differential non-linearity, monotonicity, total unadjusted error and quantizing error.

The block diagram of *Figure 1* shows the basic blocks of the complete test circuit of *Figure 2*. A storage scope is required to provide a continuous display. A Tektronix 7633 or equivalent is recommended. A typical characteristic for the ADC0800 shown in *Figure 3*.

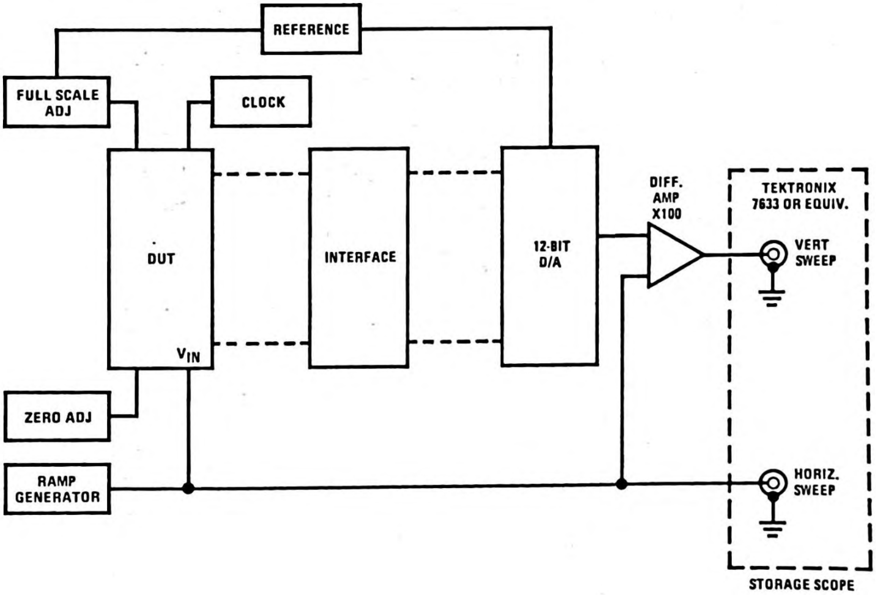
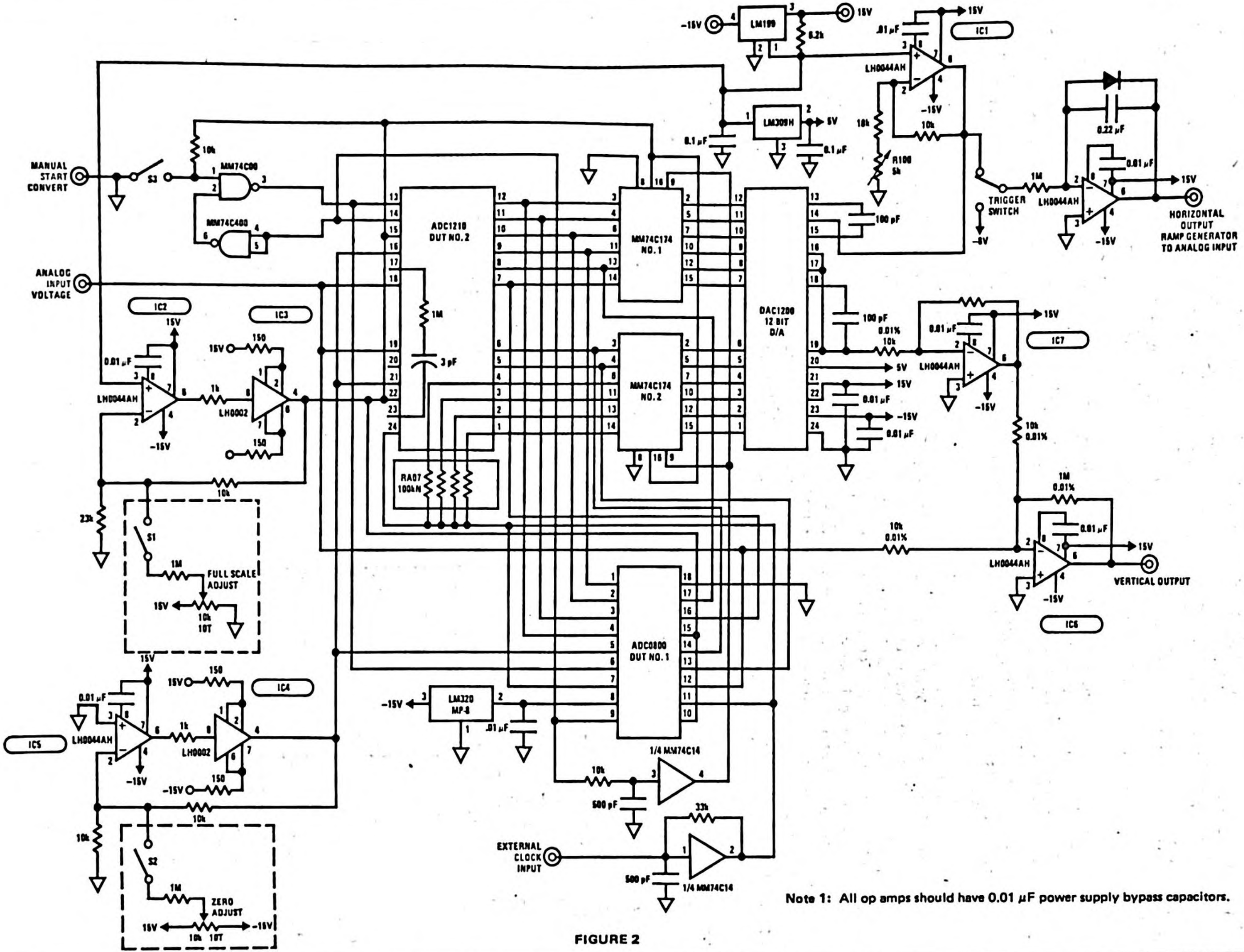


FIGURE 1. Block Diagram for A/D Tester

AN179-1


MANUAL START CONVERT
S3
10k
MM74C00
MM74C400
ANALOG INPUT VOLTAGE
IC2
IC3
IC4
IC5
IC1
IC6
IC7
LH0044AH
LH0002
0.01 μF
1k
150
15V
−15V
23k
10k
S1
1M
FULL SCALE ADJUST
10k 10T
S2
ZERO ADJUST
ADC1210 DUT NO. 2
RA07 100kΩ
3 pF
MM74C174 NO. 1
MM74C174 NO. 2
DAC1200 12 BIT D/A
ADC0800 DUT NO. 1
LM199
8.2k
LM309H
5V
0.1 μF
.01 μF
R100 5k
TRIGGER SWITCH
−5V
0.22 μF
HORIZONTAL OUTPUT RAMP GENERATOR TO ANALOG INPUT
100 pF
10k 0.01%
1M 0.01%
VERTICAL OUTPUT
LM320 MP-8
1/4 MM74C14
500 pF
33k
EXTERNAL CLOCK INPUT

Note 1: All op amps should have 0.01 μF power supply bypass capacitors.

FIGURE 2

The ramp generator provides a linear output voltage from 0V to 10V. This voltage is used as a) the horizontal amplifier input to the scope b) as a reference voltage to the difference amplifier and c) as the analog input voltage to the device under test.

The storage scope is used as an X-Y display with the horizontal input functioning as an input amplifier. The vertical input (Y-direction) displays the difference between the converter's analog input voltage and the equivalent output voltage of the same converter. The equivalent output voltage is generated by the 12-bit digital-to-analog converter (DAC1200). The horizontal input (X-direction) displays the difference voltage over the entire analog input voltage range. For a reference voltage set to 10.24V, the range is 0V to 10.24V. In the case of an 8-bit A/D, there would be 256 different voltages displayed across the entire range of the reference.

The test circuit shown in *Figure 2* can be used to test the ADC0800, ADC1211 or the ADC1210. These are 8-bit, 10-bit and 12-bit analog-to-digital converters.

Zero and full scale adjustment circuits are provided to allow a more accurate computation of non-linearity error.

The DAC1200D is a 12-bit D/A converter. It is quite adequate for the 8-bit and 10-bit parts but may be replaced by a higher resolution part if testing 12-bit A/D converters. The LH0044AH is a precision low noise amplifier and the LH0002CH is a buffer amplifier. The output of the reference must be adjusted to the full scale input voltage to assure proper output from the DAC1200. This is done by adjusting R-100.

TESTING

Figure 3 shows a typical output characteristic for the ADC0800, an 8-bit A/D converter. The reference line is set by switching the vertical channel (Y-axis amplifier) to dc and triggering the ramp generator. The adjustment is made using the horizontal positioning. The vertical range should be set to 5V/division. The 50 mV/division shown is the effective range of the channel taking into the account that the difference amplifier has a gain of 100.

When the initial set-up is completed, it is relatively easy to get readings for zero error, scale error, non-linearity error, differential non-linearity error, quantizing error, and to detect missing codes.

Zero error is simply the deviation from the reference line to the middle of the quantizing error when the input voltage is zero. All errors can be expressed as percent of full scale of in LSB's (least significant bits). For a 0V to 10.24V analog input 8-bit converter;

$$1\ \text{LSB} = \frac{10\text{V}}{2^8} = 40\ \text{mV} = 0.40\%\ \text{FS}$$

Scale error is the same as the zero error except that it occurs when the analog input voltage is at full scale.

In most applications, it is not the non-linearity in itself which is important, but rather the slope of the non-linearity. For instance, in an application using an A/D to sense gas in a tank and then to compute the remaining miles or time based on the current rate of usage, you do not want a large non-linearity slope. This gives the typical analog gas gauge effect of getting what appears to be good mileage over a certain range and poorer mileage over another range. Specifying non-linearity error and differential non-linearity error provides an error band around which to limit this change in slope or rate of change.

Non-linearity error can be defined in either of 2 ways. Shown in *Figure 3* is the "best straight line" definition for non-linearity. This is the more traditional definition for non-linearity and is the one use for the ADC0800 because of the inherent unidirectional nature of the error. A more conservative definition of "ideal straight line linearity" or more appropriately "total error" is twice that of the best straight line error. This linearity error is the maximum deviation from a straight line drawn between zero and full scale. The ADC1210 and ADC1211, 12-bit and 10-bit A/D converters, use this definition of non-linearity because the deviation can be in either direction.

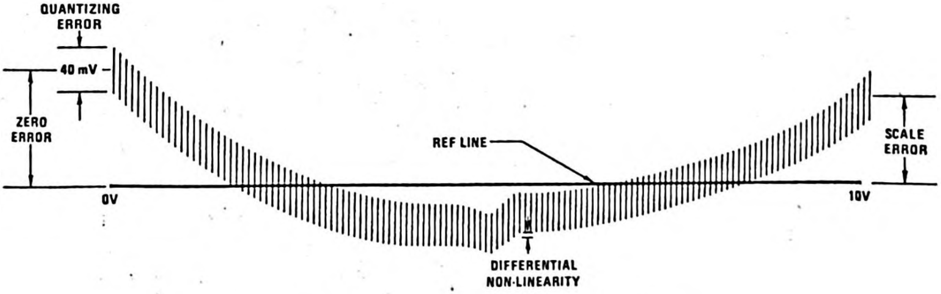


FIGURE 3. Typical Output Characteristic for the ADC0800

Differential non-linearity is most noticeable in converters using the successive approximation technique for conversion. It occurs when switching in a new resistance value for approximating the analog input voltage. It is the amount of change in the input voltage required to get a change in the digital output. On the scope it shows up as a change in non-linearity at one point. Differential non-linearity with this test method can be used to check for "no missing codes". "No missing codes" means that over the reference range, the converter will provide 2^n digital output codes, where N is the resolution of the converter.

Total unadjusted error is the maximum deviation from an ideal transfer function for an A/D converter. This error does not include quantizing error. The non-linearity error of an unadjusted ADC0800 is in a direction so as to decrease the total error. Therefore, the total unadjusted error for the ADC0800 will be either the zero error or the scale error, whichever is greater. This characteristic is only peculiar to this form of successive approximation type of converter.

Quantizing is inherent in the nature of the device. An 8-bit converter can make only 256 changes in the output regardless of the input voltage range. Therefore, for any converter there is always 1 LSB of quantizing error. This would appear as ±1/2 LSB of error around a straight line approximation of the output characteristic.

Monotonicity is the ability of the converter to give a digital output which is always in the same direction as the analog input voltage. The ADC0800 is inherently monotonic.

This paper has focused on the parameters peculiar to A/D converter products. It should give the user of any manufacturer's A/D converter a method for easily testing and comparing the characteristics of a particular A/D converter. It provides a low cost means of testing parameters which have historically been difficult to test.

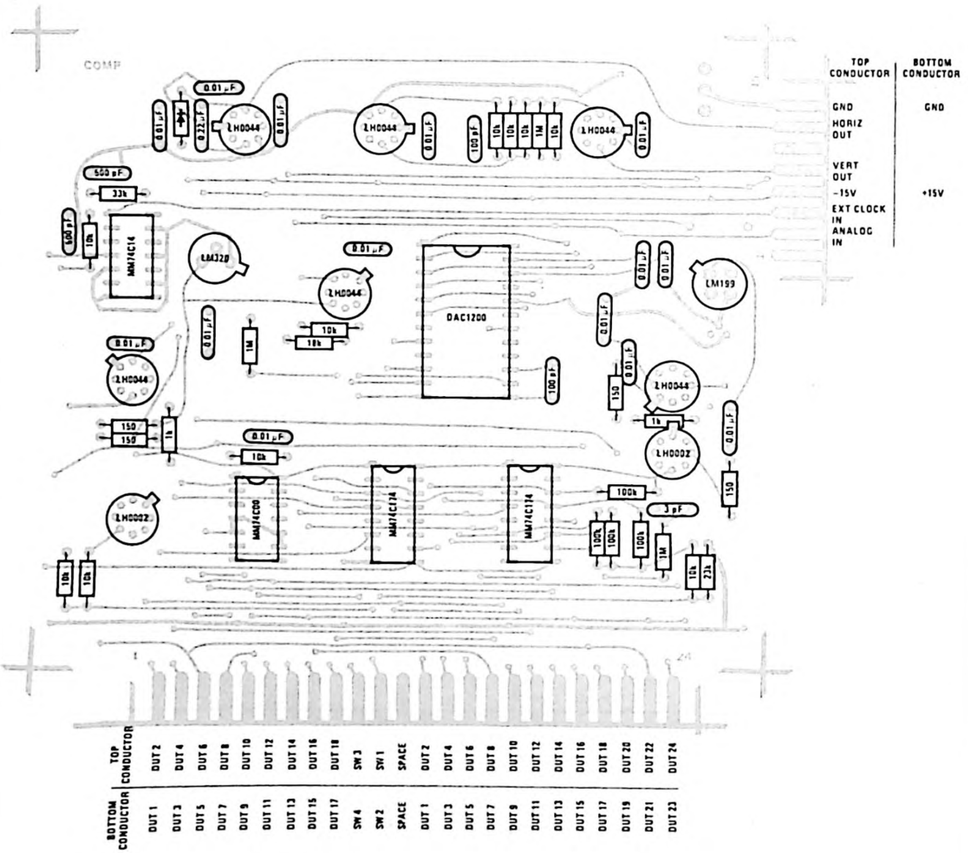

COMP
TOP CONDUCTOR
BOTTOM CONDUCTOR
GND
HORIZ OUT
VERT OUT
-15V
+15V
EXT CLOCK IN
ANALOG IN
LH0044
LH0002
LM320
LM199
MM74C14
MM74C00
MM74C174
DAC1200
0.01 µF
0.22 µF
500 pF
100 pF
3 pF
33k
10k
18k
1M
1k
150
100k
22k
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
OUT 6
OUT 7
OUT 8
OUT 9
OUT 10
OUT 11
OUT 12
OUT 13
OUT 14
OUT 15
OUT 16
OUT 17
OUT 18
OUT 19
OUT 20
OUT 21
OUT 22
OUT 23
OUT 24
SW 1
SW 2
SW 3
SW 4
SPACE

FIGURE 4. "Component Placement" on Component Side of P.C. Board

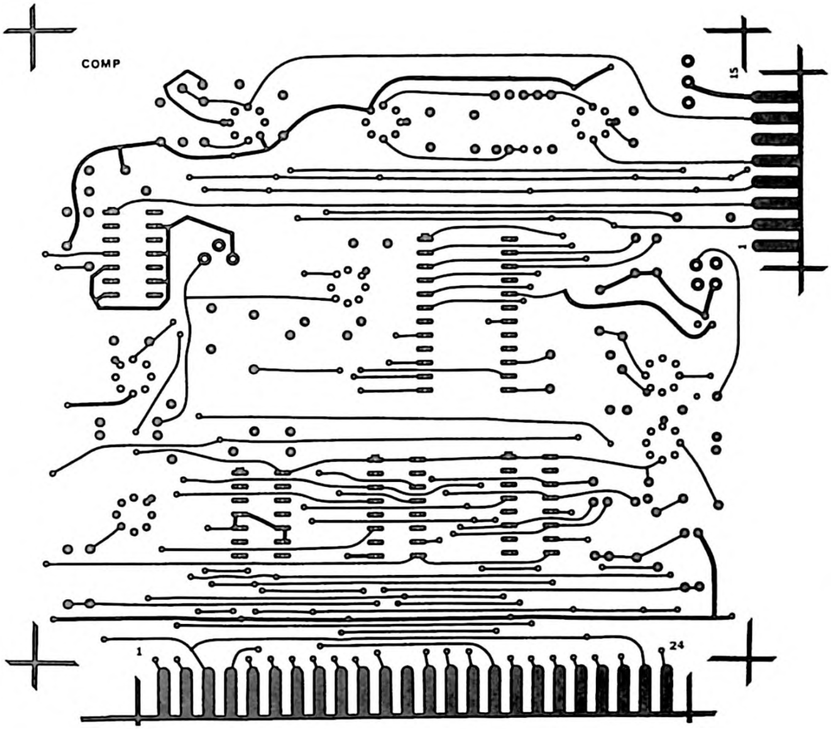

COMP
15
1
1
24

FIGURE 5. Component Side of P.C. Board Layout

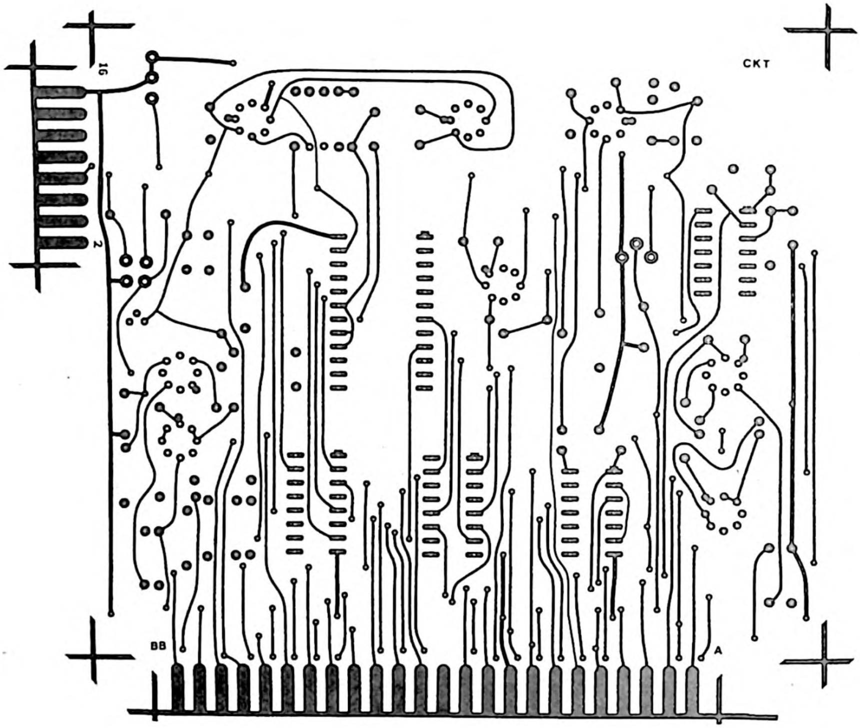


FIGURE 6. Backside of P.C. Board Layout

3-Terminal Regulator is Adjustable

National Semiconductor
Application Note 181
Robert C. Dobkin
March 1977

INTRODUCTION

Until now, all of the 3-terminal power IC voltage regulators have a fixed output voltage. In spite of this limitation, their ease of use, low cost, and full on-chip overload protection have generated wide acceptance. Now, with the introduction of the LM117, it is possible to use a single regulator for any output voltage from 1.2V to 37V at 1.5A. Selecting close-tolerance output voltage parts or designing discrete regulators for particular applications is no longer necessary since the output voltage can be adjusted. Further, only one regulator type need be stocked for a wide range of applications. Additionally, an adjustable regulator is more versatile, lending itself to many applications not suitable for fixed output devices.

In addition to adjustability, the new regulator features performance a factor of 10 better than fixed output regulators. Line regulation is 0.01%/V and load regulation is only 0.1%. It is packaged in standard TO-3 transistor packages so that heat sinking is easily accomplished with standard heat sinks. Besides higher performance, overload protection circuitry is improved, increasing reliability.

ADJUSTABLE REGULATOR CIRCUIT

The adjustment of a 3-terminal regulator can be easily understood by referring to *Figure 1*, which shows a functional circuit. An op amp, connected as a unity gain buffer, drives a power Darlington. The op amp and biasing circuitry for the regulator are arranged so that all the quiescent current is delivered to the regulator output (rather than ground) eliminating the need for a separate ground terminal. Further, all the circuitry is designed to operate over the 2V to 40V input to output differential of the regulator.

A 1.2V reference voltage appears inserted between the non-inverting input of the op amp and the adjustment terminal. About 50 μA is needed to bias the reference and this current comes out of the adjustment terminal. In operation, the output of the regulator is the voltage of the adjustment terminal plus 1.2V. If the adjustment terminal is grounded, the device acts as a 1.2V regulator. For higher output voltages, a divider R1 and R2 is connected from the output to ground as is shown in *Figure 2*. The 1.2V reference across resistor R1 forces 5 mA of current to flow. This 5 mA then flows through R2, increasing the voltage at the adjustment terminal and therefore the output voltage. The output voltage is given by:

$$V_{OUT} = 1.2V\left(1+\frac{R2}{R1}\right) + 50\,\mu A\ R2$$

The 50 μA biasing current is small compared to 5 mA and causes only a small error in actual output voltages. Further, it is extremely well regulated against line voltage or load current changes so that it contributes virtually no error to dynamic regulation. Of course, programming currents other than 5 mA can be used depending upon the application.

Since the regulator is floating, all the quiescent current must be absorbed by the load. With too light of a load, regulation is impaired. Usually the 5 mA programming current is sufficient; however, worst case minimum load for commercial grade parts requires a minimum load of 10 mA. The minimum load current can be compared to the quiescent current of standard regulators.

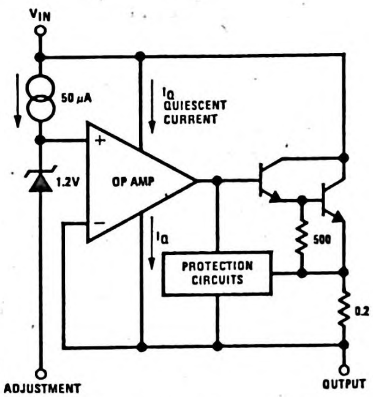
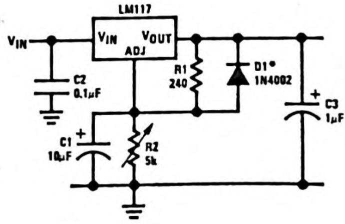


FIGURE 1. Functional Schematic of the LM117



†Solid tantalum
*Discharges C1 if output is shorted to ground

FIGURE 2. Adjustable Regulator with Improved Ripple Rejection

OVERLOAD PROTECTION CIRCUITRY

An important advancement in the LM117 is improved current limit circuitry. Current limit is set internally at about 2.2A and the current limit remains constant with temperature. Older devices such as the LM309 or LM7800 regulators use the turn-on of an emitter-base junction of a transistor to set the current limit. This causes current limit to typically change by a factor of 2 over a −55°C to +150°C temperature range. Further, to insure adequate output current at 150°C the current limit is relatively high at 25°C, which can cause problems by overloading the input supply.

Also included is safe-area protection for the pass transistor to decrease the current limit as input-to-output voltage differential increases. The safe area protection circuit in the LM117 allows full output current at 15V differential and does not allow the current limit to drop to zero at high input-to-output differential voltages, thus preventing start up problems with high input voltages. *Figure 3* compares the current limit of the LM117 to an LM340 regulator.

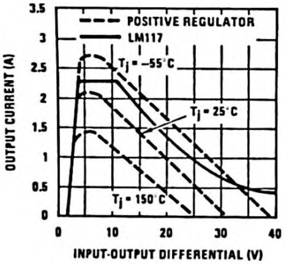


FIGURE 3. Comparison of LM117 Current Limit with Older Positive Regulator

Thermal overload protection, included on the chip, turns the regulator OFF when the chip temperature exceeds about 170°C, preventing destruction due to excessive heating. Previously, the thermal limit circuitry required about 7V to operate. The LM117 has a new design that is operative down to about 2V. Further, the thermal limit and current limit circuitry in the LM117 are functional, even if the adjustment terminal should be accidentally disconnected.

OPERATING THE LM117

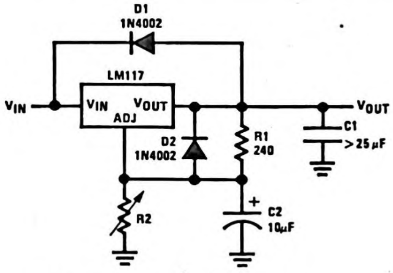
The basic regulator connection for the LM117, as shown in *Figure 2*, only requires the addition of 2 resistors and a standard input bypass capacitor. Resistor R2 sets the output voltage while R1 provides the 5 mA programming current. The 2 capacitors on the adjustment and output terminals are optional for improved performance.

Bypassing the adjustment terminal to ground improves ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 µF bypass capacitor, 80 dB ripple rejection is obtainable at any output level. Increases over 10 µF do not appreciably improve the ripple rejection at 120 Hz. If a bypass capacitor is used, it is sometimes necessary to include protection diodes as discussed later, to prevent the capacitor from discharging through internal low current paths in the LM117 and damaging the device.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 µF solid tantalum (or 25 µF aluminum electrolytic) on the output swamps this effect and insures stability. When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 µF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain a 20A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 µF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal (C2) can discharge through a low current junction. Discharge occurs when either the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V and less than 10 µF capacitance. *Figure 4* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \cdot I_{ADJ}$$

D1 protects against C1 (input shorts)

D2 protects against C2 (output shorts)

FIGURE 4. Regulator with Protection Diodes Against Capacitor Discharge

Some care should be taken in making connection to the LM117 to achieve the best load regulation. Series resistance between the output of the regulator and programming resistor R1 should be minimized. Any voltage drop due to load current through this series resistance appears as a change in the reference voltage and degrades regulation. If possible, 2 wires should be connected to the output—1 for load current and 1 for resistor R1. The ground of R2 can be returned near the ground of the load to provide remote sensing and improve load regulation.

APPLICATIONS

Figure 5 shows a 0V to 25V general purpose lab supply. Operation of the LM317 down to 0V output requires the addition of a negative supply so that the adjustment terminal can be driven to −1.2V. An LM329 6.9V reference is used to provide a regulated −1.2V reference to the bottom of adjustment pot R2. The LM129 is an IC zener which has exceptionally low dynamic impedance so the negative supply need not be well regulated. Note that a 10 mA programming current is used since lab supplies are often used with no-load, and the LM317 requires a worst-case minimum load of 10 mA.

The 1.2V minimum output of the LM117 makes it easy to design power supplies with electrical shut-down. At 1.2V, most circuits draw only a small fraction of their normal operating current. In *Figure 6* a TTL input signal causes Q1 to ground the adjustment terminal decreasing the output to 1.2V. If true zero output is desired, the adjustment can be driven to −1.2V; however, this does require a separate negative supply.

When fixed output voltage regulators are used as on-card regulator for multiple cards, the normal output voltage tolerance of ±5% between regulators can cause as much as 10% difference in operating voltage between cards. This can cause operating speed differences in digital circuitry, interfacing problems or decrease noise margins.

Figure 7 shows a method of adjusting multiple on-card regulators so that all outputs track within ±100 mV. The adjustment terminals of all devices are tied together and a single divider is used to set the outputs. Programming current is set at 10 mA to minimize the effects of the 50 μA biasing current of the regulators and should further be increased if many LM117's are used. Diodes connected across each regulator insure that all outputs will decrease if 1 regulator is shorted.

Two terminal current regulators can be made with fixed-output regulators; however, their high output voltage and high quiescent current limit their accuracy. With the LM117 as shown in *Figure 8*, a high performance current source useful from 10 mA to 1.5A can be made. Current regulation is typically 0.01%/V even at low currents since the quiescent current does not cause an error. Minimum operating voltage is less than 4V, so it is also useful as an in-line adjustable current limiter for protection of other circuitry.

Low cost adjustable switching regulators can be made using an LM317 as the control element. *Figure 9* shows the simplest configuration. A power PNP is used as the switch driving an L-C filter. Positive feedback for hysteresis is applied to the LM317 through R6. When the PNP switches, a small square wave is generated across R5. This is level shifted and applied to the adjustment terminal of the regulator by R4 and C2, causing it to

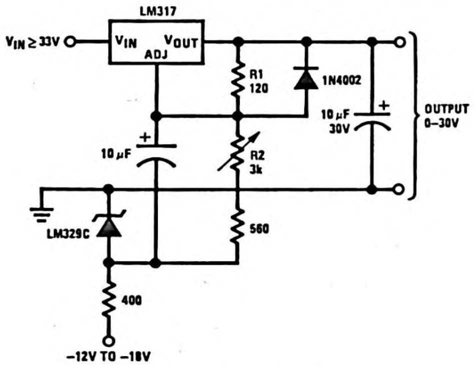
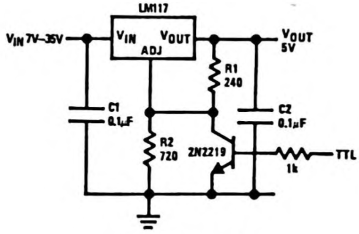
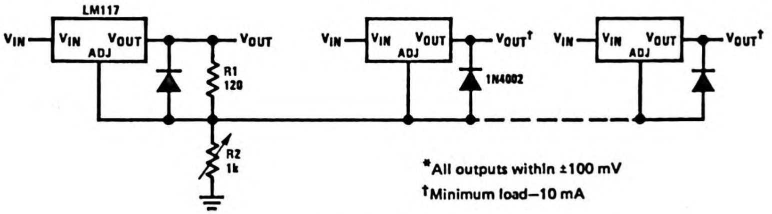


FIGURE 5. General Purpose 0–30V Power Supply



*Min output ≈ 1.2V

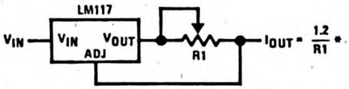
FIGURE 6. 5V Logic Regulator with Electronic Shutdown*



*All outputs within ±100 mV

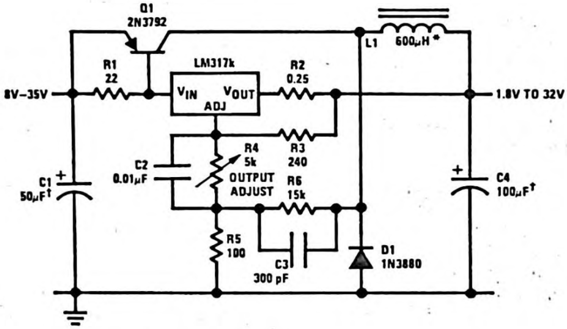
†Minimum load—10 mA

FIGURE 7. Adjusting Multiple On-Card Regulators with Single Control*



*0.8Ω ≤ R1 ≤ 120Ω

FIGURE 8. Precision Current Limiter



†Solid tantalum
*Core—Arnold A-254168-2 60 turns

FIGURE 9. Low Cost 3A Switching Regulator

switch ON or OFF. Negative feedback is taken from the output through R3, making the circuit oscillate. Capacitor C3 acts as a speed-up, increasing switching speed, while R2 limits the peak drive current to Q1.

The circuit in *Figure 9* provides no protection for Q1 in case of an overload. A blow-out proof switching regulator is shown in *Figure 10*. The PNP transistor has been replaced by a PNP-NPN combination with LM395's used as the NPN transistors. The LM395 is an IC which acts as an NPN transistor with overload protection. Included on the LM395 is current limiting, safe-area protection and thermal overload protection making the device virtually immune to any type of overload.

Efficiency for the regulators ranges from 65% to 85%, depending on output voltage. At low output voltages, fixed power losses are a greater percentage of the total output power so efficiency is lowest. Operating frequency is about 30 kHz and ripple is about 150 mV, depending upon input voltage. Load regulation is about 50 mV and line regulation about 1% for a 10V input change.

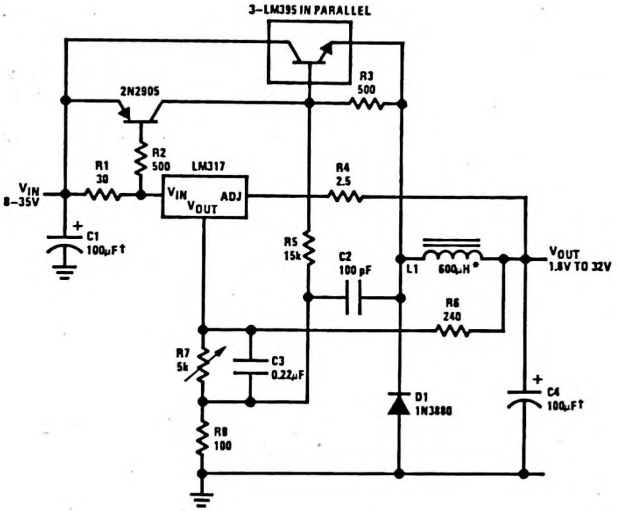
One of the more unique applications for these switching regulators is as a tracking pre-regulator. The only DC connection to ground on either regulator is through the 100Ω resistor (R5 or R8) that sets the hysteresis. Instead of tying this resistor to ground, it can be connected to the output of a linear regulator so that the switching regulator maintains a constant input-to-output differential on the linear regulator. The switching regulator would typically be set to hold the input voltage to the linear regulator about 3V higher than the output.

Battery charging is another application uniquely suited for the LM117. Since battery voltage is dependent on electrochemical reactions, the charger must be designed specifically for the battery type and number of cells. Ni-Cads are easily charged with the constant current sources shown previously. For float chargers on lead-acid type batteries all that is necessary is to set the output of the LM117 at the float voltage and connect it to the battery. An adjustable regulator is mandatory since, for long battery life the float voltage must be precisely controlled. The output voltage temperature coefficient can be matched to the battery by inserting diodes in series with the adjustment resistor for the regulator and coupling the diodes to the battery.

A high performance charger for gelled electrolite lead-acid batteries is shown in *Figure 11*. This charger is designed to quickly recharge a battery and shut off at full charge.

Initially, the charging current is limited to 2A by the internal current limit of the LM117. As the battery voltage rises, current to the battery decreases and when the current has decreased to 150 mA, the charger switches to a lower float voltage preventing overcharge. With a discharged battery, the start switch is not needed since the charger will start by itself; however, it is included to allow topping off even slightly discharged batteries.

When the start switch is pushed, the output of the charger goes to 14.5V set by R1, R2 and R3. Output current is sensed across R6 and compared to a fraction of the 1.2V reference (across R2) by an LM301A op


3–LM395 IN PARALLEL
2N2905
R3
500
R2
500
LM317
R1
30
R4
2.5
V_{IN}
8–35V
V_{IN}
V_{OUT}
ADJ
C1
100μF†
R5
15k
C2
100 pF
L1
600μH*
V_{OUT}
1.8V TO 32V
R6
240
R7
5k
C3
0.22μF
D1
1N3880
C4
100μF†
R8
100

†Solid tantalum

*Core—Arnold A-254168-2 60 turns

FIGURE 10. 4A Switching Regulator with Overload Protection

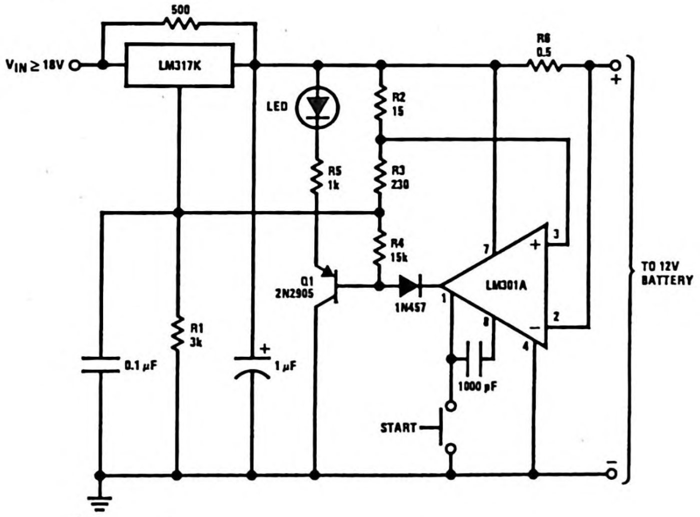

500
$V_{IN} \geq 18V$
LM317K
R6
0.5
+
LED
R2
15
R5
1k
R3
230
R4
15k
Q1
2N2905
1N457
LM301A
7
3
2
1
8
4
TO 12V
BATTERY
R1
3k
0.1 μF
1 μF
1000 pF
START
–

FIGURE 11. 12V Battery Charger

amp. As the voltage across R6 decreases below the voltage across R2, the output of the LM101A goes low shunting R1 with R4. This decreases the output voltage from 14.5V to about 12.5V terminating the charging. Transistor Q1 then lights the LED as a visual indication of full charge.

The LM117 can even be used as a peak clipping AC voltage regulator. Two regulators are used, 1 for each polarity of the input as shown in *Figure 12*. Internal to the LM117 is a diode from input-to-output which conducts the current around the device when the opposite regulator is active. Since each regulator is operating independently, the positive and negative peaks must be set separately for a symmetrical output.

CONCLUSIONS

A new IC power voltage regulator has been developed which is significantly more versatile than older devices. The output voltage is adjustable, in addition to improved regulation specifications. Further, reliability is increased in 2 fashions. Overload protection circuitry has been improved to make the device less susceptable to fault conditions and under short circuit conditions, minimum stress is transmitted back to the input power supply. Secondly, the device is 100% burned-in under short circuit conditions at the time of manufacture. Finally, the LM117 is made with a standard IC production process and packaged in a standard TO-3 power package, keeping costs low.

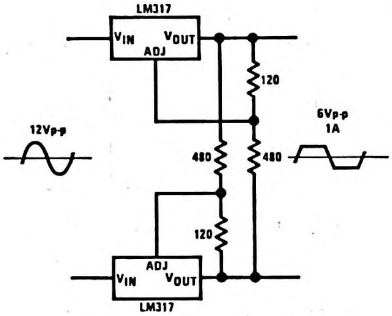


FIGURE 12. AC Voltage Regulator

Improving Power Supply Reliability with IC Power Regulators

National Semiconductor
Application Note 182
Robert C. Dobkin
April 1977

Three-terminal IC power regulators include on-chip overload protection against virtually any normal fault condition. Current limiting protects against short circuits fusing the aluminum interconnects on the chip. Safe-area protection decreases the available output current at high input voltages to insure that the internal power transistor operates within its safe area. Finally, thermal overload protection turns off the regulator at chip temperatures of about 170°C, preventing destruction due to excessive heating. Even though the IC is fully protected against normal overloads, careful design must be used to insure reliable operation in the system.

SHORT CIRCUITS CAN OVERLOAD THE INPUT

The IC is protected against short circuits, but the value of the on-chip current limit can overload the input rectifiers or transformer. The on-chip current limit is usually set by the manufacturer so that with worst-case production variations and operating temperature the device will still provide rated output current. Older types of regulators, such as the LM309, LM340 or LM7800 can have current limits of 3 times their rated output current.

The current limit circuitry in these devices uses the turn-on voltage of an emitter-base junction of a transistor to set the current limit. The temperature coefficient of this junction combined with the temperature coefficient of the internal resistors gives the current limit a −0.5%/°C temperature coefficient. Since devices must operate and provide rated current at 150°C, the 25°C current limit is 120% higher than typical. Production variations will add another ±20% to initial current limit tolerance so a typical 1A part may have a 3A current limit at 25°C. This magnitude of overload current can blow the input transformer or rectifiers if not considered in the initial design—even though it does not damage the IC.

One way around this problem (other than fuses) is by the use of minimum size heat sinks. The heat sink is designed for only normal operation. Under overload conditions, the device (and heat sink) are allowed to heat up to the thermal shut-down temperature. When the device shuts down, loading on the input is reduced.

Newer regulators have improved current limiting circuitry. Devices like the LM117 adjustable regulator, LM123 3A, 5V logic regulator or the LM120 negative regulators have a relatively temperature-stable current limit. Typically these devices hold the current limit within ±10% over the full −55°C to +150°C operating range. A device rated for 1.5A output will typically have a 2.2A current limit, greatly easing the problem of input overloads.

Many of the older IC regulators can oscillate when in current limit. This does not hurt the regulator and is mostly dependent upon input bypassing capacitors. Since there is a large variability between regulator types and manufacturers, there is no single solution to eliminating oscillations. Generally, if oscillations cause other circuit problems, either a solid tantalum input capacitor or a solid tantalum in series with 5Ω to 10Ω will cure the problem. If one doesn't work, try the other.

Start-up problems can occur from the current limit circuitry too. At high input-output differentials, the current limit is decreased by the safe-area protection. In most regulators the decrease is linear, and at input-output voltages of about 30V the output current can decrease to zero. Normally this causes no problem since, when the regulator is initially powered, the output increases as the input increases. If such a regulator is running with, for example, 30V input and 15V output and the output is momentarily shorted, the input-output differential increases to 30V and available output current is zero. Then the output of the regulator stays at zero even if the short is removed. Of course, if the input is turned OFF, then ON, the regulator will come up to operating voltage again. The LM117 is the only regulator which is designed with a new safe-area protection circuit so output current does not decrease to zero, even at 40V differential.

This type of start-up problem is particularly load dependent. Loads to a separate negative supply or constant-current devices are among the worst. Another, usually overlooked, load is pilot lights. Incandescent bulbs draw 8 times as much current when cold as when operating. This severely adds to the load on a regulator, and may prevent turn-on. About the only solutions are to use an LM117 type device, or bypass the regulator with a resistor from input to output to supply some start-up current to the load. Resistor bypassing will not degrade regulation if, under worst-case conditions of maximum input voltage and minimum load current, the regulator is still delivering output current rather than absorbing current from the resistor. *Figure 1* shows the output current of several different regulators as a function of output voltage and temperature.

When a positive regulator (except for the LM117) is loaded to a negative supply, the problem of start-up can be doubly bad. First, there is the problem of the safe-area protection as mentioned earlier. Secondly, the internal circuitry cannot supply much output current when the output pin is driven more negative than the ground pin of the regulator. Even with low input voltages, some positive regulators will not start when loaded by 50 mA to a negative supply. Clamping the output to ground with a germanium or Schottky diode usually solves this problem. Negative regulators, because of different internal circuitry, do not suffer from this problem.

DIODES PROTECT AGAINST CAPACITOR DISCHARGE

It is well recognized that improper connections to a 3-terminal regulator will cause its destruction. Wrong polarity inputs or driving current into the output (such as a short between a 5V and 15V supply) can force high currents through small area junctions in the IC, destroying them. However, improper polarities can be applied accidently under many normal operating conditions, and the transient condition is often gone before it is recognized.

Perhaps the most likely sources of transients are external capacitors used with regulators. *Figure 2* shows the discharge path for different capacitors used with a positive regulator. Input capacitance, C1, will not cause a problem under any conditions. Capacitance on the ground pin (or adjustment pin in the case of the LM117) can discharge through 2 paths which have low current junctions.

If the output is shorted, C2 will discharge through the ground pin, possibly damaging the regulator. A reverse-biased diode, D2, diverts the current around the regulator, protecting it. If the input is shorted, C3 can discharge through the output pin, again damaging the regulator. Diode D1 protects against C3, preventing damage. Also, with both D1 and D2 in the circuit, when the input is shorted, C2 is discharged through both diodes, rather than the ground pin.

In general, these protective diodes are a good idea on all positive regulators. At higher output voltages, they become more important since the energy stored in the capacitors is larger. With negative regulators and the LM117, there is an internal diode in parallel with D1 from output-to-input, eliminating the need for an external diode if the output capacitor is less than 25 μF.

Another transient condition which has been shown to cause problems is momentary loss of the ground connection. This charges the output capacitor to the unregulated input voltage minus a 1–2V drop across the regulator. If the ground is then connected, the output capacitor, C3, discharges through the regulator output to the ground pin, destroying it. In most cases, this problem occurs when a regulator (or card) is plugged into a powered system and the input pin is connected

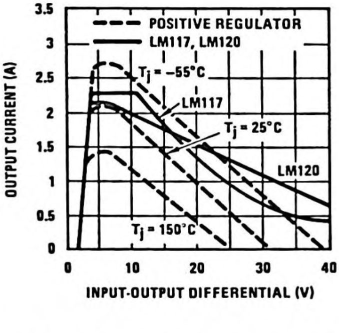


FIGURE 1. Comparison of LM117 Current Limit with Older Positive Regulator

before the ground. Control of the connector configuration, such as using 2 ground pins to insure ground is connected first, is the best way of preventing this problem. Electrical protection is cumbersome. About the only way to protect the regulator electrically is to make D2 a power zener 1V to 2V above the regulator voltage and include 10Ω to 50Ω in the ground lead to limit the current.

LOW OPERATING TEMPERATURE INCREASES LIFE

Like any semiconductor circuit, lower operating temperature improves reliability. Operating life decreases at high junction temperatures. Although many regulators are rated to meet specifications at 150°C, it is not a good idea to design for continuous operation at that temperature. A reasonable maximum operating temperature would be 100°C for epoxy packaged devices and 125°C for hermetically sealed (TO-3) devices. Of course, the lower the better, and decreasing the above temperatures by 25°C for normal operation is still reasonable.

Another benefit of lowered operating temperatures is improved power cycle life for low cost soft soldered packages. Many of today's power devices (transistors included) are assembled using a TO-220 or TO-3 aluminum soft solder system. With temperature excursions, the solder work-hardens and with enough cycles the solder will ultimately fail. The larger the temperature change, the sooner failure will occur. Failures can start at about 5000 cycles with a 100°C temperature excursion. This necessitates, for example, either a large heat sink or a regulator assembled with a hard solder, such as steel packages, for equipment that is continuously cycled ON and OFF.

THERMAL LIMITING GIVES ABSOLUTE PROTECTION

Without thermal overload protection, the other protection circuitry will only protect against short term overloads. With thermal limiting, a regulator is not destroyed by long time short circuits, overloads at high temperatures or inadequate heat sinking. In fact, this overload protection makes the IC regulator tolerant of virtually any abuse, with the possible exception of high-voltage transients, which are usually filtered by the capacitors in most power supplies.

One problem with thermal limiting is testing. With a 3-terminal regulator, short-circuit protection and safe-area protection are easily measured electrically. For thermal limiting to operate properly, the electrical circuitry on the IC must function and the IC chip must be well die-attached to the package so there are no hot spots. About the only way to insure that thermal limiting works is to power the regulator, short the output, and let it cook. If the regulator still works after 5 minutes (or more) the thermal limit has protected the regulator.

This type of testing is time consuming and expensive for the manufacturer so it is not always done. Some regulators, such as the LM117, LM137, LM120 and LM123, do receive an electrical burn-in in thermal shutdown as part of their testing. This insures that the thermal limiting works as well as reducing infant mortality. If it is probable that a power supply will have overloads which cause the IC to thermally limit, testing the regulator is in order.

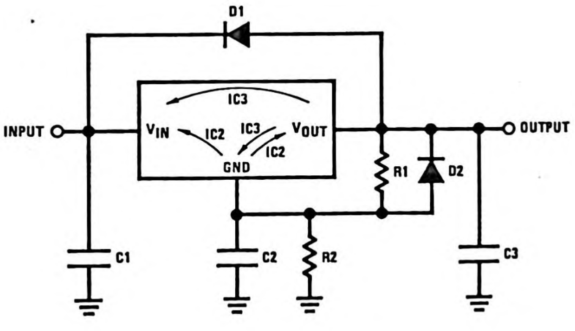


FIGURE 2. Positive Regulator with Diode Protection Against Transient Capacitor Discharge

References for A/D Converters

National Semiconductor
Application Note 184
Robert C. Dobkin
July 1977

Interfacing between digital and analog signals is becoming increasingly important with the proliferation of digital signal processing. System accuracy is often limited by the accuracy of the converter and a limitation of the converter is the voltage reference. Design can be difficaul if the reference is external.

The accuracy of any converter is limited by the temperature dirft or long term drift of the voltage reference, even if conversion linearity is perfect. Assuming that the voltage reference is allowed to add 1/2 least significant bit error (LSB) to the converter, it is surprising how good the reference must be when even small temperature excursions are considered. When temperature changes are large, the reference design is a major problem. Table I shows the reference requirements for different converters while Table II shows how the same problems exist with digital panel meters.

The voltage reference circuitry is required to do several functions to maintain a stable output. First, input power supply changes must be rejected by the reference circuitry. Secondly, the zener used in the reference must be biased properly, while other parts of circuitry scale the typical zener voltage and provides a low impedance output. Finally, the reference circuitry must reject ambient temperature changes so that the temperature drift of the reference circuitry plus the drift of the zener does not exceed the desired drift limit.

While zener temperature coefficient is obviously critical to reference performance, other sources of drift can easily add as much error as zener — even in voltage references with modest performance of 20 ppm/°C temperature drift. Zener drift and op amp drift add directly to the drift error, while resistor error is only a function of how well the scaling resistors track. Resistors which have a high TC can be used if they track.

For a 10V output with a 6.9V zener, the drift contribution of resistor mistracking is about 0.4 since the gain is 1.4. The range of temperature coefficient errors for different components used to make a 10V reference from a 6.9V zener are shown in Table III. Another potential source of error, input supply variations, are negligible if the input is 1% regulated, and the resistor feeding the zener is stable to 1%.

Less frequently specified sources of error in voltage reference zeners are hysteresis and stress sensitivity. Stress on either a zener-diode junction or the series-temperature-compensating junction will cause voltage shifts. The axial leads on discrete devices can transmit stress from outside the package to the junction, causing 1 mV to 5 mV shifts.

Temperature cycling the discrete zener can also induce non-reversible changes in zener voltage. If a zener is heated from 25°C to 100°C and then back to 25°C, the zener voltage may not return to its original value. This is because the temperature cycle has permanently changed the stress in the die, changing the voltage. This effect can be as high as 5 mV in some diodes and may be cumulative with many temperature cycles. The new planar IC zeners, such as the LM199 (temperature stabilized) or the LM129 are insensitive to stress and show only about 50 μV of hysteresis for a 150°C temperature cycle since the package does not stress the silicon chip.

DESIGNING THE REFERENCE

If moderate temperature performance such as 20 ppm/°C is all that is needed, 2 different approaches can be used in the reference design. In the first, the temperature drift error is split equally between the zener and the amplifier or scaling resistors. This requires a moderately low drift zener and op amp with 10 ppm resistors.

TABLE I. Maximum Allowable Reference Drift for 1/2 Least Significant Bits Error of Binary Coded Converter

TEMP CHANGE	BITS					
	6	8	10	12	14	
25°C	310	80	20	5	1.25	ppm/°C
50°C	160	40	10	2.5	0.6	ppm/°C
100°C	80	20	5	1.2	0.3	ppm/°C
125°C	63	16	3	1	0.2	ppm/°C

TABLE II. Maximum Allowable Reference Drift for 1/2 Digit Error of Digital Meters

TEMP CHANGE	DIGITS								
	2	2 1/2	3	3 1/2	4	4 1/2	5	5 1/2	
25°C	200	100	20	10	2	1	0.2	0.1	ppm/°C
5°C			100	50	10	5	1	0.5	ppm/°C

*0.01%/°C = 100 ppm/°C, 0.001%/°C = 10 ppm/°C, 0.0001%/°C = 1 ppm/°C

TABLE III. Drift Error Contribution From Reference Components for a 10V Reference

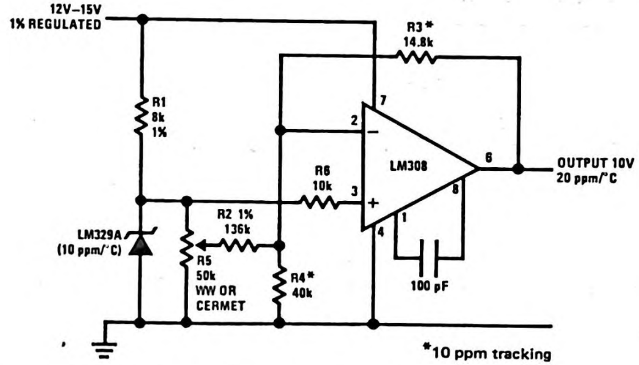
DEVICE	ERROR	10V OUTPUT DRIFT
Zener	**Zener Drift**	
LM199A	0.5 ppm/°C	0.5 ppm/°C
LM199, LM399A	1 ppm/°C	1 ppm/°C
LM399	2 ppm/°C	2 ppm/°C
1N829, LM3999	5 ppm/°C	5 ppm/°C
LM129, 1N823A, 1N827A, LM329A	10–50 ppm/°C	10–50 ppm/°C
LM329, 1N821, 1N825	20–100 ppm/°C	20–100 ppm/°C
Op Amp	**Offset Voltage Drift**	
LM725, LH0044, LM121	1 μV/°C	0.15 ppm/°C
LM108A, LM208A, LM308A	5 μV/°C	0.7 ppm/°C
LM741, LM101A	15 μV/°C	2 ppm/°C
LM741C, LM301A, LM308	30 μV/°C	4 ppm/°C
Resistors	**Resistance Ratio Drift**	
1% (RN55D)	50–100 ppm	20–40 ppm/°C
0.1% (Wirewound)	5–10	2–4 ppm
Tracking 1 ppm Film or Wirewound	—	0.4 ppm/°C

The second approach uses a very low drift zener and allows the buffer amplifier or scaling resistor to cause most of the drift error. This type of design is now made economical by the availability of low cost temperature stabilized IC zeners with virtually no TC. Further, the temperature coefficient of this reference is easily upgraded, if necessary. The 2 reference circuits are shown in *Figure 1a and Figure 1b.*

In *Figure 1a*, an LM308 op amp is used to increase the typical zener output to 10V while adding a worst-case drift of 4 ppm/°C to the 10 ppm/°C of the zener. Resistors R3 and R4 should track to better than 10 ppm bringing the total error so far to 18 ppm. Since the output must be adjusted to eliminate the initial zener tolerance, a pot, R5 and R2 have been added. The loading on the pot by R2 is small, and there is no tracking requirement between the pot and R2. It is necessary for R2 to track R3 and R4 within 50 ppm.

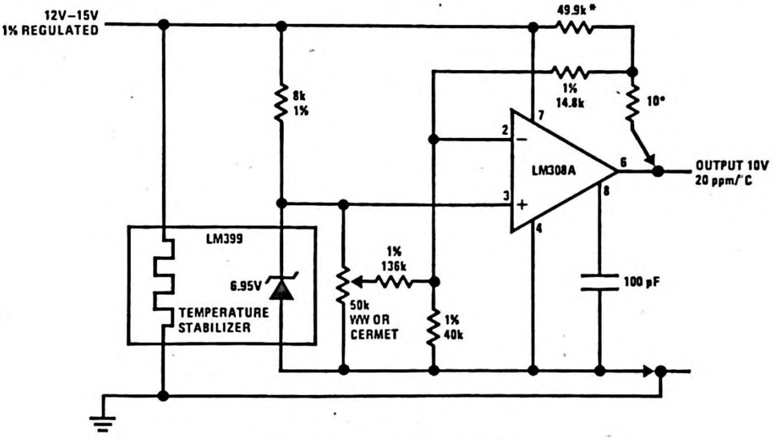
In *Figure 1b*, a low drift reference and op amp are used to give a total drift, exclusive of resistors of 3 ppm/°C. Now the resistor tracking requirement is relaxed to about 50 ppm, allowing ordinary 1% resistors to be used. The circuit in *Figure 1b* is modified easily for applications requiring 3 ppm/°C to 5 ppm/°C overall drift by tightening the tracking of the resistors. For more accurate applications, the Kelvin sensing for both output and ground should be used. For even lower drifts, substituting a 1 μV/°C op amp, 1 ppm tracking resistors and an LM199A zener, overall drifts of 1 ppm/°C can be achieved. In both of the circuits, it is important to remember that the tracking of resistors can, at worst-case, be twice temperature drift of either resistance.

In both circuits, the zener is biased by a single resistor from the supply, rather than from the reference output. This eliminates possible start-up problems and, because of the 1Ω dynamic impedance of the IC zeners, only



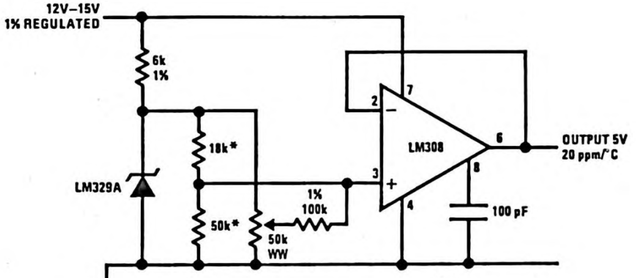
*10 ppm tracking

FIGURE 1a. 10V, 20 ppm Reference Using a Low Cost Zener and Low Drift Resistors


12V–15V
1% REGULATED
49.9k*
8k
1%
1%
14.8k
10*
7
2
6
LM308A
OUTPUT 10V
20 ppm/°C
3
8
4
LM399
1%
136k
6.95V
100 pF
TEMPERATURE
STABILIZER
50k
WW OR
CERMET
1%
40k

*Optional—improves line regulation

FIGURE 1b. 10V Reference has Low Drift Reference and Standard 1% Resistors. Kelvin Sensing is Shown with Compensation for Line Changes.


12V–15V
1% REGULATED
6k
1%
7
2
18k*
LM308
6
OUTPUT 5V
20 ppm/°C
3
8
LM329A
1%
100k
4
100 pF
50k*
50k
WW

*20 ppm tracking

FIGURE 2. Low Voltage Reference

adds about 20 μV of error. Compensation for input changes is shown in *Figure 1b*. Conventional zeners do not allow this biasing. A conventional 5 ppm reference such as the 1N829 has a dynamic impedance of about 15Ω. If it is biased from a resistor from a 1% regulated 15V supply, the operating current can change by 1.7% or 127 μA. This will shift the zener voltage by 1.9 mV or 60 ppm. With the IC zeners operating at 1 mA, a 1% shift in the supply will change the reference by 20 μV or 3 ppm. Further, power dissipation in the IC is only 7 mW, giving low warm-up drift compared to 7.5 mA zeners. The biasing resistor for the IC zener need not be any better than an ordinary 1% resistor since performance is independent of current.

When output voltages less than the zener voltage are desired, the IC zeners significantly simplify circuit design since no auxiliary regulator is needed for biasing. *Figure 2* shows a 5V reference circuit for use with a 15V input. In this case, zener drift contributes proportionally to the output drift while op amp offset drift adds a greater rate. With the 10V reference, 15 μV/°C from the op amp contributed 2 ppm/°C drift, but for the 5V reference, 15 μV/°C adds 3 ppm/°C. This makes op amp choice more important as the output voltage is lowered. Of course, if a high output impedance is tolerable, the op amp can be eliminated.

APPROACHING THE ULTIMATE DRIFT

To obtain the lowest possible drifts, temperature coefficient trimming is necessary. With discrete zeners, the operating current can sometimes be trimmed to change the TC of the reference; however, the temperature coefficient is not always linear or predictable. With the new IC zeners, TC is independent of operating current so trimming must be done elsewhere in the circuit. The lowest drift components should be used since

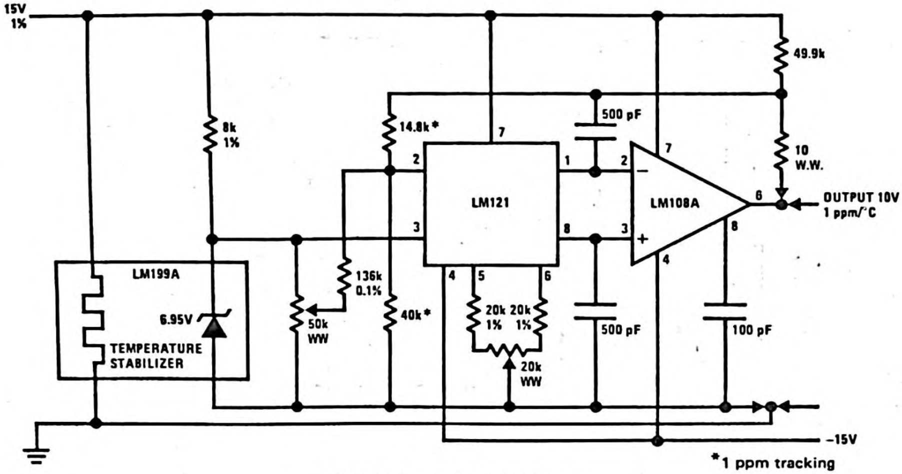


FIGURE 3. Ultra Low Drift Reference

trimming can only remove a linear component of drift. High TC devices can have a highly non-linear drift, making trimming difficult.

Figure 3 shows a circuit suitable for trimming. An LM199A reference with 0.5 ppm/°C drift is used with a 121/108 op amp. Resistors should be 1 ppm tracking to give overall untrimmed drifts of about 0.9 ppm. The 121/108 is a low drift amplifier combination where drift is predictably proportional to offset voltage. An offset can be set for the 108/121 combination to cancel the measured drift with 1 pass calibration.

Trimming procedure is as follows: the zener is disconnected and the input of the op amp grounded. Then the offset of the op amp is nulled out to zero. Reconnecting the zener, the output is adjusted to precisely 10V. A temperature run is made and the drift noted. The op amp will drift 3.6 μV/°C for every 1 mV of offset, so for every 5 μV/°C drift at the output, the offset of the op amp is adjusted 1 mV (1.4 mV measured at the output) in the opposite direction. The output is readjusted to 10V and the drift checked.

Although this trimming scheme was chosen since only a single adjustment is usually required, compensation is not always perfect. Hysteresis effects can appear in resistors or op amps as well as zeners. Best results can be obtained by cycling the circuit to temperature a few times before taking data to relieve assembly stresses on the components. Also, oven testing can sometimes cause thermal gradients across circuits, giving 50 μV to 100 μV of error. However, with careful layout and trimming, overall reference drifts of 0.1 ppm/°C to 0.2 ppm/°C can be achieved.

There are 2 other possible problem areas to be considered before final layout. Good single point grounding is important. Traces on a PC board can easily have 0.1Ω and only 10 mA will cause a 1 mV shift. Also, since these references are close to high-speed digital circuitry, shielding may be necessary to prevent pick-up at the inputs of the op amp. Transient response to pick-up or rapid loading changes can sometimes be improved by a large capacitor (1 μF–10 μF) directly on the op amp output; but this will depend on the stability of the op amp.

12-Bit Analog/Digital-Digital/Analog Conversion Card for SC/MP

National Semiconductor
Application Note 192
Milt Schwartz and Doug Hall
October 1977

This application note presents a one-card solution for Analog-to-Digital and Digital-to-Analog (A/D—D/A) converter circuits for SC/MP. This card is intended for general-purpose breadboarding and demonstrates 12-bit capability. Under direct control of SC/MP, an 8-bit microprocessor, 12 bits of precision are achieved by time-multiplexing data on the SC/MP Data Bus. The A/D—D/A circuit is designed to interface with a user-supplied SC/MP system using the SC/MP Control Signals, Data Bus, and Address Bus as shown in figure 1.

The A/D—D/A circuit contains an Address and Order Decode section for decoding the board address and generating the various control signals required by the A/D—D/A converters. Analog input and output to the circuit is via eight analog input channels and four dual analog output channels (expandable to 8). The A/D input channels are selectable under direct software control thus enabling the selection of one particular input channel for conversion or the scanning of two or more input channels for conversion. The D/A output channels are automatically refreshed by an on-board read/write memory (RAM), with each output consisting of a voltage source and a current source. Additionally, the digital data stored in the on-board RAM is available for output onto the SC/MP Data Bus. A more detailed description of the A/D—D/A converter circuit is contained in the Functional Description.

As designed and programmed in this application, the A/D circuit can typically accept analog data for input at an average rate of approximately 3000 channels per second. Since input sampling is directly dependent upon which SC/MP is used (P-channel or N-channel) and the programming technique used, how the program is written can directly affect the sampling rate. Sampling the analog data input is typically 25% faster when using in-line code* as opposed to using subroutine calls. The trade-off, of course, is the increase in program space requirements. A breakdown of typical A/D sampling rates is contained in Table 1.

The delay time of the D/A circuit is also dependent upon which SC/MP chip is used and the programming technique used (in-line or subroutine). The output delay time that exists between calling digital data from the system memory to outputting the analog data to any particular channel is contained in Table 2. The rates and times shown in Table 1 and Table 2, respectively, are for the program examples shown in this application note. If any tighter code can be written for the input or output routines, the throughput times will decrease correspondingly.

To implement this circuit, all components (with the exception of the SC/MP System) were breadboarded on two wire-wrap prototyping cards (IPC-16P/801) stacked end-to-end. Stacking the boards end-to-end provided two 72-pin edge connections, one for the SC/MP System and one for the analog input and output channels.

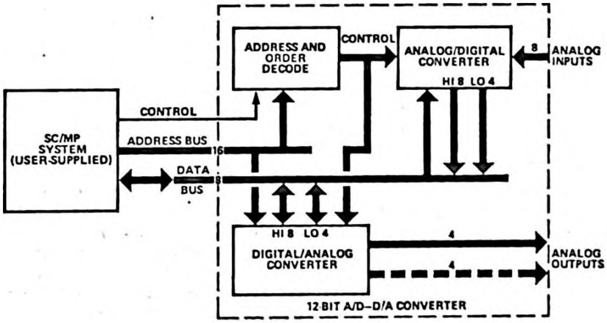


Figure 1. SC/MP and A/D—D/A Functional Block Diagram

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*Code written so that each individual sample is sequentially taken using its own block of code within the body of the main program.

Table 1. Typical A/D Sample Rates

In-Line Code		Subroutine Call	
P-Channel SC/MP	N-Channel SC/MP	P-Channel SC/MP	N-Channel SC/MP
≈2500 Channels/sec.	≈5000 Channels/sec.	≈2000 Channels/sec.	≈4000 Channels/sec.

Table 2. Typical D/A Delay Times

P-Channel SC/MP	N-Channel SC/MP
170 μs	85 μs

Table 3. A/D Address Requirements

	Desired Function	SC/MP Address Bus					
		15 ↔ 5	4	3	2	1	0
1	Select Analog Inputs* (using Store Instruction) Read Digital Output from A/D Converter	Board Address	0	X	0	0	0
2	Enable A/D Sample & Hold		0	X	1	0	0
3	Hold A/D Sample & Hold		0	X	1	0	1
4	Start A/D Conversion		0	X	0	1	1
5	Select Hi 8 Data Bits		0	X	0	0	1
6	Select Lo 4 Data Bits		0	X	0	1	0

1 = Sequence of execution

X = Don't Care

* = Data bits determine input channel selection (see Table 4)

GENERAL USE

Since all A/D–D/A conversion is performed under software control, conversion routines (or subroutines) must be a component part of any software written to process A/D–D/A data using this circuit. No matter whether it is desired to select one particular analog input or to scan from two to eight inputs, it is a simple matter to change back and forth by simply modifying the channel selector in the conversion routine.

The analog outputs are multiplexed and sequentially refreshed under hardware control and therefore are not individually selectable. What this means is, that if only one output channel is needed at any particular time, the analog outputs on the other channels can be ignored. Clearing the on-board RAM will cause each output to go to zero, otherwise the outputs will reflect whatever value is stored in RAM.

The 11 high-order address bits (ADR5 through ADR15) are compared to the on-board address switches to determine board addressing. Since address bits ADR0 through ADR4 are not decoded for addressing purposes, the board occupies 32 consecutive locations in the SC/MP system memory. However, address bits ADR0 through ADR4 are decoded by the order decoder to select the various functions to be performed by the A/D–D/A converters. The A/D address requirements are in Table 3 and the A/D input channel selection requirements are in Table 4. The D/A input address requirements are in Table 5.

Table 4. A/D Input Channel Selection Requirements

Input Channel	SC/MP Data Bus			
	7 – 3	2	1	0
1	X	0	0	0
2	X	0	0	1
3	X	0	1	0
4	X	0	1	1
5	X	1	0	0
6	X	1	0	1
7	X	1	1	0
8	X	1	1	1

X = Don't Care

Table 5. D/A Input Address Requirements

Desired Function	SC/MP Address Bus						NWDS	NRDS
	15 ↔ 5	4	3	2	1	0		
Read from Hi 8 bits of On-Board RAM to Data Bus	Board	1	0	n	n	n	0	1
Read from Lo 4 bits of On-Board RAM to Data Bus	Address	1	1	n	n	n	0	1
Write to Hi 8 bits of On-Board RAM from Data Bus		1	0	n	n	n	1	0
Write to Lo 4 bits of On-Board RAM from Data Bus		1	1	n	n	n	1	0
Refresh Analog Outputs	x	0	x	x	x	x	x	x
or								
Refresh Analog Outputs	Not Selected	x	x	x	x	x	x	x

x = Don't Care

n = One of eight RAM channel locations selected. Note that for each channel, the Hi 8 and Lo 4 lower 3 address bits must be the same.

INPUT/OUTPUT SPECIFICATIONS

The I/O specifications pertaining to voltage and current are the only ones presented in this application note. Any reference to the individual device specifications should be taken from the appropriate National Semiconductor Data Book. The input and output voltage and current specifications for each channel are contained in Table 6.

Table 6. Input/Output Specifications

Input Channels	Output Channels
0 V - 10 V	0 V - 10 V or 4 mA - 20 mA

NOTE

All inputs and outputs referenced to A/D-D/A circuit ground.

Due to the value of the precision voltage reference used in this application, the input voltage specifications are fixed at a maximum of +10 volts. For this application, the current source output was designed to operate using the +15-volt supply as the +V supply shown in figure 2. The current source output is, however, able to operate at voltages higher than +15 volts due to the open-collector output transistor. The current source voltage must, of course, be within the specifications of the output transistor. Figure 2 illustrates the current source output load configuration.

To calculate minimum load

$$R_L = \frac{(+V) - V_1}{20\text{ mA}}$$

The two examples in the following sections are typical of the programs that can be written for the A/D–D/A circuit. Each program has been written to utilize only one section of the A/D–D/A circuit so as to present a simplified view of the two conversion operations.

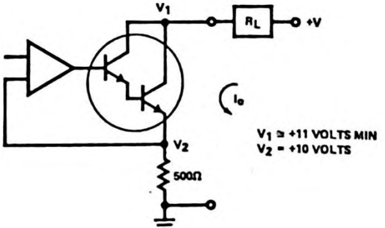


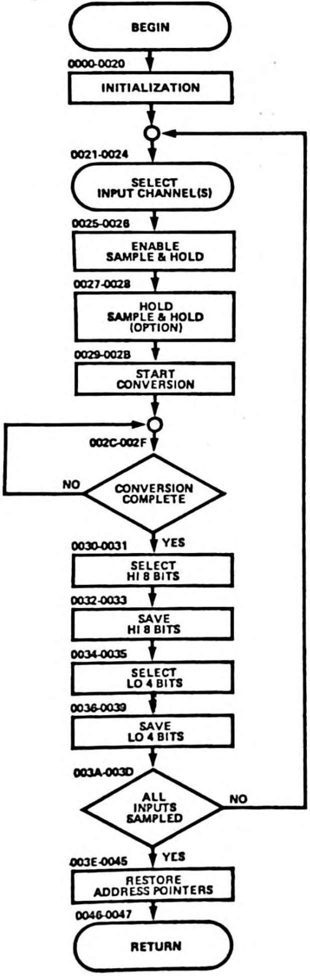
Figure 2. Current Source Output Configuration

ANALOG-TO-DIGITAL USE

In Table 3, each of the six functions that constitute one A/D conversion is preceded by a number which indicates the position of that function in the A/D conversion process. In general use, the program must select an input channel for conversion and then enable the sample and hold device (S & H) to sample the input data. The program must then disable the S/H device and hold the analog input (via the S/H device) while the A/D converter converts the analog input to its digital equivalent. Once conversion is complete, the data can be stored into two consecutive locations in the SC/MP System RAM (Hi 8 bits followed by the Lo 4 bits) for future processing. Refer to the functional description for more detailed information.

The A/D program following this section scans all eight of the analog inputs and stores the 12-bit digital results into the SC/MP system RAM. A flowchart and conversion program illustrating the sequence of operation when performing A/D conversions are illustrated in figure 3 and figure 4, respectively.

The SC/MP system RAM locations used for data storage are listed in the program listing in figure 4.


BEGIN
0000-0020
INITIALIZATION
0021-0024
SELECT INPUT CHANNEL(S)
0025-0026
ENABLE SAMPLE & HOLD
0027-0028
HOLD SAMPLE & HOLD (OPTION)
0029-002B
START CONVERSION
002C-002F
NO
CONVERSION COMPLETE
YES
0030-0031
SELECT HI 8 BITS
0032-0033
SAVE HI 8 BITS
0034-0035
SELECT LO 4 BITS
0036-0039
SAVE LO 4 BITS
003A-003D
ALL INPUTS SAMPLED
NO
YES
003E-0045
RESTORE ADDRESS POINTERS
0046-0047
RETURN

Set pointers; address A/D—D/A card; and set up input channel selection.

One of the eight analog input signals is selected using the data from Table 4.

The Sample & Hold circuit must be enabled for a minimum of 30 µs in order to sample the analog input signal (with 0.01% accuracy).

The Hold Sample & Hold circuitry allows the user to retain any particular input that has just been sampled (held voltage will degrade at the rate of 4 microvolts per millisecond).

Once the input has been sampled (and held) the Start Conversion Signal allows the A/D converter to begin conversion.

Once the A/D converter completes the conversion process, the Conversion Complete Signal signals SC/MP that conversion is complete. The digital data will remain latched in the A/D Converter until a new Start Conversion Signal is generated.

Upon receipt of the Conversion Complete Signal, SC/MP selects the Hi 8 bits output by the A/D converter and outputs them onto the SC/MP Data Bus.

SC/MP stores the Hi 8 bits into the system memory for future processing.

SC/MP selects the Lo 4 bits output by the A/D converter and outputs them onto the SC/MP Data Bus.

SC/MP stores the Lo 4 bits into the system memory for future processing.

Test to see if all of the analog inputs have been sampled.

The user's address pointer is restored from RAM.

Return to user's routine to process converted analog data.

Figure 3. A/D Sample Program Flowchart

```
SC/MP ASSEMBLER REV-A
MAINPR

                    ;SUBROUTINE CALL TO A/D CONVERTER ON AD/DA CARD.
                    ;THIS SUBROUTINE SCANS ALL 8 ANALOG INPUT CHANNELS
                    ;AND STORES THE 12 BIT RESULTS (HI 8 AND LO 4) IN
                    ;CONSECUTIVE LOCATIONS IN USERS RAM.  THEREFORE,
                    ;16 LOCATIONS MUST BE RESERVED FOR THE DATA.
                    ;POINTER 1 IS USED AS THE CALLING POINTER, WHILE POINTER 2
                    ;IS MAINTAINED AS THE USERS RAM POINTER.
                    ;IN ADDITION, 4 LOCATIONS IN USER RAM MUST BE RESERVED
                    ;FOR BOOK-KEEPING.  FOR THIS EXAMPLE, THE BASE ADDRESS OF THE
                    ;AD/DA CARD IS X'8000.  SENSE A IS USED TO TEST THE
                    ;CONVERESION COMPLETE SIGNAL FROM THE A/D CONVERTER.
                    ;IN THIS EXAMPLE SENSE A IS SCANNED, BUT AN INTERRUPT COULD
                    ;BE USED INSTEAD.



     0017                LCNT  = X'17          ;LOOP COUNTER LOCATION
                                               ;FOR A/D SUBROUTINE
     0018                CHSEL = X'18          ;A/D CHANNEL SELECTOR
     0019                HSAV1 = X'19          ;TEMP.  STORAGE FOR PTR 1 HI
     001A                LSAV1 = X'1A          ;TEMP.  STORAGE FOR PTR 1 LO


                      ;USER RAM FOR STORING 8 CHANNELS OF 12 BIT DATA

                         ;LOCATION X'1000 = CHANNEL 1 HI 8 BITS
                         ;LOCATION X'1001 = CHANNEL 1 LO 4 BITS

                         ;LOCATION X'1002 = CHANNEL 2 HI 8 BITS
                         ;LOCATION X'1003 = CHANNEL 2 LO 4 BITS

                         ;LOCATION X'1004 = CHANNEL 3 HI 8 BITS
                         ;LOCATION X'1005 = CHANNEL 3 LO 4 BITS

                         ;LOCATION X'1006 = CHANNEL 4 HI 8 BITS
                         ;LOCATION X'1007 = CHANNEL 4 LO 4 BITS

                         ;LOCATION X'1008 = CHANNEL 5 HI 8 BITS
                         ;LOCATION X'1009 = CHANNEL 5 LO 4 BITS

                         ;LOCATION X'100A = CHANNEL 6 HI 8 BITS
                         ;LOCATION X'100B = CHANNEL 6 LO 4 BITS

                         ;LOCATION X'100C = CHANNEL 7 HI 8 BITS
                         ;LOCATION X'100D = CHANNEL 7 LO 4 BITS

                         ;LOCATION X'100E = CHANNEL 8 HI 8 BITS
                         ;LOCATION X'100F = CHANNEL 8 LO 4 BITS



                         ;TYPICAL USER PROGRAM

 0000 08        INIT:    NOP
 0001 C410               LDI     X'10
 0003 36                 XPAH    2
 0004 C400               LDI     0
 0006 32                 XPAL    2             ;PTR 2 NOW INITIALIZED
                                               ;AT X'1000 AS RAM PTR
                         ;
                         ;
                      ;**** USERS MAIN PROGRAM ****


                      ;**** USER PROGRAM NOW GETS READY TO CALL ****
                           ;A/D SUBROUTINE.
```

Figure 4. A/D Conversion Program

```

0007 C400               LDI     H(AD)          ;AD IS LABEL OF SUBROUTINE
0009 35                 XPAH    1
000A C40D               LDI     L(AD)-1
000C 31                 XPAL    1              ;POINTER 1 NOW LOADED
                                               ;WITH CORRECT ADDRESS
000D 3D                 XPPC    1              ;CALL AD SUBROUTINE
                        ;
                        ;
                      ;**** CONTINUE USER PROGRAM ****


000E 04        AD:      DINT                   ;DISABLE INTERRUPT
000F C480               LDI     X'80
0011 35                 XPAH    1              ;LOAD PTR 1 WITH HI ORDER
                                               ;ADDRESS OF AD-DA CARD
0012 CA19               ST      HSAV1(2)       ;SAVE OLD PTR 1
0014 C400               LDI     0
0016 31                 XPAL    1              ;LOAD PTR 1 WITH LO ORDER
                                               ;ADDRESS OF AD-DA CARD
0017 CA1A               ST      LSAV1(2)       ;SAVE OLD PTR 1 LO
0019 C408               LDI     8
001B CA17               ST      LCNT(2)        ;SET UP LOOP COUNTER
                                               ;FOR 8 CHANNEL READINGS
001D C4FF               LDI     X'FF
001F CA18               ST      CHSEL(2)       ;SET UP CHANNEL SELECTOR
0021 AA18      AGAIN:   ILD     CHSEL(2)       ;UPDATE TO SELECT CHANNEL
0023 C900               ST      (1)            ;SELECT INPUT CHANNEL
0025 C905               ST      5(1)           ;SAMPLE & HOLD SET TO SAMPLE
0027 C904               ST      4(1)           ;SAMPLE & HOLD SET TO HOLD
0029 C903               ST      3(1)           ;START AD CONVERTER
002B 06        TEST:    CSA
002C D410               ANI     X'10           ;SELECT SENSE A (CONVERSION
                                               ;COMPLETE SIGNAL).
002E 9CFB               JNZ     TEST           ;WAIT FOR CONVERSION COMPLETE
                                               ;TO GO LO
0030 C101               LD      1(1)           ;READ HI 8 BITS FROM A/D
0032 CE01               ST      @1(2)          ;SAVE HI 8 IN USER RAM
0034 C102               LD      2(1)           ;READ LO 4 BITS FROM A/D
0036 D40F               ANI     X'F            ;MASK TO SAVE LO 4
0038 CE01               ST      @1(2)          ;SAVE LO 4 BITS IN USER RAM
003A BA17               DLD     LCNT(2)
003C 9CE3               JNZ     AGAIN          ;WHEN 0, ALL 8 CHANNELS HAVE
                                               ;BEEN READ AND SAVED
003E C6F0               LD      @-16(2)        ;RESTORE PTR 2
0040 C219               LD      HSAV1(2)
0042 35                 XPAH    1
0043 C21A               LD      LSAV1(2)
0045 31                 XPAL    1              ;PTR 1 RESTORED FOR RETURN
0046 3D                 XPPC    1              ;RETURN TO USER PROGRAM



     0000               END


AD      000E     AGAIN  0021     CHSEL  0018     HSAV1  0019
INIT    0000 *   LCNT   0017     LSAV1  001A     TEST   002B

NO ERROR LINES
SOURCE CHECKSUM = 5971
INPUT FILE    1:ADDA.SRC
```

Figure 4. A/D Conversion Program (continued)

DIGITAL-TO-ANALOG USE

To convert a digital value into an analog output it is necessary to store the digital value into the on-board RAM. The digital value is then converted and output to one particular channel.

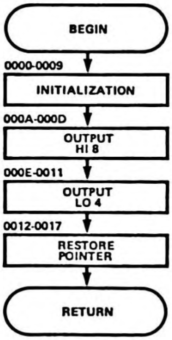
To store a digital value into the on-board RAM requires two sequential store (ST) instructions, one for the Hi 8 bits and one for the Lo 4 bits. Referring to Table 5 it can be seen that ADR0, ADR1, and ADR2 determine which channel (the location in on-board RAM) is to be written to (or read from). Address bit ADR3 determines whether it is the Hi 8 bits or Lo 4 bits that are written to or read from the on-board RAM. Address bit ADR4 selects the D/A converter. For this application, only four output channels were utilized although the circuit can be expanded to a total of eight outputs (complementing the eight inputs). With only four output channels this means that only the first four locations of on-board RAM storage can be used; this means ADR0 and ADR1 select the RAM channel location while ADR2 must be a logic zero ('0'). This is important because the analog outputs are refreshed by the hardware and if data is stored to a location that is not refreshed, then the data will never be seen at the outputs. For this implementation of the A/D—D/A circuit, the lower eight locations in the on-board RAM are cycled by the Address Generator.

Once data is written into the on-board RAM, the data can be read back out onto the SC/MP Data Bus by execcuting a Read Instruction. During data read or write operations, the output refresh is disabled and the outputs hold the last value output by the D/A converter.

Whenever ADR4 goes to a logic '0' or the board is not selected, the analog output is automatically refreshed by the circuit hardware. The auto-refresh circuit automatically steps through the first eight locations in RAM. Each output from RAM is synchronized so that the converted digital value is output on one particular channel. Since each output contains a Sample & Hold device, each analog output will continue to reflect the analog equivalent of the digital value in RAM until the value is modified.

Each channel contains a voltage source output and a current source output which are at common industrial levels to ease interfacing.

A flowchart and conversion program illustrating the sequence of operation when performing a single D/A conversion are illustrated in figure 5 and figure 6, respectively. The D/A program stores a 12-bit digital value into the A/D—D/A RAM and then outputs the analog equivalent to one channel.



The A/D—D/A card address is stored in the SC/MP pointers for address and order decoding and the user's program pointer is saved in RAM.

The Hi 8 bits of the digital value to be converted is output to the D/A converter and the output channel is then selected.

The Lo 4 bits of the digital value to be converted is output to the D/A converter and the output channel is then selected.

The user's address pointer is restored from RAM.

Return to user program.

Figure 5. D/A Sample Program Flowchart

```
SC/MP ASSEMBLER REV-A
MAINPR


 1            ;THIS PROGRAM OUTPUTS A 12 BIT DIGITAL
 2            ;VALUE TO ONE CHANNEL OF THE D/A CONVERTER.
 3            ;THIS EXAMPLE SHOWS HOW 3 VOLTS IS PRESENTED
 4            ;AT THE  CHANNEL 1 OUTPUT.
 5
 6            ;EACH VOLT IS APPROX. X'199, THEREFORE
 7            ;3 VOLTS IS APPROX. X'4CB
 8
 9                     ;POINTER 1 = CARD ADDRESS = X'8000
10                     ;POINTER 2 = USER RAM POINTER
11      0020       HSAV = X'20                ;RESERVED LOCATION IN
12                                            ;USER RAM. THIS COULD BE
13                                            ;ANY CONVENIENT LOCATION
14                                            ;AND IS ONLY SHOWN HERE TO
15                                            ;GET A CORRECT ASSEMBLY
16
17      0021       LSAV = X'21                ;SAME COMMENT AS FOR HSAV
18
19
20
21                     ;
22                     ;
23                ;**** USER PROGRAM ****
24
25                     ;BEGIN IN-LINE CODE TO D/A
26
27 0000 C480   OUTPUT: LDI     X'80
28 0002 35             XPAH    1
29 0003 CA20           ST      HSAV(2)           ;SAVE OLD PTR 1 HI
30 0005 C400           LDI     0
31 0007 31             XPAL    1                 ;PTR 1 = CARD ADDRESS
32 0008 CA21           ST      LSAV(2)           ;SAVE OLD PTR 1 LO
33 000A C44C           LDI     X'4C              ;GET HI 8 VALUE OF 3 VOLTS
34 000C C910           ST      X'10(1)           ;OUTPUT HI 8 TO CHANNEL 1
35 000E C40B           LDI     X'B               ;GET LO 4 VALUE OF 3 VOLTS
36 0010 C918           ST      X'18(1)           ;OUTPUT LO 4 TO CHANNEL 1
37 0012 C220           LD      HSAV(2)
38 0014 35             XPAH    1
39 0015 C221           LD      LSAV(2)
40 0017 31             XPAL    1                 ;PTR 1 RESTORED
41                     ;
42                     ;
43
44
45
46                ;**** CONTINUE USER PROGRAM ****
47
48
49
50
51                     ;NOTE:   TO SELECT THE REMAINING CHANNELS THE
52                     ;        DISPLACEMENT VALUE OF THE INSTRUCTIONS
53                     ;        AT LINES 34 AND 36 WOULD BE CHANGED
54                     ;        ACCORDING TO THE TABLE BELOW.
55
56
57
58
59            ;CHANNEL          DISPLACEMENT
60            ;                 HI 8  LO 4
61
62            ;    1            X'10  X'18
63            ;    2            X'11  X'19
64            ;    3            X'12  X'1A
65            ;    4            X'13  X'1B
66
67
68      0000            END

 HSAV   0020     LSAV   0021     OUTPUT 0000 *

 NO ERROR LINES
 SOURCE CHECKSUM = 570C
 INPUT FILE     1:DA.SRC
```

Figure 6. D/A Conversion Program

FUNCTIONAL DESCRIPTION

The A/D–D/A circuit can be separated into three functional blocks. These blocks are:

- The Address and Order Decode section
- The Analog-to-Digital conversion section
- The Digital-to-Analog conversion section

A more detailed functional block diagram of the A/D–D/A Converter is contained in figure 7. The block diagram serves two purposes: to provide a general idea of the flow of data and control signals within each block of the A/D–D/A Converter; and to provide a reference source for block-to-block interconnections when used in conjunction with the logic schematics. Detailed descriptions of each functional block within the A/D–D/A Converter follow.

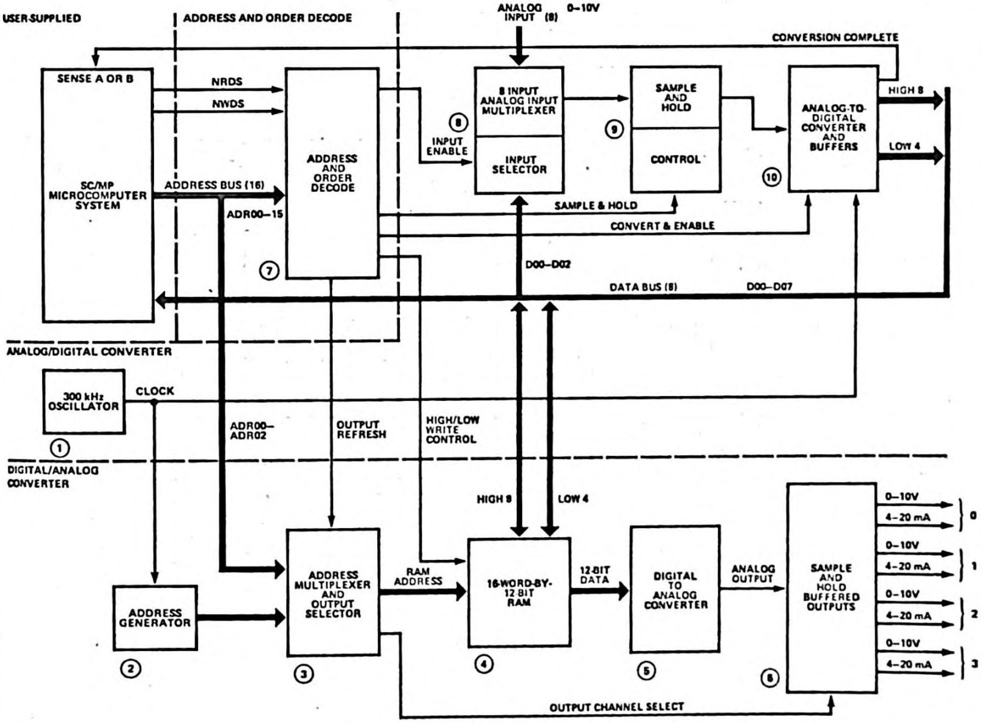
ADDRESS AND ORDER DECODE LOGIC

The Address and Order Decode section performs the functions that allow the A/D–D/A circuit to operate under software control from a SC/MP system. The on-board switches allow the user to create an 11-bit address code which is compared to the upper 11 bits of the address bus for determining the board location within the system memory. Once addressed correctly, the Address Decoder generates a Board Enable Signal for the Order Decode Logic. The Order Decode logic uses address bits ADR0 through ADR4, NRDS, and NWDS to create the various order functions detailed in Table 3 and Table 5. Of the five address bits, ADR4 selects either the A/D section or the D/A section of the converter circuit while ADR3 selects the Hi 8 bits or Lo 4 bits of on-board RAM when reading from or writing to the on-board RAM. Depending upon which mode of operation the A/D–D/A circuit is in, address bits ADR0, ADR1, and ADR2 generate either the various orders needed by the A/D circuit or the read/write addresses for the D/A circuit.

NOTE

> The MEMSEL* inverter is used only if using a SC/MP LCDS to operate the A/D–D/A circuit.

The Address and Order Decode logic schematic is illustrated in figure 8.



USER-SUPPLIED
ADDRESS AND ORDER DECODE
ANALOG INPUT (8)
0–10V
CONVERSION COMPLETE
SENSE A OR B
NRDS
NWDS
SC/MP MICROCOMPUTER SYSTEM
ADDRESS BUS (16)
ADR00–15
ADDRESS AND ORDER DECODE
⑦
⑧
INPUT ENABLE
8 INPUT ANALOG INPUT MULTIPLEXER
INPUT SELECTOR
⑨
SAMPLE AND HOLD
CONTROL
⑩
ANALOG-TO-DIGITAL CONVERTER AND BUFFERS
HIGH 8
LOW 4
SAMPLE & HOLD
CONVERT & ENABLE
D00–D02
DATA BUS (8)
D00–D07
ANALOG/DIGITAL CONVERTER
300 kHz OSCILLATOR
CLOCK
①
ADR00–ADR02
OUTPUT REFRESH
HIGH/LOW WRITE CONTROL
DIGITAL/ANALOG CONVERTER
HIGH 8
LOW 4
ADDRESS GENERATOR
②
ADDRESS MULTIPLEXER AND OUTPUT SELECTOR
③
RAM ADDRESS
16-WORD-BY-12 BIT RAM
④
12-BIT DATA
DIGITAL TO ANALOG CONVERTER
⑤
ANALOG OUTPUT
SAMPLE AND HOLD BUFFERED OUTPUTS
⑥
0–10V
4–20 mA
0
0–10V
4–20 mA
1
0–10V
4–20 mA
2
0–10V
4–20 mA
3
OUTPUT CHANNEL SELECT

Figure 7. A/D–D/A Converter Functional Block Diagram

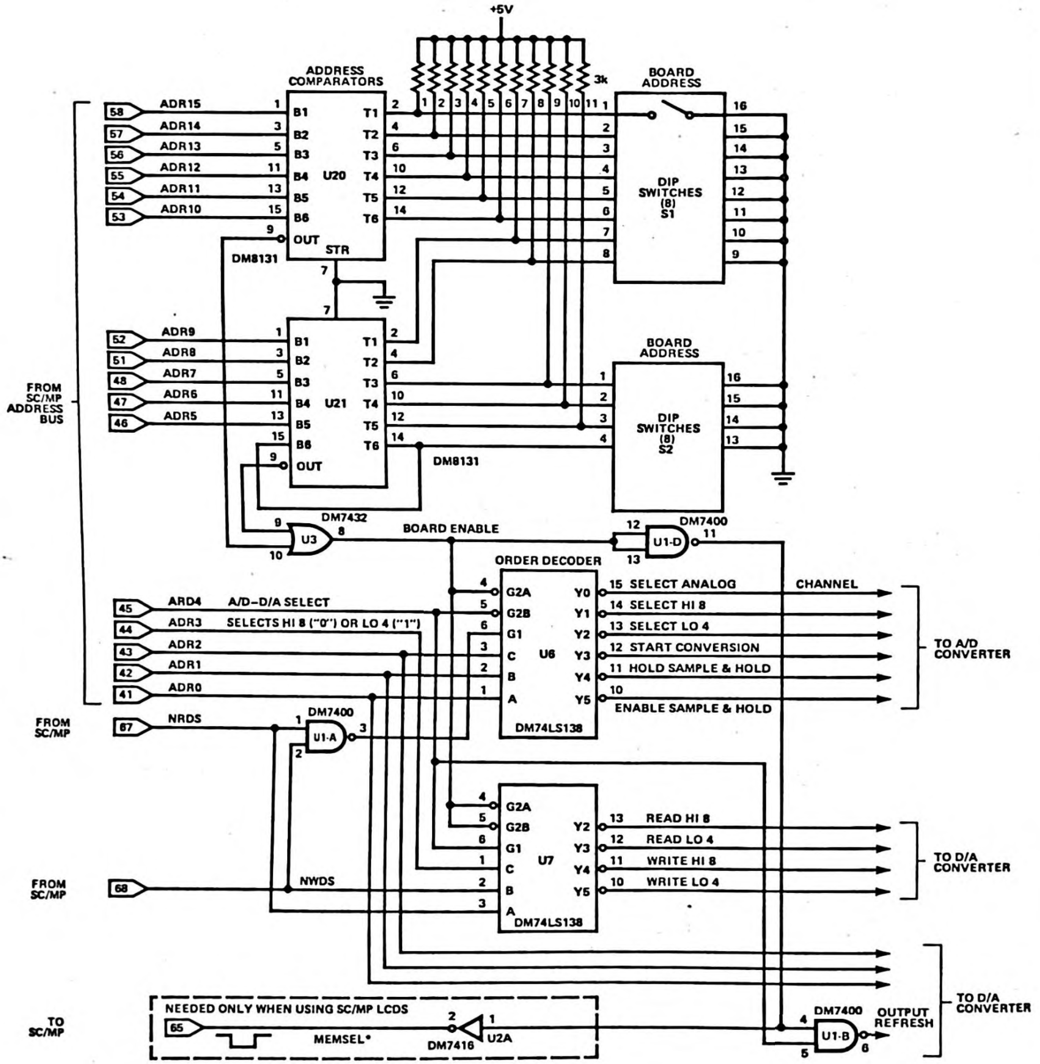

+5V
3k
ADDRESS COMPARATORS
BOARD ADDRESS
ADR15
ADR14
ADR13
ADR12
ADR11
ADR10
58
57
56
55
54
53
B1
B2
B3
B4
B5
B6
OUT
STR
T1
T2
T3
T4
T5
T6
U20
DM8131
DIP SWITCHES (8) S1
ADR9
ADR8
ADR7
ADR6
ADR5
52
51
48
47
46
U21
DM8131
BOARD ADDRESS
DIP SWITCHES (8) S2
FROM SC/MP ADDRESS BUS
DM7432
U3
BOARD ENABLE
DM7400
U1-D
ORDER DECODER
ARD4
A/D–D/A SELECT
ADR3
SELECTS HI 8 ("0") OR LO 4 ("1")
ADR2
ADR1
ADR0
45
44
43
42
41
G2A
G2B
G1
C
B
A
U6
Y0
Y1
Y2
Y3
Y4
Y5
DM74LS138
SELECT ANALOG
CHANNEL
SELECT HI 8
SELECT LO 4
START CONVERSION
HOLD SAMPLE & HOLD
ENABLE SAMPLE & HOLD
TO A/D CONVERTER
FROM SC/MP
67
NRDS
DM7400
U1-A
U7
READ HI 8
READ LO 4
WRITE HI 8
WRITE LO 4
TO D/A CONVERTER
FROM SC/MP
68
NWDS
TO D/A CONVERTER
NEEDED ONLY WHEN USING SC/MP LCDS
TO SC/MP
65
MEMSEL*
DM7416
U2A
DM7400
U1-B
OUTPUT REFRESH

Figure 8. Address and Order Decode

ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter consists of four functional logic blocks:

- The Analog Input Multiplexer
- The Sample and Hold Logic
- The Analog-to-Digital Converter and Buffers
- The Oscillator

The Analog Input Multiplexer selects one of eight analog inputs by latching the lower three data bits from the SC/MP Data Bus. The selected analog input is then passed through the Analog Multiplexer to the Sample-and-Hold device. The bit configurations necessary for the input channel selection are shown in Table 4. The selected analog input is sampled by the input Sample and Hold circuit upon receipt of the Enable Sample and Hold signal. The Enable Signal must be present for a minimum of 30 microseconds before disabling the Sample and Hold device (by generating the Hold Sample and Hold signal). The Hold Sample and Hold signal allows the Sample and Hold device to 'hold' the correct level for the Analog-to-Digital converter regardless of how the analog input may change.

Conversion of the analog input held at the input to the A/D converter begins upon receipt of the first low-to-high edge Clock pulse following the Start Conversion Signal.

The low-to-high transition (the leading edge) of the Conversion Complete Signal is used as feedback to remove the Start Conversion Signal. This feedback allows the A/D converter to begin conversion at the earliest possible moment since conversion will not actually begin until the Start Convert Signal is removed. The high-to-low transition (the trailing edge) of the Conversion Complete Signal signals SC/MP, via Sense A or Sense B, that conversion is complete and the digital equivalent to the analog input is ready at the output of the A/D converter.

NOTE

> A/D conversion is completed upon receipt of the Conversion Complete Signal *or* after 14 clock cycles of the on-board clock (approximately 60 μs).

The Level Shifters convert the voltage levels that are output by the A/D converter into the TTL levels for the SC/MP Data Bus. The converter data must be stored into RAM by a Load (LD) Instruction, followed by a Store (ST) Instruction. The first Load Instruction selects the data at the Hi 8 bit output buffers for storage into the system memory. The second Load Instruction selects the data at the Low 4 bit output buffers for storage into the next consecutive location in the system memory. All analog conversion in both the A/D and D/A section is performed using a precision (+10V ± 0.01V) reference source.

The Oscillator is a simple CMOS oscillator that generates a 300 kHz clock for the A/D converter and the D/A Address Generator.

The Analog-to-Digital Converter logic schematic is illustrated in figure 9.

DIGITAL-TO-ANALOG CONVERTER

The Digital-to-Analog Converter contains five functional logic blocks:

- The Address Multiplexer and Output Selector
- The Address Generator
- The 16-by-12 word RAM
- The Digital-to-Analog Converter
- The Sample and Hold Buffered Outputs

The Address Generator consists of two 4-bit binary counters that operate in series as a free-running counter to generate sequential addresses for the automatic output refresh mode.

The Address Multiplexer and Output Selector operates under control of the Order Decode Logic. Depending upon the state of the Output Refresh Signal, one of two functions are performed:

1. When Output Refresh is high, the D/A circuit is in the output refresh mode. The Output Selector is enabled and the Address Multiplexer passes addresses generated by the Address Generator. In this mode, the data in the on-board RAM are sequentially output to the D/A converter. At the same time, the Output Selector demultiplexer is enabled, thereby generating the output channel select signals for the Sample-and-Hold devices. The Channel Select signals are in synchronization with each of the corresponding channel data output by the on-board RAM. Being in synchronization causes the converted data output from each of the sequenced RAM channel locations to go to the channel's associated Output Channel Buffer. The analog level output by each of the Output Channel Buffers will be constantly refreshed and will stay constant until new data is written into the on-board RAM.

2. When the Output Refresh is low, the D/A circuit is in the read/write mode. The Address Multiplexer passes address bits ADR0, ADR1, and ADR2 through to the on-board RAM so each channel location can be accessed. At the same time the Output Selector is disabled so no output refresh occurs. Each output will, however, retain the last analog value output to the Sample-and-Hold devices. When writing to the on-board RAM from the SC/MP Data Bus, the Write Hi 8 function must be generated along with the address of the location to be written to. (See Table 5 for the address requirements.) The Write Lo 4 function must then follow the Write Hi 8 function (this is done using the same on-board RAM address as for the Write Hi 8 function). The operation to read from RAM onto the SC/MP Data Bus is performed in the same manner as for a write operation except that the address is modified to generate the Read function rather than the Write function.

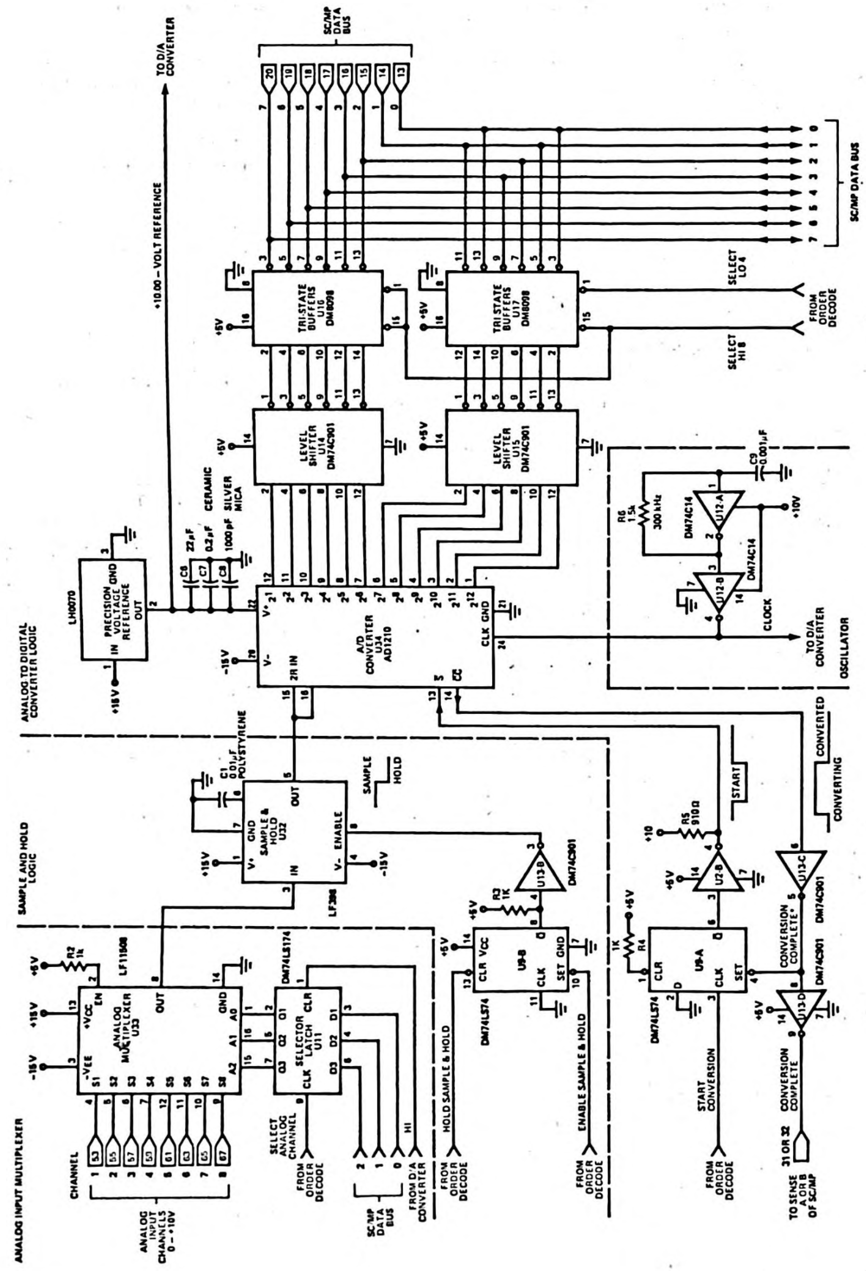

ANALOG INPUT MULTIPLEXER
SAMPLE AND HOLD LOGIC
ANALOG TO DIGITAL CONVERTER LOGIC
OSCILLATOR
ANALOG INPUT CHANNELS 0 – +10V
CHANNEL
ANALOG MULTIPLEXER U33
LF11508
SELECTOR LATCH U11
DM74LS174
SELECT ANALOG CHANNEL
FROM ORDER DECODE
SC/MP DATA BUS
FROM D/A CONVERTER
HOLD SAMPLE & HOLD
ENABLE SAMPLE & HOLD
SAMPLE & HOLD U32
LF398
C1 0.01µF POLYSTYRENE
SAMPLE
HOLD
U13-B
DM74C901
U8-B
DM74LS74
U8-A
U2-B
R5 910Ω
START
START CONVERSION
CONVERSION COMPLETE
CONVERSION COMPLETE*
U13-C
U13-D
CONVERTED
CONVERTING
TO SENSE A OR B OF SC/MP
31 OR 32
LH0070
PRECISION VOLTAGE REFERENCE
+10.00 – VOLT REFERENCE
TO D/A CONVERTER
C6 22pF CERAMIC
C7 0.2µF
C8 1000pF SILVER MICA
A/D CONVERTER U34 AD1210
CLOCK
TO D/A CONVERTER
U12-A
U12-B
DM74C14
R6 15k
300 kHz
C9 0.001µF
LEVEL SHIFTER U14 DM74C901
LEVEL SHIFTER U15 DM74C901
TRI-STATE BUFFERS U16 DM8098
TRI-STATE BUFFERS U17 DM8098
SELECT LO 4
SELECT HI 8
FROM ORDER DECODE
SC/MP DATA BUS

Figure 9. Analog-to-Digital Converter

The on-board RAM consists of three 16-word-by-4-bit bipolar RAMs interconnected to create a 16-word-by-12-bit memory array. The memory array is arranged to provide for storage of eight 12-bit digital equivalents to an analog voltage. Memory devices U22 and U23 constitute the upper 8 bits of the memory array while device U24 constitutes the lower 4 bits of the memory array. When addressed in the Read mode by the Control Logic, the on-board RAM outputs the selected channel data to the Output Buffers. The data is put onto the SC/MP data bus in two steps, the Hi 8 bits followed by the Lo 4 bits. When in the Refresh mode of operation, all 12 bits of RAM are output at the same time to the D/A converter.

The D/A converter converts the digital value output by the on-board RAM into the analog equivalent. The output of the D/A converter is applied to the inputs of the Sample-and-Hold devices to await the Select Channel Enable Signals. Since the Select Channel Enable Signals are in synchronization with the output from the on-board RAM, each output will sample and hold a value that corresponds to a particular channel output from RAM. Each Sample-and-Hold device in turn controls two output buffers; one, a voltage source and the other a current source.

NOTE

> For this application, only four output channels were used although the circuit is capable of supporting a total of eight outputs. To utilize all eight outputs, it will be necessary to add additional Sample-and-Hold devices and buffers and to enable the outputs using the four additional Channel Select Signals available from the output selector.

Figure 10 illustrates the Digital-to-Analog Converter logic schematic.

Figure 11 contains the component parts list for the A/D–D/A converter circuit.

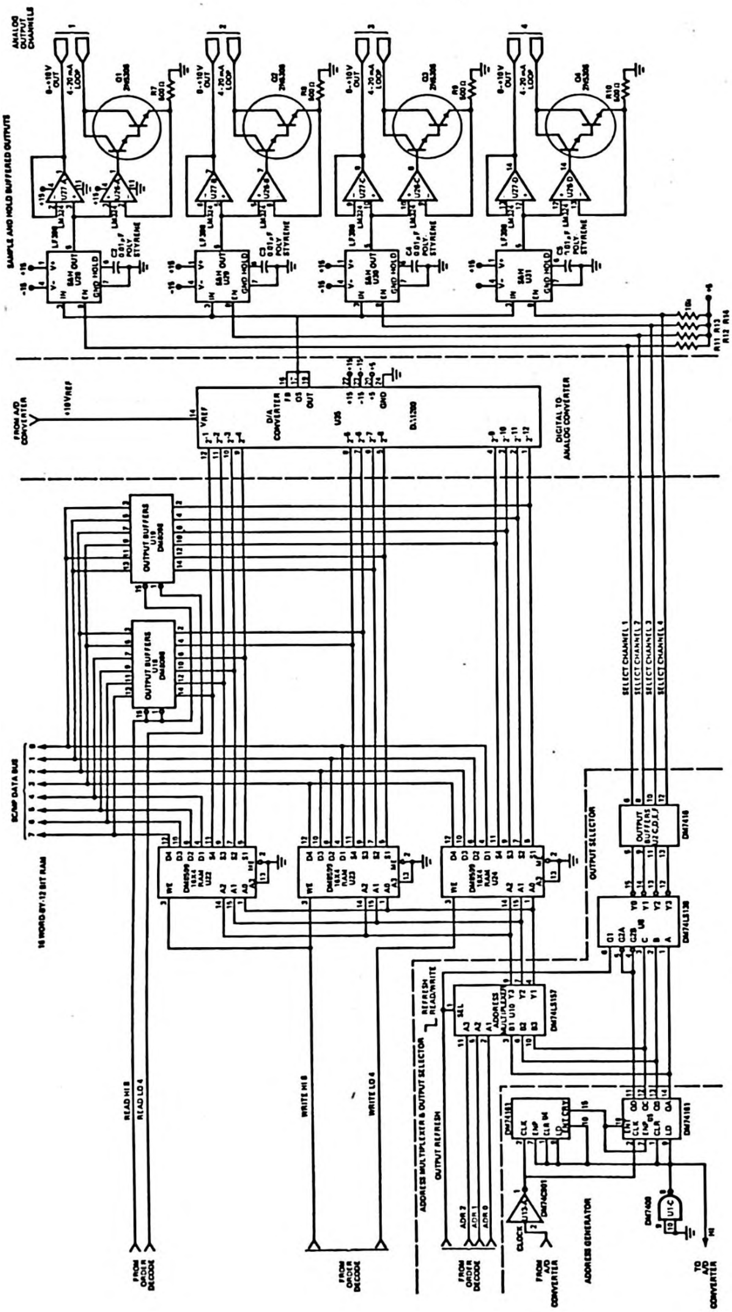

ANALOG OUTPUT CHANNELS
SAMPLE AND HOLD BUFFERED OUTPUTS
0-+10V OUT
4-20 mA LOOP
2N5306
500 Ω
LF398
LM324
0.01 μF POLY-STYRENE
S&H
IN
OUT
HOLD
GND
FROM A/D CONVERTER
+10 VREF
D/A CONVERTER
U25
DIGITAL TO ANALOG CONVERTER
OUTPUT BUFFERS
U19
U18
SC/MP DATA BUS
16 WORD-BY-12 BIT RAM
16X4 RAM
U22
U23
U24
OUTPUT SELECTOR
DM74LS138
SELECT CHANNEL 1
SELECT CHANNEL 2
SELECT CHANNEL 3
SELECT CHANNEL 4
R11 R12 R13 R14
10k
+5
REFRESH READ/WRITE
ADDRESS MULTIPLEXER
U10
DM74LS157
ADDRESS MULTIPLEXER & OUTPUT SELECTOR
OUTPUT REFRESH
READ HI 8
READ LO 4
WRITE HI 8
WRITE LO 4
FROM ORDER DECODE
ADR 2
ADR 1
ADR 0
CLOCK
FROM A/D CONVERTER
ADDRESS GENERATOR
DM74161
DM7400
U1-C
TO A/D CONVERTER

Figure 10. Digital-to-Analog Converter

U1	DM7400	R1	Resistor Array, RA15 (3K)
U2	DM7416	R2, 3, 4	1K
U3	DM7432	R5	910Ω
U4, 5	DM74161	R6	1.5K
U6, 7, 8	DM74LS138	R7, 8, 9, 10	500Ω
U9	DM74LS74	R11, 12, 13, 14	10K
U10	DM74LS157		
U11	DM74LS174		
U12	DM74C14		
U13, 14, 15	DM74C901	C1, 2, 3, 4, 5	0.01 μF — Polystyrene
U16, 17, 18, 19	DM8098	C6	22 μF — 15VDC
U20, 21	DM8131	C7	0.2 μF — Ceramic
U22, 23, 24	DM8599	C8	1000 pF — Silver Mica
U25	LH0070	C9	0.001 μF
U26, 27	LM324		
U28, 29, 30, 31, 32	LF398		
U33	LF11508		
U34	AD1210		
U35	DA1200	S1, 2	SPST DIP Switches
Q1, 2, 3, 4	2N5306		

Figure 11. Parts List

REFERENCE PUBLICATIONS

AN-156 Specifying A/D and D/A Converters

National Semiconductor Linear Data Book

SC/MP Technical Description Pub. No. 4200079A

SC/MP Microprocessor Assembly Language Programming Manual, Order No. ISP-85/9948

Instrumentation Amplifier

National Semiconductor
Linear Brief 1
Robert C. Dobkin
March 1969

The differential input single-ended output instrumentation amplifier is one of the most versatile signal processing amplifiers available. It is used for precision amplification of differential dc or ac signals while rejecting large values of common mode noise. By using integrated circuits, a high level of performance is obtained at minimum cost.

Figure 1 shows a basic instrumentation amplifier which provides a 10 volt output for 100 mV input, while rejecting greater than ±11V of common mode noise. To obtain good input characteristics, two voltage followers buffer the input signal. The LM102 is specifically designed for voltage follower usage and has 10,000 MΩ input impedance with 3 nA input currents. This high of an input impedance provides two benefits: it allows the instrumentation amplifier to be used with high source resistances and still have low error; and it allows the source resistances to be unbalanced by over 10,000 ohms with no degradation in common mode rejection. The followers drive a balanced differential amplifier, as shown in Figure 1, which provides gain and rejects the common mode voltage. The gain is set by the ratio of R_4 to R_2 and R_5 to R_3. With the values shown, the gain for differential signals is 100.

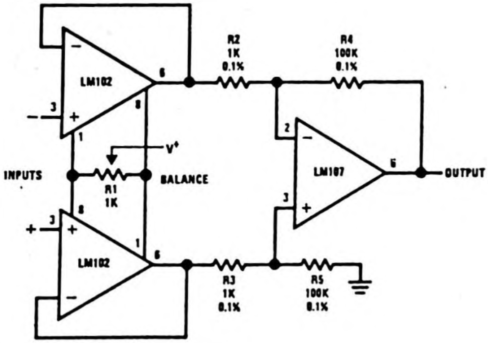


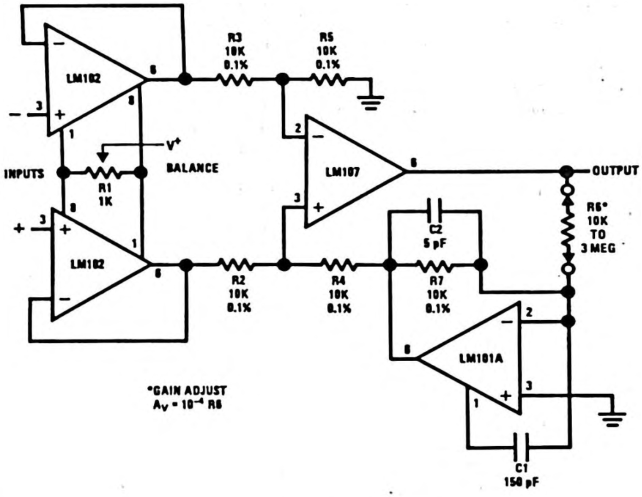
FIGURE 1. Differential-Input Instrumentation Amplifier

Figure 2 shows an instrumentation amplifier where the gain is linearly adjustable from 1 to 300 with a single resistor. An LM101A, connected as a fast inverter, is used as an attenuator in the feedback loop. By using an active attenuator, a very low impedance is always presented to the feedback resistors, and common mode rejection is unaffected by gain changes. The LM101A, used as shown, has a greater bandwidth than the LM107, and may be used in a feedback network without instability. The gain is linearly dependent on R_6 and is equal to $10^{-4} R_6$.

To obtain good common mode rejection ratios, it is necessary that the ratio of R_4 to R_2 match the ratio of R_5 to R_3. For example, if the resistors in circuit shown in Figure 1 had a total mismatch of 0.1%, the common mode rejection would be 60 dB times the closed loop gain, or 100 dB. The circuit shown in Figure 2 would have constant common mode rejection of 60 dB, independent of gain. In either circuit, it is possible to trim any one of the resistors to obtain common mode rejection ratios in excess of 100 dB.

For optimum performance, several items should be considered during construction. R_1 is used for zeroing the output. It should be a high resolution, mechanically stable potentiometer to avoid a zero shift from occurring with mechanical disturbances. Since there are several ICs operating in close proximity, the power supplies should be bypassed with .01 μF disc capacitors to insure stability. The resistors should be of the same type to have the same temperature coefficient.

A few applications for a differential instrumentation amplifier are: differential voltage measurements, bridge outputs, strain gauge outputs, or low level voltage measurement.



*GAIN ADJUST
$A_V = 10^{-4}$ R6

FIGURE 2. Variable Gain, Differential-Input Instrumentation Amplifier

Feedforward Compensation Speeds Op Amp

National Semiconductor
Linear Brief 2
Robert C. Dobkin
March 1969

A feedforward compensation method increases the slew rate of the LM101A from 0.5/μs to 10V/μs as an inverting amplifier. This extends the usefulness of the device to frequencies an order of magnitude higher than the standard compensation network. With this speed improvement, IC op amps may be used in applications that previously required discretes. The compensation is relatively simple and does not change the offset voltage or current of the amplifier.

In order to achieve unconditional closed loop stability for all feedback connections, the gain of an operational amplifier is rolled off at 6 dB per octave, with the accompanying 90 degrees of phase shift, until a gain of unity is reached. The frequency compensation networks shape the open loop response to cross unity gain before the amplifier phase shift exceeds 180 degrees. Unity gain for the LM101A is designed to occur at 1 MHz. The reason for this is the lateral PNP transistors used for level shifting have poor high frequency response and exhibit excess phase shift about 1 MHz. Therefore, the stable closed loop bandwidth is limited to approximately 1 MHz.

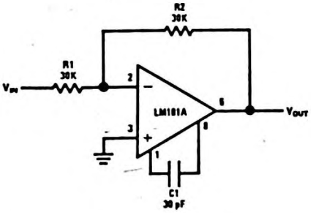


FIGURE 1. Standard Frequency Compensation

Usually, the LM101A is frequency compensated by a single 30 pF capacitor between Pins 1 and 8, as shown in Figure 1. This gives a slew rate of 0.5V/μs. The feedforward is achieved by connecting a 150 pF capacitor between the inverting input, Pin 2, and one of the compensation terminals, Pin 1, as shown in Figure 2. This eliminates the lateral PNP's from the signal path at high frequencies. Unity gain bandwidth is 10 MHz and the slew rate is 10V/μs. The diode can be added to improve slew with high speed input pulses.

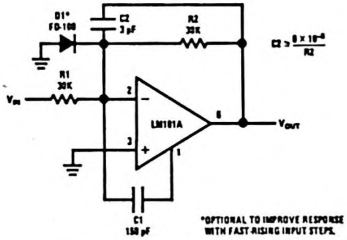

D1*
FD-100
C2
3 pF
R2
30K
$C2 \geq \frac{8 \times 10^{-6}}{R2}$
R1
30K
V_{IN}
2
3
LM101A
6
1
V_{OUT}
C1
150 pF
*OPTIONAL TO IMPROVE RESPONSE WITH FAST-RISING INPUT STEPS.

FIGURE 2. Feedforward Frequency Compensation

Figure 3 shows the open loop response in the high and low speed configuration. Higher open loop gain is realized with the fast compensation, as the gain rolls off at about 6 dB per octave until a gain of unity is reached at about 10 MHz. Figures 4 and 5 show the small signal and large signal transient response. There is a small amount of ringing; however, the amplifier is stable over a −55°C to +125°C temperature range. For comparison, large signal transient response with 30 pF frequency compensation is shown in Figure 6.

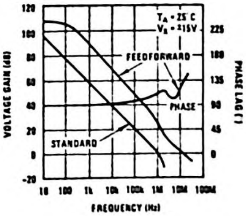


FIGURE 3. Open Loop Response for Both Frequency Compensation Networks

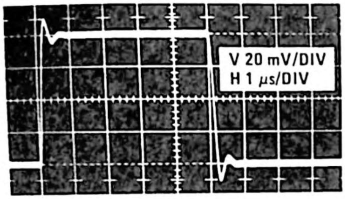


FIGURE 4. Small Signal Transient Response with Feedforward Compensation

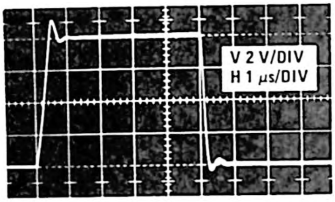


FIGURE 5. Large Signal Transient Response with Feedforward Compensation

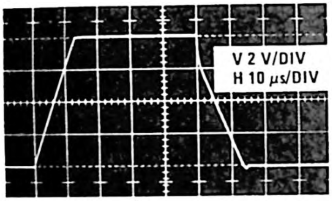


FIGURE 6. Large Signal Transient Response with Standard Compensation

As with all high frequency, high-gain amplifiers, certain precautions should be taken to insure stable operation. The power supplies should be bypassed near the amplifier with .01 μF disc capacitors. Stray capacitance, such as large lands on printed circuit boards, should be avoided at Pins 1, 2, 5, and 8. Load capacitance in excess of 75 pF should be decoupled, as shown in Figure 7; however, 500 pF of load capacitance can be tolerated without decoupling at the expense of bandwidth by the addition of 3 pF between Pins 1 and 8. A small capacitor C_2 is needed as a lead across the feedback resistor to insure that the rolloff is less than 12 dB per octave at unity gain. The capacitive reactance of C_2 should equal the feedback resistance between 2 and 3 MHz. For integrator applications, the lead capacitor is isolated from the feedback capacitor by a resistor, as shown in Figure 8.

Feedforward compensation offers a marked improvement over standard compensation. In addition to having higher bandwidth and slew, there is vanishingly small gain error from DC to 3 kHz, and less than 1% gain error up to 100 kHz as a unity gain inverter. The power bandwidth is also extended from 6 kHz to 250 kHz. Some applications for this type of amplifier are: fast summing amplifier, pulse amplifier, D/A and A/D systems, and fast integrator.

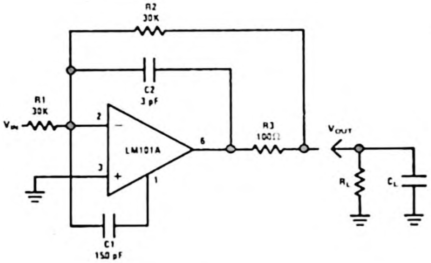


FIGURE 7. Capacitive Load Isolation

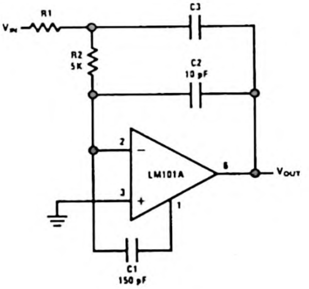


FIGURE 8. Fast Integrator

Worst Case Power Dissipation in Linear Regulators

National Semiconductor
Linear Brief 3
April 1969

The most frequent cause of failures of voltage regulators is excessive dissipation in the semiconductor components. Regulators using integrated circuits are no exception to this. In fact, IC regulators are more prone to overdissipation because they are not generally available in power packages, because complete integrated circuits must be operated at a lower, maximum junction temperature than silicon power transistors, and because the package must be able to dissipate the quiescent operating power of the control circuitry in addition to the power in the pass transistor.

The problems and solutions presented here give examples of the worst case calculations that should be used in designing voltage regulators with ICs. These questions were used in a contest sponsored by National Semiconductor. The entries received clearly showed that engineers have a marked tendency to be overly optimistic about the dissipation capability of the IC regulators as well as the power ratings of the external power transistors used with them. In a surprising number of cases the errors were of such a magnitude to cause almost certain, premature failure of the regulator under the conditions specified. The questions and answers follow:

1. What is the power limited full-load current for a 24V regulator using the LM100 (without a heat sink) when the worst case operating conditions are 125°C ambient and 40V input voltage?

   The maximum chip temperature of the LM100 is 150°C, and the thermal resistance of the TO-5 package is 150°C/W when no heat sink is used. The permissable, junction-to-ambient temperature rise is 25°C with a 125°C ambient, so the maximum allowable package dissipation is 167 mW.

   The worst case quiescent current of the LM100 is 3.0 mA. With a 40V input voltage, this produces an internal dissipation of 120 mW, even with no load. Therefore, the device can only dissipate another 47 mW in supplying the load current. With 40V in and 24V out, the input-output voltage differential is 16V. This means that 2.95 mA can be supplied through the internal pass transistor without exceeding the ratings.

   The divider resistors required on the LM100 feedback to give a 24V output are 26.6k and 2.1k. For a 1.8V sense voltage on the feedback terminal, the divider current will be 0.85 mA. Since this current must be supplied by the integrated circuit, it must be subtracted from the available load current. Hence the maximum output current, taking into account worse case conditions, is *2.1 mA*.

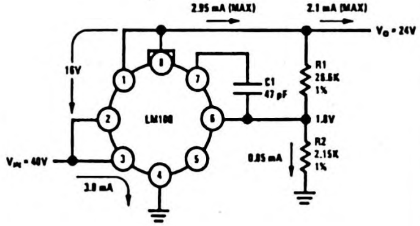


FIGURE 1. Circuit Used in the Solution of Question 1.

2. What is the maximum allowable short-circuit current for an LM104 regulator circuit, with a 2N2905A series pass transistor (without a heat sink) when the worst case input is 20V at an ambient of 85°C?

   The 2N2905A, without a heat sink, can dissipate a maximum of 0.6W at 25°C. However, this must be derated by 3.42 mW/°C for operation at higher temperatures. Since an 85°C ambient is 60°C higher than the temperature at which the transistors are specified, the maximum power rating must be reduced by 205 mW, to 395 mW. With a shorted output, the voltage dropped across the current limit sense resistor is 0.5V, so the voltage across the external pass transistor will be 19.5V for 20V input. This means that the 395 mW maximum dissipation rating will be exceeded for short-circuit currents greater than *20.2 mA*.

3. In the previous example, what is the maximum current when the case temperature of the 2N2905A is held to 100°C?

The maximum dissipation of the 2N2905A is 3W at 25°C case temperature, but this must be derated by 17.2 mW/°C for higher case temperatures. With a 100°C case temperature, the allowable dissipation is reduced by 1.29W to 1.71W.

As in the previous example, the voltage across the pass transistor will be 19.5V. This gives a dissipation-limited short-circuit current of *88 mA.*

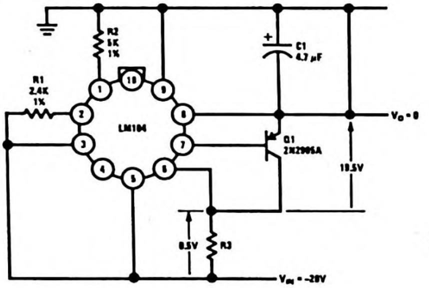


FIGURE 2. Circuit Used in the Solution of Questions 2 and 3.

4. In the negative regulator with foldback current limiting, what will be the worst case dissipation in the PNP driver, Q_1, with full load and a 24V input voltage?

   The 2N3772 is specified to have a minimum current gain of 15 at 10A and 25°C. It would be reasonable to assume a minimum current gain of 15 at 5A for elevated temperatures where dissipation is most significant. This means that the base current for a 5A load current will be 0.33A. The worst case emitter-base voltage of the 2N3772 at 5A will be about 1V, so the current through the 68Ω emitter-base resistor will be 15 mA. Hence, the PNP driver must supply a total current of 345 mA.

   The voltage dropped across the PNP driver will be the 12V input output voltage differential, less the 1V dropped across the current sense resistor and the 1V dropped across the emitter-base junction of the 2N3772. Therefore, the PNP driver operates with 10V across it and dissipates about *3.5W.*

5. Could a 2N2905A be used in the example above if the maximum ambient were 85°C?

   Even with an infinite heat sink, the 2N2905A can dissipate only 2W at 85°C. *Therefore, it cannot be used.*

The answers to these questions show that the maximum output current of a regulator can be substantially less than might be expected from a cursory analysis of the circuit. Detailed analysis under worst case conditions is necessary to insure a reliable design. These calculations are more important than most other design calculations because errors do not result in somewhat degraded performance that usually shows up in checking out the equipment. Instead, these errors cause failures that do not always show up during checkout, but can occur in field operation.

Additional information on the design of reliable voltage regulators is given in application notes AN-21 and AN-23, available from National Semiconductor.

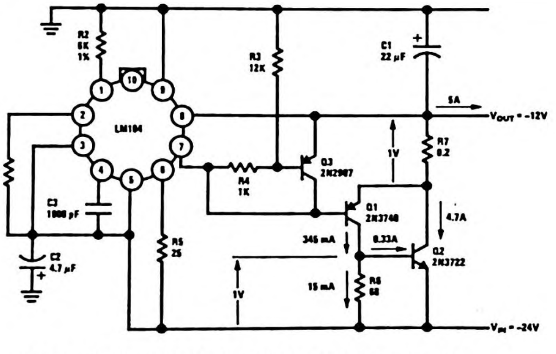


FIGURE 3. Circuit Used in the Solution of Questions 4 and 5.

Fast Compensation Extends Power Bandwidth

National Semiconductor
Linear Brief 4
Robert C. Dobkin
April 1969

In all IC operational amplifiers the power bandwidth depends on the frequency compensation. Normally, compensation for unity gain operation is accompanied by the lowest power bandwidth. A technique is presented which extends the power bandwidth of the LM101A for non-inverting gains of unity to ten, and also reduces the gain error at moderate frequencies.

In order to achieve unconditional stability, an operational amplifier is rolled off at 6 dB per octave, with an accompanying 90 degrees of phase shift, until a gain of unity is reached. Unity gain in most monolithic operational amplifiers is limited to 1 MHz, because the lateral PNP's used for level shifting have poor frequency response and exhibit excess phase shift at frequencies above 1 MHz. Hence, for stable operation, the closed loop bandwidth must be less than 1 MHz where the phase shift remains below 180 degrees.

For high closed loop gains, less severe frequency compensation is necessary to roll the open loop gain off at 6 dB per octave until it crosses the closed loop gain. The frequency where it crosses must, as previously mentioned, be less than 1 MHz. For closed loop gains between 1 and 10, more frequency compensation must be used to insure that the open loop gain has been rolled off soon enough to cross the closed loop gain before 1 MHz is reached.

The power bandwidth of an operational amplifier depends on the current available to charge the frequency compensation capacitors. For unity gain operation, where the compensation capacitor is largest, the power bandwidth of the LM101A is 6 kHz. Figure 1 shows an LM101A with unity gain

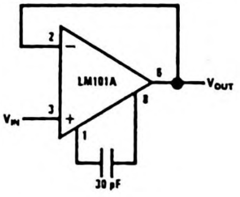


FIGURE 1. LM101A With Standard Frequency Compensation.

compensation and Figure 3 shows the open loop gain as a function of frequency.

A two-pole frequency compensation network, as shown in Figure 2, provides more than a factor of two improvement in power bandwidth and reduced gain error at moderate frequencies. The network consists of a 30 pF capacitor, which sets the unity gain frequency at 1 MHz, along with a 300 pF capacitor and a 10k resistor. By dividing the ac output voltage with the 10k resistor and 300 pF capacitor, there is less ac voltage across the 30 pF capacitor and less current is needed for charging. Since the voltage division is frequency sensitive, the open loop gain rolls off at 12 dB per octave until a gain of 20 is reached at 50 kHz. From 50 kHz to 1 MHz the 10k resistor is larger than the impedance of the 300 pF capacitor and the gain rolls off at 6 dB per octave. The open loop gain plot is shown in Figure 3. To insure sufficient drive to the 300 pF capacitor, it is connected to the output, Pin 6, rather than Pin 8. With this frequency compensation method, the power bandwidth is typically 15–20 kHz as a follower, or unity gain inverter.

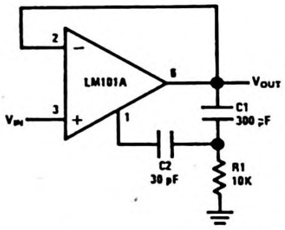


FIGURE 2. **LM101A with Frequency Compensation to Extend Power Bandwidth.**

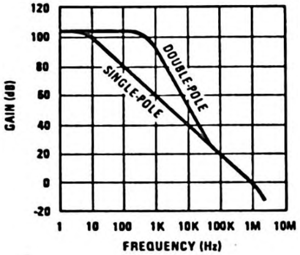


FIGURE 3. **Open Lopp Response for Both Frequency Compensation Networks.**

This frequency compensation, in addition to extending the power bandwidth, provides an order of magnitude lower gain error at frequencies from DC to 5 kHz. Some applications where it would be helpful to use the compensation are: differential amplifiers, audio amplifiers, oscillators, and active filters.

High Q Notch Filter

National Semiconductor
Linear Brief 5
Robert C. Dobkin
March 1969

The twin "T" network is one of the few RC filter networks capable of providing an infinitely deep notch. By combining the twin "T" with an LM102 voltage follower, the usual drawbacks of the network are overcome. The Q is raised from the usual 0.3 to something greater than 50. Further, the voltage follower acts as a buffer, providing a low output resistance; and the high input resistance of the LM102 makes it possible to use large resistance values in the "T" so that only small capacitors are required, even at low frequencies. The fast response of the follower allows the notch to be used at high frequencies. Neither the depth of the notch nor the frequency of the notch are changed when the follower is added.

Figure 1 shows a twin "T" network connected to an LM102 to form a high Q, 60 Hz notch filter.

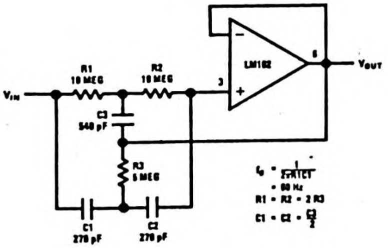


FIGURE 1. High Q Notch Filter

The junction of R_3 and C_3, which is normally connected to ground, is bootstrapped to the output of the follower. Because the output of the follower is a very low impedance, neither the depth nor the frequency of the notch change; however, the Q is raised in proportion to the amount of signal fed back to R_3 and C_3. Figure 2 shows the response of a normal twin "T" and the response with the follower added.

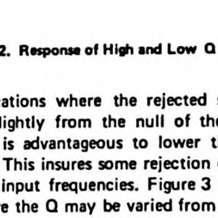


FIGURE 2. Response of High and Low Q Notch Filter

In applications where the rejected signal might deviate slightly from the null of the notch network, it is advantageous to lower the Q of the network. This insures some rejection over a wider range of input frequencies. Figure 3 shows a circuit where the Q may be varied from 0.3 to 50. A fraction of the output is fed back to R_3 and C_3 by a second voltage follower, and the notch Q is dependent on the amount of signal fed back. A second follower is necessary to drive the twin "T" from a low-resistance source so that the notch frequency and depth will not change with the potentiometer setting. Depending on the potentiometer setting, the circuit in Figure 3 will have a response that falls in the shaded area of Figure 2.

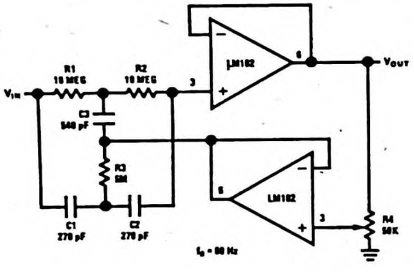


FIGURE 3. Adjustable Q Notch Filter

An interesting change in the high Q twin "T" occurs when components are not exactly matched in ratio. For example, an increase of 1 to 10 percent in the value of C_3 will raise the Q, while degrading the depth of the notch. If the value of C_3 is raised by 10 to 20 percent, the network provides voltage gain and acts as a tuned amplifier. A voltage gain of 400 was obtained during testing. Further increases in C_3 cause the circuit to oscillate, giving a clipped sine wave output.

The circuit is easy to use and only a few items need be considered for proper operation. To minimize notch frequency shift with temperature, silver mica, or polycarbonate, capacitors should be used with precision resistors. Notch depth depends on component match, therefore, 0.1 percent resistors and 1 percent capacitors are suggested to minimize the trimming needed for a 60 dB notch. To insure stability of the LM102, the power supplies should be bypassed near the integrated circuit package with .01 μF disc capacitors.

Fast Voltage Comparators with Low Input Current

National Semiconductor
Linear Brief 6
May 1969

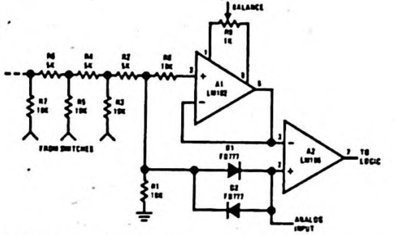
Monolithic voltage comparators are available today which are both fast and accurate. They can detect the height of a pulse with a 5 mV accuracy within 40 ns. However, these devices have relatively high input currents and low input impedances, which reduces their accuracy and speed when operating from high source resistances. This is probably a basic limitation since the input transistors of the integrated circuit must be operated at a relatively high current to get fast operation. Further, the circuit must be gold doped to reduce storage time, and this limits the current gain that can be obtained in the transistors. High gain transistors operating at low collector currents are necessary to get good input characteristics.

One way of overcoming this difficulty is to buffer the input of the comparator. A voltage follower is available which is ideally suited for this job. This device, the LM102*, is both fast and has a low input current. It can reduce the effective input current of the comparator by more than three orders of magnitude without greatly reducing speed.

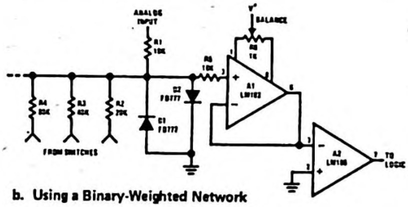
A comparator circuit for an A/D converter which uses this technique is shown in Figure 1a. An LM102 voltage follower buffers the output of a ladder network and drives one input of the comparator. The analog signal is fed to the other input of the comparator. It should come from a low impedance source such as the output of a signal processing amplifier, or another LM102 buffer amplifier.

Clamp diodes, D_1 and D_2, are included to make the circuit faster. These diodes clamp the output of the ladder so that it is never more than 0.7V different from the analog input. This reduces the voltage excursion that the buffer must handle on the most significant bit and keeps it from slewing. If fast, low-capacitance diodes are used, the signal to the comparator will stabilize approximately 200 ns after the most significant bit is switched in. This is about the same as the stabilization time of the ladder network alone, as its speed is limited by stray capacitances. The diodes also limit the voltage swing across the inputs of the comparator, increasing its operating speed and insuring that the device is not damaged by excessive differential input voltage.

The buffer reduces the loading on the ladder from 45 μA to 20 nA, maximum, over a −55°C to 125°C temperature range. Hence, in most applications the input current of the buffer is totally insignificant. This low current will often permit the use of larger resistances in the ladder which simplifies design of the switches driving it.



a. Using a Ladder Network



b. Using a Binary-Weighted Network

FIGURE 1. Comparator Circuits for Fast A/D Converters

It is possible to balance out the offset of the LM102 with an external 1 kΩ potentiometer, R_9. The adjustment range of this balance control is large enough so that it can be used to null out the offset of both the buffer and the comparator. A 10 kΩ resistor should be installed in series with the input to the LM102, as shown. This is required to make the short circuit protection of the device effective and to insure that it will not oscillate. This resistor should be located close to the integrated circuit.

A similar technique can be used with A/D converters employing a binary-weighted resistor network. This is shown in Figure 1b. The analog input is fed into a scaling resistor, R_1. This resistor is selected so that the input voltage to the LM102 is zero when the output of the D/A network corresponds to the analog input voltage. Hence, if the D/A output is too low, the output of the LM106 will be a logical zero; and the output will change to a logical one as the D/A output exceeds the analog signal.

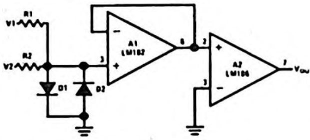
The analog signal must be obtained from a source impedance which is low by comparison to R_1. This can be either another LM102 buffer or the output of the signal-processing amplifier. Clamp diodes, D_1 and D_2, restrict the signal swing and speed up the circuit. They also limit the input signal seen by the LM106 to protect if from overloads. Operating speed can be increased even further by using silicon backward diodes (a degenerate tunnel diode) in place of the diodes shown, as they will clamp the signal swing to about 50 mV. The offset voltage of both the LM102 and the LM106 can be balanced out, if necessary, with R_6.

The binary weighted network can be driven with single pole, single-throw switches. This will result in a change in the output resistance of the network when it switches, but circuit performance will not be affected because the input current of the LM102 is negligible. Hence, using the LM102 greatly simplifies switch design.

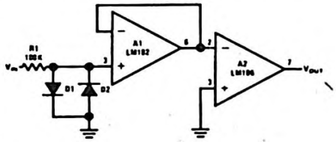
Although it is possible to use a 710 as the voltage comparator in these circuits, the LM106 offers several advantages. First, it can drive a fan out of 10 with standard, integrated DTL or TTL. It also has two strobe terminals available which disable the comparator and give a high output when either of the terminals is held at a logical zero. This adds logic capability to the comparator in that it makes it equivalent to a 710 and a two-input NAND gate. If not needed, the strobe pins can be left unconnected without affecting performance. The voltage gain of the LM106 is about 45,000, which is 30 times higher than that of the 710. The increased gain reduces the error band in making a comparison. The LM106 will also operate from the same supply voltage as the LM102, and other operational amplifiers, for ±12V supplies. However, it can also be operated from ±15V supplies if a 3V zener diode is connected in series with the positive supply lead.

It is necessary to observe a few precautions when working with fast circuits operating from relatively high impedances. A good ground is necessary, and a ground plane is advisable. All the individual points in the circuit which are to be grounded, including bypass capacitors, should be returned separately to the same point on the ground so that voltages will not be developed across common lead inductance. The power supply leads of the integrated circuits should also be bypassed with low inductance 0.01 µF capacitors. These capacitors, preferably disc ceramic, should be installed with short leads and located close to the devices. Lastly, the output of the comparator should be shielded from the circuitry on the input of the buffer, as stray coupling can also cause oscillation.

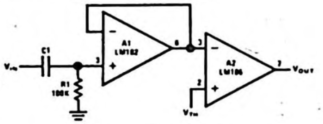
Although the circuits shown so far were designed for use in A/D converters, the same techniques apply to a number of other applications. Figure 2 gives examples of circuits which can put stringent input current requirements on the comparator. The first is a comparator for signals of opposite polarity. Resistors (R_1 and R_2) are required to isolate the two signal sources. Frequently, these resistors must be relatively large so that the signal sources are not loaded. Hence, the input current of the comparator must be reduced to prevent inaccuracies. Another example is the zero-crossing detector in Figure 2b. When the input signal can exceed the common mode range of the comparator (±5V for the LM106), clamp diodes must be used. It is then necessary to isolate the comparator from the input with a relatively large resistance to prevent loading. Again, bias currents should be reduced. A third example, in Figure 2c, is a comparator with an ac coupled input. An LM106 will draw an input current which is twice the specified bias current when the signal is above the comparison threshold. Yet, it draws no current when the signal is below the threshold. This asymmetrical current drain will charge any coupling capacitor on the input and produce an error. This problem can be eliminated by using a buffer, as the input current will be both low and constant.



a. Comparator for Signals of Opposite Polarity



b. Zero Crossing Detector



c. Comparator for AC Coupled Signals

FIGURE 2. Applications Requiring Low Input Current Comparators

The foregoing has shown how two integrated circuits can be combined to provide state-of-the-art performance in both speed and input current. Equivalent results will probably not be achievable in a single circuit for some time, as the technologies required are not particularly compatible. Further, considering the low cost of monolithic circuits, approaches like this are certainly economical.

Tracking Voltage Regulators

National Semiconductor
Linear Brief 7
Robert C. Dobkin
August 1969

Integrated circuit voltage regulators are available today which are economical and offer a high degree of performance. There are both positive and negative regulators capable of achieving better than 0.1% regulation under normal fluctuations in input supply and load. Due to production variations, the internal reference voltage in these regulators may vary as much as 10% from unit to unit. Normally, this causes no problems as most power supply circuits have an adjustment potentiometer which is varied to obtain the correct output voltage. In systems with more than one regulated output voltage, it is sometimes desirable to adjust all supplies with a single potentiometer. This results in savings by eliminating one or more potentiometers as well as eliminating the need to adjust the supplies individually.

Figure 1 shows a 5V and a 15V regulator with both outputs adjusted with a single potentiometer. Although the technique is not exact, the error is typically under 2%. As shown in Figure 1, the internal reference voltages for the LM105* regulators, available at pin 5, are tied together. This insures that both regulators operate with the same reference voltage. The lower resistors of the output divider, R_2, are connected through a common adjustment potentiometer to ground. R_5 adjusts both regulators for variations in the 1.8V reference. Note that the wiper of R_5 is connected to one side of the potentiometer. If a rheostat connection were used, the arm might open circuit during adjustment, causing large transients on the output.

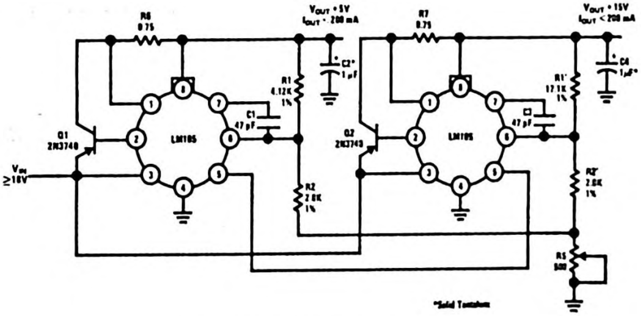
The calculations of resistor values for the output divider resistors are made with the consideration that the adjustment is not exact and that two regulators are adjusted. The bottom resistor of the divider, R_2, is fixed at 2K. The top of the divider, R_1, is then calculated for the output voltage using 1.6V as the reference voltage. To help compensate for the inaccuracies in the adjustment, output voltages are calculated slightly off from the desired values. For the 5 and 15V regulators, R_1 is calculated to give a 2% low output voltage on the 5V regulator and a 2% high output voltage on the 15V regulator.

$$R_1 = \frac{(V_{OUT} - 1.6V)\ 2000\Omega}{1.6V}$$

R_5 will now adjust both regulators to within 2% of the desired output for reference variations from 1.6V to 2.0V. From the previous calculations, a 1.6V reference yields outputs of 4.9V and 15.3V. If the reference is 2.0V, R_5 is adjusted to 324 ohms and the output voltages are 5.1V and 14.9V. If the reference is near the typical value of 1.8V, both outputs are within 1% of nominal.

These calculations do not account for resistor inaccuracies. If 1% resistors are used there is an additional worst case error of 2% for each regulator. Resistor errors are inherent in any type of tracking regulator system, even if the adjustment is theoretically exact.

Actually, any number of regulators may be connected to a single adjustment resistor. The adjustment accuracy of this technique depends on the output voltage differences among the regulators. The previous example was a severe difference, and had only 2% accuracy. With close output voltages, such as 12V and 15V, the error is much smaller. The 12V regulator is calculated to 1/2% low and 15V regulator 1/2% high with the 1.6V reference. Both regulators are then within 1/2% for reference variations of 1.6 to 2.0 volts. This adjustment method is, of course, exact if two regulators have the same output.



*Solid Tantalum

FIGURE 1. Tracking Positive Regulators

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*R. J. Widlar, "The LM105–An Improved Positive Regulator," National Semiconductor Corporation, AN 23, January, 1969.

Using a negative regulator to track a positive regulator is a somewhat easier task. An inverting operational amplifier may be used to provide a negative output voltage while using a positive voltage as a reference. The LM104† negative regulator is easily adapted for use as an inverting amplifier and provides several advantages over conventional operational amplifiers. It is designed to drive boost transistors for higher output current as well as providing a convenient method of current limiting the output. Further, the frequency compensation used on the LM104 is optimized for transient response to line and load changes. Figure 2 shows tracking ±15V regulators.

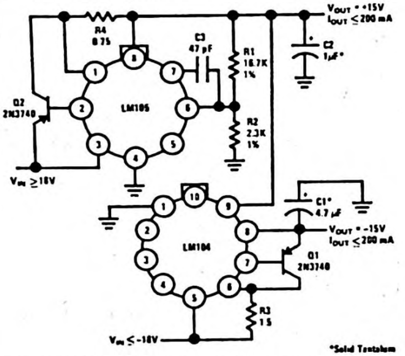
VOUT = +15V
IOUT ≤ 200 mA
R4
0.75
C3
47 pF
R1
16.7K
1%
C2
1µF*
Q2
2N3740
LM105
R2
2.3K
1%
VIN ≥ 18V
1
2
3
4
5
6
7
8
10
9
C1*
4.7 µF
VOUT = -15V
IOUT ≤ 200 mA
LM104
Q1
2N3740
R3
1.5
VIN ≤ -18V
*Solid Tantalum

FIGURE 2. Tracking Positive and Negative Regulators

Operation is most easily understood by referring to the functional schematic of the LM104 in Figure 3. The non-inverting input of the internal amplifier, pin 1, is connected to ground. The positive 15V reference is connected through an internal 15K ohm input resistor, R_{16}, to the inverting input. Feedback resistor, R_{15}, is also 15K ohm. This forms a unity gain inverting amplifier with a negative output voltage equal to the positive input voltage. The 15K ohm resistors in the LM104 are typically matched to 1%. This means that the output of both regulators may be adjusted with 1% accuracy by changing R_1 in Figure 2.

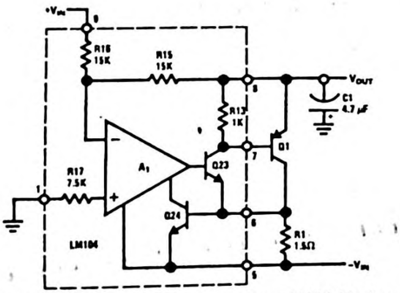
+VIN
9
R16
15K
R15
15K
8
VOUT
C1
4.7 µF
R13
1K
Q1
7
A1
Q23
R17
7.5K
1
−
+
Q24
6
LM104
R1
1.5Ω
-VIN
5

FIGURE 3. Functional Diagram of the LM104 Used as an Amplifier

The LM104 may also be used with inverting gain for negative output voltages greater than the positive reference voltage. Figure 4 shows a circuit where the −15V supply tracks a +5V supply. In this configuration the non-inverting input is not grounded, but tied to divider, R_5, R_6, between the negative output and ground. The output voltage equals

$$V_{OUT} = V^{+} \left[\frac{R_5 + R_6}{R_6 - R_5}\right]$$

where V^+ is the positive reference.

The line regulation and temperature drift are determined primarily by the positive reference, with the negative output tracking. The reference must be a low impedance source, such as an LM105 regulator, to insure that current drawn by pin 9 of the LM104 does not affect the reference voltage. Since the LM104 is connected to a positive voltage instead of ground, it sees a total voltage equal to the sum of the unregulated negative input and the positive reference voltage. This reduces the maximum unregulated negative input voltage allowable, and should be considered during design. If the negative output voltage must be less than the positive reference or the decrease in maximum unregulated input voltage cannot be tolerated, an alternate method of constructing tracking regulators is given elsewhere†. Of course, many negative regulators may be slaved to a single positive regulator.

Using standard linear integrated circuits, multiple output positive and negative supplies may be adjusted to within 2% or less by a single resistor. Although the absolute output is not exact, the regulation accuracy is still within 0.1%. These techniques can result in savings by the elimination of both time and materials when used.

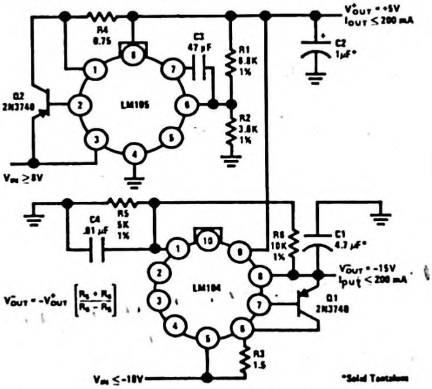
V^{+}_{OUT} = +5V
IOUT ≤ 200 mA
R4
0.75
C3
47 pF
R1
6.8K
1%
C2
1µF*
Q2
2N3740
LM105
R2
3.8K
1%
VIN ≥ 8V
1
2
3
4
5
6
7
8
C4
.01 µF
R5
5K
1%
10
9
R6
10K
1%
C1
4.7 µF*
V^{-}_{OUT} = -15V
IOUT < 200 mA
LM104
Q1
2N3740
$V^{-}_{OUT} = -V^{+}_{OUT}\left[\frac{R_5 + R_6}{R_6 - R_5}\right]$
R3
1.5
VIN ≤ -18V
*Solid Tantalum

FIGURE 4. Tracking Regulators With Different Output Voltages

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†R. J. Widlar, "Designs for Negative Regulators," National Semiconductor Corporation, AN-21, December, 1968.

Precision AC/DC Converters

National Semiconductor
Linear Brief 8
Robert C. Dobkin
August 1969

Although semiconductor diodes available today are close to "ideal" devices, they have severe limitations in low level applications. Silicon diodes have a 0.6V threshold which must be overcome before appreciable conduction occurs. By placing the diode in the feedback loop of an operational amplifier, the threshold voltage is divided by the open loop gain of the amplifier. With the threshold virtually eliminated, it is possible to rectify millivolt signals.

Figure 1 shows the simplest configuration for eliminating diode threshold potential. If the voltage at the non-inverting input of the amplifier is positive, the output of the LM101A swings positive. When the amplifier output swings 0.6V positive, D_1 becomes forward biased; and negative feedback through D_1 forces the inverting input to follow the non-inverting input. Therefore, the circuit acts as a voltage follower for positive signals. When the input swings negative, the output swings negative and D_1 is cut off. With D_1 cut off no current flows in the load except the 30 nA bias current of the LM101A. The conduction threshold is very small since less than 100 µV change at the input will cause the output of the LM101A to swing from negative to positive.

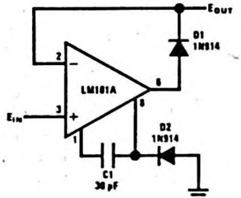

FIGURE 1. Precision Diode

A useful variation of this circuit is a precision clamp, as is shown in Figure 2. In this circuit the output is precisely clamped from going more positive than the reference voltage. When E_{IN} is more positive than E_{REF}, the LM101A functions as a summing amplifier with the feedback loop closed through D_1. Neglecting offsets, negative feedback keeps the summing node, and therefore the output, within 100 µV of the voltage at the non-inverting input. When E_{IN} is about 100 µV more negative than E_{REF}, the output swings positive, reverse biasing D_1. Since D_1 now prevents negative feedback from controlling the voltage at the inverting input, no clamping action is obtained. On both of the circuits in Figures 1 and 2 an output clamp diode is added at pin 8 to help speed response. The clamp prevents the operational amplifier from saturating when D_1 is reverse biased.

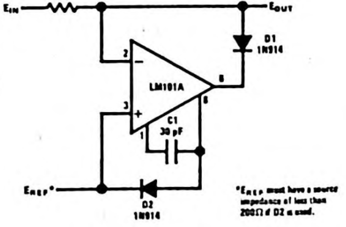

FIGURE 2. Precision Clamp

When D_1 is reverse biased in either circuit, a large differential voltage may appear between the inputs of the LM101A. This is necessary for proper operation and does no damage since the LM101A is designed to withstand large input voltages. These circuits will not work with amplifiers protected with back to back diodes across the inputs. Diode protection conducts when the differential input voltage exceeds 0.6V and would connect the input and output together. Also, unprotected devices such as the LM709, are damaged by large differential input signals.

The circuits in Figures 1 and 2 are relatively slow. Since there is 100% feedback for positive input signals, it is necessary to use unity gain frequency compensation. Also, when D_1 is reverse biased, the feedback loop around the amplifier is opened and the input stage saturates. Both of these conditions cause errors to appear when the input frequency exceeds 1.5 kHz. A higher performance precision half wave rectifier is shown in Figure 3. This circuit will provide rectification with 1% accuracy at frequencies from dc to 100 kHz. Further, it is easy to extend the operation to full wave rectification for precision ac/dc converters.

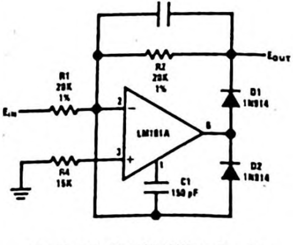

FIGURE 3. Fast Half Wave Rectifier

This precision rectifier functions somewhat differently from the circuit in Figure 1. The input signal is applied through R_1 to the summing node of an inverting operational amplifier. When the signal is negative, D_1 is forward biased and develops an output signal across R_2. As with any inverting amplifier, the gain is R_2/R_1. When the signal goes positive, D_1 is non-conducting and there is no output. However, a negative feedback path is provided by D_2. The path through D_2 reduces the negative output swing to −0.7V, and prevents the amplifier from saturating.

Since the LM101A is used as an inverting amplifier, feedforward* compensation can be used. Feedforward compensation increases the slew rate to 10V/μs and reduces the gain error at high frequencies. This compensation allows the half wave rectifier to operate at higher frequencies than the previous circuits with no loss in accuracy.

The addition of a second amplifier converts the half wave rectifier to a full wave rectifier. As is shown in Figure 4, the half wave rectifier is connected to inverting amplifier A_2. A_2 sums the half wave rectified signal and the input signal to provide a full wave output. For negative input signals the output of A_1 is zero and no current flows through R_3. Neglecting for the moment C_2, the output of A_2 is $-\frac{R_7}{R_6} E_{IN}$. For positive input signals, A_2 sums the currents through R_3 and R_6; and

$$E_{OUT} = R_7 \left[\frac{E_{IN}}{R_3} - \frac{E_{IN}}{R_6}\right].$$

If R_3 is 1/2 R_6, the output is $\frac{R_7}{R_6} E_{IN}$. Hence, the output is always the absolute value of the input.

Filtering, or averaging, to obtain a pure dc output is very easy to do. A capacitor, C_2, placed across R_7 rolls off the frequency response of A_2 to give an output equal to the average value of the input. The filter time constant is R_7C_2, and must be much greater than the maximum period of the input signal. For the values given in Figure 4, the time constant is about 2.0 seconds. This converter has better than 1% conversion accuracy to above 100 kHz and less than 1% ripple at 20 Hz. The output is calibrated to read the rms value of a sine wave input.

As with any high frequency circuit some care must be taken during construction. Leads should be kept short to avoid stray capacitance and power supplies bypassed with .01 μF disc ceramic capacitors. Capacitive loading of the fast rectifier circuits must be less than 100 pF or decoupling becomes necessary. The diodes should be reasonably fast and film type resistors used. Also, the amplifiers must have low bias currents.

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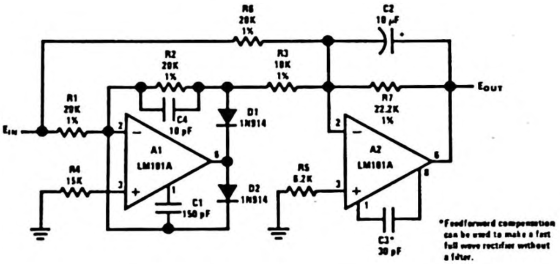
*R. C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor Corporation, LB-2*, April, 1969.



*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

FIGURE 4. Precision AC to DC Converter

Universal Balancing Techniques

National Semiconductor
Linear Brief 9
Robert C. Dobkin
August 1969

IC op amps are widely accepted as a universal analog component. Although the circuit designs may vary, most devices are functionally interchangeable. However, offset voltage balancing remains a personality trait of the particular amplifier design. The techniques shown here allow offset voltage balancing without regard to the internal circuitry of the amplifier.

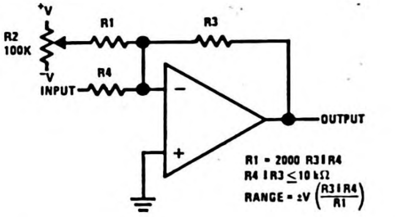


FIGURE 1. Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

The circuit shown in Figure 1 is used to balance out the offset voltage of inverting amplifiers having a source resistance of 10 kΩ or less. A small current is injected into the summing node of the amplifier through R_1. Since R_1 is 2000 times as large as the source resistance the voltage at the arm of the pot is attenuated by a factor of 2000 at the summing node. With the values given and ±15V supplies the output may be zeroed for offset voltages up to ±7.5 mV.

If the value of the source resistance is much larger than 10 kΩ, the resistance needed for R_1 becomes too large. In this case it is much easier to balance out the offset by supplying a small voltage at the non-inverting input of the amplifier. Figure 2 shows such a scheme. Resistors R_1 and R_2 divide the voltage at the arm of the pot to supply a ±7.5 mV adjustment range with ±15V supplies. This adjustment method is also useful when the feedback element is a capacitor or non-linear device.

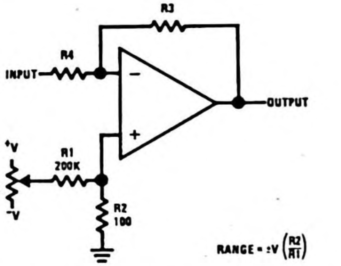


FIGURE 2. Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element

This technique of supplying a small voltage effectively in series with the input is also used for adjusting non-inverting amplifiers. As is shown in Figure 3, divider R_1, R_2 reduces the voltage at the arm of the pot to ±7.5 mV for offset adjustment. Since R_2 appears in series with R_4, R_2 should be considered when calculating the gain. If R_4 is greater than 10 kΩ the error due to R_2 is less than 1%.

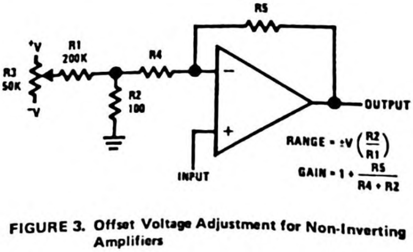


FIGURE 3. Offset Voltage Adjustment for Non-Inverting Amplifiers

A voltage follower may be balanced by the technique shown in Figure 4. R_1 injects a current which produces a voltage drop across R_3 to cancel the offset voltage. The addition of the adjustment resistors causes a gain error, increasing the gain by 0.05%. This small error usually causes no problem. The adjustment circuit essentially causes the offset voltage to appear at full output, rather than at low output levels, where it is a large percentage error.

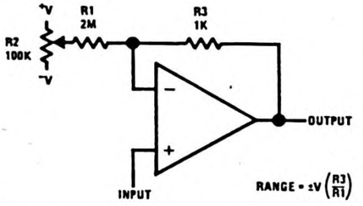


FIGURE 4. Offset Voltage Adjustment for Voltage Followers

Differential amplifiers are somewhat more difficult to balance. The offset adjustment used for a differential amplifier can degrade the common mode rejection ratio. Figure 5 shows an adjustment circuit which has minimal effect on the common mode rejection. The voltage at the arm of the pot is divided by R_4 and R_5 to supply an offset correction of ±7.5 mV. R_4 and R_5 are chosen such that the common mode rejection ratio is limited by the amplifier for values of R_3 greater than 1 kΩ. If R_3 is less than 1K the shunting of R_4 by R_5 must be considered when choosing the value of R_3.

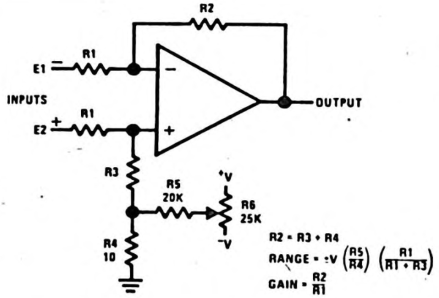


FIGURE 5. Offset Voltage Adjustment for Differential Amplifiers

The techniques described for balancing offset voltage at the input of the amplifier offer two main advantages: First, they are universally applicable to all operational amplifiers and allow device interchangeability with no modifications to the balance circuitry. Second, they permit balancing without interfering with the internal circuitry of the amplifier. The electrical parameters of the amplifiers are tested and guaranteed without balancing. Although it doesn't usually happen, balancing could degrade performance.

IC Regulators Simplify Power Supply Design

National Semiconductor
Linear Brief 10
Robert C. Dobkin
January 1970

Although power supply requirements vary, IC voltage regulators can fulfill the majority of needs. Power supplies designed with ICs can give predictable regulation better than 0.1% with a minimum of engineering effort. Output voltages between 0 and 40V at currents of 10A are easily achieved. Further, with a minimum of changes, a single regulator circuit can be used for a wide variety of output voltages and currents.

A basic 200 mA positive regulator circuit is shown in Figure 1. The LM105[1] contains the voltage reference and control circuitry while the external components set the output voltage, current limit and increase power handling capacity of the IC. The output voltage is set by R_2 and R_3. A fraction of the output voltage is compared by an error amplifier with an internal 1.8V reference. Any error is amplified and used to drive the 2N3740 power transistor. Since the open loop gain is large, there is little error and a high degree of regulation.

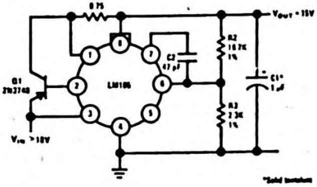


FIGURE 1. 200 mA Positive Regulator

Current limiting is set by R_1. The voltage drop across R_1 is applied to the emitter base junction of a transistor in the IC. When the transistor is turned on, it removes drive from the series pass transistor; and the regulator output exhibits a constant current characteristic. Since the turn on voltage of a transistor is temperature dependent, so is the current limit. The current limit sense voltage is about 0.4V at 25°C decreasing linearly to 0.3V at 125°C. Therefore, the current limit resistor must be chosen to provide adequate output current at the maximum operating temperature.

To regulate negative voltages, the circuit in Figure 2 is used. An LM104[2] contains the voltage reference and control circuitry while an external transistor is used to increase the power handling capacity. A reference voltage is generated by driving a constant current, determined by R_1, through R_2. The voltage across this resistor is fed into an error amplifier. The error amplifier controls the output voltage at twice the voltage across R_2. The output voltage is resistor programmable with R_2 and adjustable down to zero.

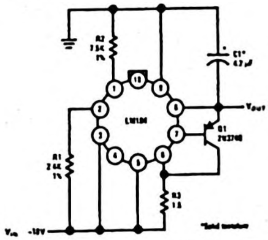


FIGURE 2. 200 mA Negative Regulator

Current limit in the LM104 is similar to the LM105. Voltage across R_3 turns on an internal transistor that decreases drive to the output transistors. This current limit sense voltage is also temperature dependent, decreasing from 0.65V at 25°C to 0.45V at 125°C.

Boosting the available output current from 200 mA is relatively simple. Figure 3 shows positive and negative 2A regulators. An additional power transistor increases the current handling capability of the regulator. Adding the boost tran-

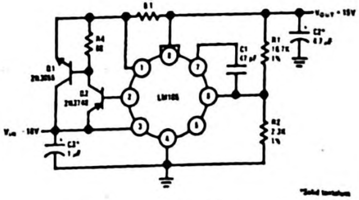


FIGURE 3a. 2A Positive Regulator

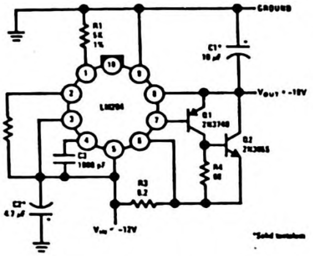


FIGURE 3b. 2A Negative Regulator

sistors increases the output current without increasing the minimum input-output voltage differential. The minimum differential will be 2 to 3V, depending on the drive current required from the integrated circuit and operating temperature. Low input-output voltage differential allows more efficient regulation.

Although the regulators are relatively simple, some precautions must be taken to eliminate possible problems. First, when the regulator is used with boost transistors, a solid tantalum output capacitor is needed. Unlike electrolytics, solid tantalum capacitors have low internal impedance at high frequencies. This suppresses possible high frequency minor loop oscillations as well as providing low output impedance at high frequency. Also, for the LM104, the output capacitor frequency compensates the regulator and must have good frequency characteristics.

The power transistors recommended are single-diffused, wide-base devices. These devices have fewer oscillation problems than double-diffused, planar transistors. Also, they seem less prone to failure under overload conditions. Of course, like the power transistors in any regulator, adequate heat sinking is necessary. The heat sink should keep the transistor junction temperature at an acceptable level for worst case conditions of maximum input voltage, maximum ambient temperature and shorted output. By far, the major cause of regulator failures is inadequate heat sinking.

Good construction techniques ara also important for regulator performance. If proper care is not taken, ground loop errors and lead resistance drops can easily become greater than regulator errors. For example, 0.05" wide, 2 oz. printed circuit conductor has a resistance of about 0.007Ω per inch. For a 200 mA, 15V regulator, ten inches of conductor would decrease the regulation by a factor of 2.

Ground loops are worst yet, since voltage drops can be amplified and appear at the regulator's output. In Figure 3, voltage drops between Pin 4 of the LM105 and the bottom of R_3 are amplified by the ratio of R_2/R_3 and appear at the output.

When the regulator is powered from ac that is rectified and filtered, current flowing in the filter can sometimes cause an unusual ground loop problem. For capacitor input filters, the peak charging current is many times the average load current. Even a few milliohms of resistance can cause appreciable voltage drop during the peak of the charging. When the charging current produces a voltage drop between R_3 and Pin 4 of the LM105, it appears as excessive ripple on the output of the regulator.

Of course, single point grounding eliminates these problems, but this is not always possible. Usually it is sufficient to insure that load current does not generate a voltage drop between the ground side of the voltage setting resistor and the ground of the IC.

In most cases, short circuit protection is the only fault protection needed. However, for some regulator circuits, such as positive and negative regulators used together, additional protection is necessary. If the positive and negative supplies are shorted together, it is possible to cause the output voltage of one of the supplies to reverse, blowing the IC. This is especially true if the current capabilities are different, such as a 200 mA negative supply and a 2A positive supply. A clamp diode between the output and ground of each supply will prevent such polarity reversals. Also, clamp diodes should be used to prevent input polarity reversal and input-output voltage differential reversal.

The use of ICs in regulator circuits can enhance power supply performance while minimizing cost and engineering time. Since only one IC is needed for a wide range of outputs, the part cost, board space and purchasing problems are less when compared to discrete designs. Also engineering time is saved since typical and worst case performance data, as well as application data, is available from the manufacturer before design is begun.

REFERENCES:

1. R.J. Widlar, "An Improved Positive Regulator," *National Semiconductor AN-23*, January, 1969.
2. R.J. Widlar, "Designs for Negative Regulators," *National Semiconductor AN-21*, October, 1968.

The LM110 — An Improved IC Voltage Follower

National Semiconductor
Linear Brief 11
March 1970

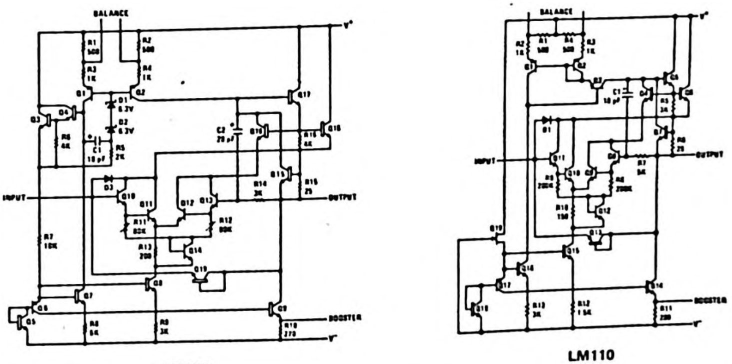
There are quite a few applications where op amps are used as voltage followers. These include sample and hold circuits and active filters as well as general purpose buffers for transducers or other high-impedance signal sources. The general usefulness of such an amplifier is particularly enhanced if it is both fast and has a low input bias current. High speed permits including the buffer in the signal path or within a feedback loop without significantly affecting response or stability. Low input current prevents loading of high impedance sources, which is the reason for using a buffer in the first place.

The LM102, introduced in 1967, was designed specifically as a voltage follower. Therefore, it was possible to optimize performance so that it worked better than general purpose IC amplifiers in this application. This was particularly true with respect to obtaining low input currents along with high-speed operation.

One secret of the LM102's performance is that followers do not require level shifting. Hence, lateral PNP's can be eliminated from the gain path. This has been the most significant limitation on the frequency response of general purpose amplifiers. Secondly, it was the first IC to use super-gain transistors. With these devices, high speed operation can be realized along with low input currents.

The LM110 is a voltage follower that has been designed to supersede the LM102. It is considerably more flexible in its application and offers substantially improved performance. In particular, the LM110 has lower offset-voltage drift, input current and noise. Further, it is faster, less prone to oscillations and operates over a wider range of supply voltages.

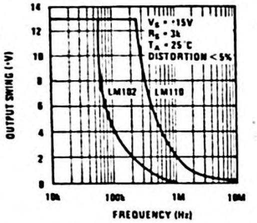
The advantages of the LM110 over the LM102 are described by the following curves. Improvements not included are increased output swing under load, larger small-signal bandwidth, and elimination of oscillations with low-impedance sources. The performance of these devices is also compared with general-purpose op amps in Tables I and II. The advantages of optimizing an IC for this particular slot are clearly demonstrated. Lastly, some typical applications for voltage followers with the performance capability of the LM110 are given.



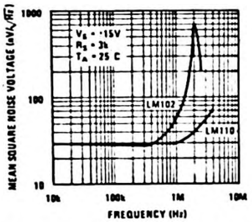
LM102

LM110

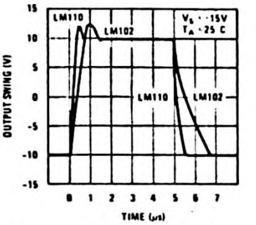
Biggest design difference between the LM102 and LM110 is the elimination of the zener diodes (D1 and D2) in the biasing circuit. This reduces noise and permits operation at low supply voltages.



Power bandwidth of the LM110 is five times larger than the LM102.



Eliminating zeners reduces typical high frequency noise by nearly a factor of 10. Worst case noise is reduced even more. High frequency noise of LM102 has caused problems when it was included inside feedback loop with other IC op amps.



Large signal pulse response shows 40V/µs slew for LM110 and 10V/µs for LM102. Leading edge overshoot on LM110 is virtually eliminated, so external clamp diode frequently required on the LM102 is not needed.

DEVICE	OFFSET** VOLTAGE (mV)	BIAS** CURRENT (nA)	SLEW† RATE (V/µs)	BANDWIDTH† (MHz)	SUPPLY* CURRENT (mA)
LM110	6.0	10	40	20	5.5
LM102	7.5	100	10	10	5.5
MC1556	6.0	30	2.5	1	1.5
µA715	7.5	4000	20	10	7.0
LM108	3.0	3	0.3	1	0.6
LM108A	1.0	3	0.3	1	0.6
LM101A	3.0	100	0.6	1	3.0
µA741	6.0	1500	0.6	1	3.0

**Maximum for −55°C < T_A < 125°C

*Maximum at 25°C

†Typical at 25°C

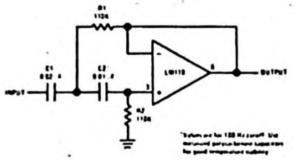
Table I. Comparing Performance of Military Grade IC Op Amps in the Voltage-Follower Connection.

DEVICE	OFFSET* VOLTAGE (mV)	BIAS* CURRENT (nA)	SLEW† RATE (V/µs)	BANDWIDTH† (MHz)	SUPPLY* CURRENT (mA)
LM310	7.5	7.0	40	20	5.5
LM302	15	30	20	10	5.5
MC1456	10	30	2.5	1	1.5
µA715C	7.5	1500	20	10	10
LM308	7.5	7.0	0.3	1	0.8
LM308A	0.5	7.0	0.3	1	0.8
LM301A	7.5	250	0.6	1	3.0
µA741C	6.0	500	0.6	1	3.0

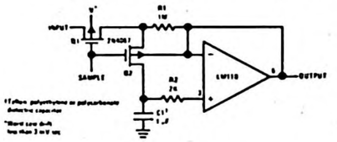
*Maximum at 25°C

†Typical at 25°C

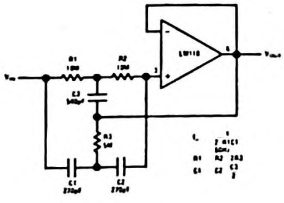
Table II. Comparison of Commercial Grade Devices.



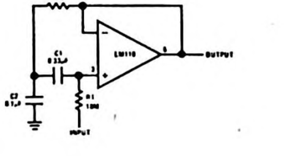
High Pass Active Filter



Low Drift Sample and Hold*



High Q Notch Filter



Bandpass Filter

An IC Voltage Comparator for High Impedance Circuitry

National Semiconductor
Linear Brief 12
January 1970

The IC voltage comparators available in the past have been designed primarily for low voltage, high speed operation. As a result, these devices have high input error currents, which limit their usefulness in high impedance circuitry. An IC is described here that drastically reduces these error currents, with only a moderate decrease in speed.

This new comparator is considerably more flexible than the older devices. Not only will it drive RTL, DTL and TTL logic; but also it can interface with MOS logic and FET analog switches. It operates from standard ±15V op amp supplies and can switch 50V, 50 mA loads, making it useful as a driver for relays, lamps or light-emitting diodes. A unique output stage enables it to drive loads referred to either supply or ground and provide ground isolation between the comparator inputs and the load.

Another useful feature of the circuit is that it can be powered from a single 5V supply and drive DTL or TTL integrated circuits. This enables the designer to perform linear functions on a digital-circuit card without using extra supplies. It can, for example, be used as a low-level photodiode detector, a zero crossing detector for magnetic transducers, an interface for high-level logic or a precision multivibrator.

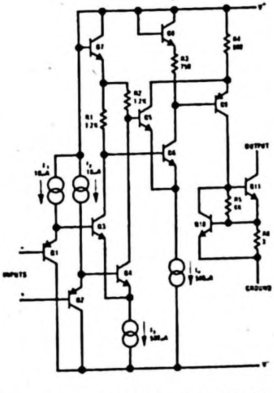


FIGURE 1. Simplified Schematic of the LM111

Figure 1 shows a simplified schematic of this versatile comparator. PNP transistors buffer the differential input stage to get low input currents without sacrificing speed. Because the emitter base breakdown voltage of these PNPs is typically 70V, they can also withstand a large differential input voltage. The PNPs drive a standard differential stage. The output of this stage is further amplified by the Q_5-Q_6 pair. This feeds a lateral PNP, Q_9, that provides additional gain and drives the output stage.

The output transistor is Q_{11} which is driven by the level shifting PNP. Current limiting is provided by R_6 and Q_{10} to protect the circuit from intermittent shorts. Both the output and the ground lead are isolated from other points within the circuit, so either can be used as the output. The V^- terminal can also be tied to ground to run the circuit from a single supply. The comparator will work in any configuration as long as the ground terminal is at a potential somewhere between the supply voltages. The output terminal, however, can go above the positive supply as long as the breakdown voltage of Q_{11} is not exceeded.

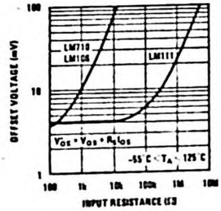


FIGURE 2. Illustrating the Influence of Source Resistance on Worst Case, Equivalent Input Offset Voltage.

Figure 2 shows how the reduced error currents of the LM111 improve circuit performance. With the LM710 or LM106, the offset voltage is degraded for source resistances above 200Ω. The LM111, however, works well with source resistances in excess of 30 kΩ. Figure 2 applies for equal source resistances on the two inputs. If they are unequal, the degradation will become pronounced at lower resistance levels.

Table I gives the important electrical characteristics of the LM111 and compares them with the specifications of older ICs.

A few, typical applications of the LM111 are illustrated in Figure 3. The first is a zero crossing detector driving a MOS analog switch. The ground terminal of the IC is connected to V^-; hence, with ±15V supplies, the signal swing delivered to the gate of Q_1 is also ±15V. This type of circuit is useful where the gain or feedback configuration of

Table I. Comparing the LM111 with earlier IC comparators. Values given are worst case over a −55°C to 125°C temperature range, except as noted.

Parameter	LM111	LM106	LM710	Units
Input Offset Voltage	4	3	3	mV
Input Offset Current	0.02	7	7	μA
Input Bias Current	0.15	45	45	μA
Common Mode Range	±14	±5	±5	V
Differential Input Voltage Range	±30	±5	±5	V
Voltage Gain†	200	40	1.7	V/mV
Response Time†	200	40	40	ns
Output Drive				
Voltage	50	24	2.5	V
Current	50	100	1.6	mA
Fan Out (DTL/TTL)	8	16	1	
Power Consumption	80	145	160	mW

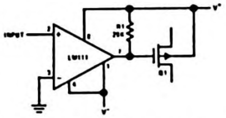
†Typical at 25°C.

an op amp circuit must be changed at some precisely-determined signal level. Incidentally, it is a simple matter to modify the circuit to work with junction FETs.

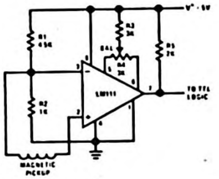
The second circuit is a zero crossing detector for a magnetic pickup such as a magnetometer or shaft-position pickoff. It delivers the output signal directly to DTL or TTL logic circuits and operates from the 5V logic supply. The resistive divider, R_1 and R_2, biases the inputs 0.5V above ground, within the common mode range of the device. An optional offset balancing circuit, R_3 and R_4, is included.

The next circuit shows a comparator for a low-level photodiode operating with MOS logic. The output changes state when the diode current reaches 1 μA. At the switching point, the voltage across the photodiode is nearly zero, so its leakage current does not cause an error. The output switches between ground and −10V, driving the data inputs of MOS logic directly.

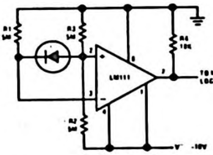
The last circuit shows how a ground-referred load is driven from the ground terminal of the LM111. The input polarity is reversed because the ground terminal is used as the output. An incandescent lamp, which is the load here, has a cold resistance eight times lower than it is during normal operation. This produces a large inrush current, when it is switched on, that can damage the switch. However, the current limiting of the LM111 holds this current to a safe value.



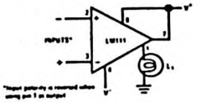
a. Zero Crossing Detector Driving Analog Switch



b. Detector for Magnetic Transducer



c. Comparator for Low Level Photodiode



d. Driving Ground–Referred Load

FIGURE 3. Typical Applications of the LM111.

The applications described above show that the output-circuit flexibility and wide supply-voltage range of the LM111 opens up new fields for IC comparators. Further, its low error currents permit its use in circuits with impedance levels above 1 kΩ. Although slower than older devices, it is more than an order of magnitude faster than op amps used as comparators.

The LM111 has the same pin configuration as the LM710 and LM106. It is interchangeable with these devices in applications where speed is not of prime concern.

Speed Up the LM108 Feedforward Compensation

National Semiconductor
Linear Brief 14
Robert C. Dobkin
November 1970

Feedforward frequency compensation of operational amplifiers can provide a significant increase in slew rate and bandwidth over standard lag compensation. When feedforward compensation is applied to the LM101A operational amplifier,[1] an order of magnitude increase in bandwidth results. A simple feedforward network has also been developed for use with the LM108 micropower amplifier to give a factor of five improvement in speed. It uses no active components and does not degrade the excellent dc characteristics of the LM108.

Figure 1 shows a schematic of an LM108 using the new compensation. The signal from the inverting input is fed forward around the input stage by a 500 pF capacitor, C_1. At high frequencies it provides a phase lead. With this lead, overall phase shift is reduced and less compensation is needed to keep the amplifier stable. The $C_2 - R_1$ network provides lag compensation, insuring that the open loop gain is below unity before 180° phase shift occurs. The open loop gain and phase as a function of frequency is compared with standard compensation in Figure 2.

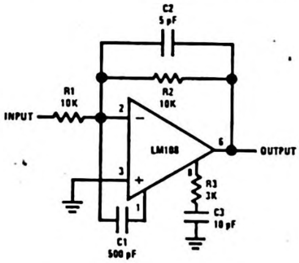


FIGURE 1. LM108 with Feedforward Compensation

The slew rate is increased from 0.3V/μs to about 1.3V/μs and the 1 kHz gain is increased from 500 to 10,000. Small signal bandwidth is extended to 3 MHz. The bandwidth must be limited to 3 MHz because the phase shift through the lateral PNP transistors used in the second stage becomes excessive at higher frequencies. With the LM101A, 10 MHz bandwidth was possible since the signal was bypassed around the low frequency lateral PNP's. Nonetheless, 3 MHz is very respectable for a micropower amplifier drawing only 300 μA quiescent current.

When the LM108 is used with feedforward compensation, it is less tolerant of capacitive loading and stray capacitance. Precautions must be taken to insure stability. If load capacitance is greater than about 75 to 100 pF, it must be isolated as shown in Figure 3. A small capacitor is always needed to provide a lead across the feedback resistor to compensate for strays at the input. About 3 to 5 pF is the minimum value capacitor. Care must be taken to minimize stray capacitance at Pins 1, 2 and 8 when feedforward compensation is used. Additionally, when the source resistance on the noninverting input is greater than 10k, it should be bypassed with a .01 μF capacitor.

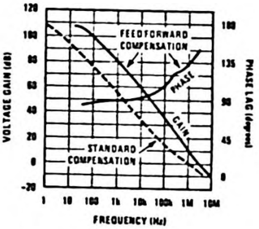


FIGURE 2. Open Loop Voltage Gain

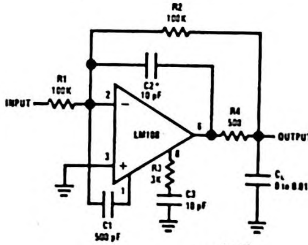


FIGURE 3. Decoupling Load Capacitance

As with any externally compensated amplifier, increasing the compensation of the LM108 increases the stability at the expense of slew and bandwidth. The circuit shown is for the fastest response. Increasing the size of C_2 to 20 or 30 pF will provide 2 or 3 times greater stability and capacitive load tolerance. Therefore, the size of the compensation capacitor should be optimized for the bandwidth of the particular application.

The stability of the LM108 with feedforward compensation is indicated by the small signal transient responses shown in Figure 4. It is quite stable since there is little overshoot and ringing even though the amplifier is loaded with a 50 pF capacitor. Large signal transient response for a 20V square wave is shown in Figure 5. The small positive overshoot is not severe and usually causes no problems.

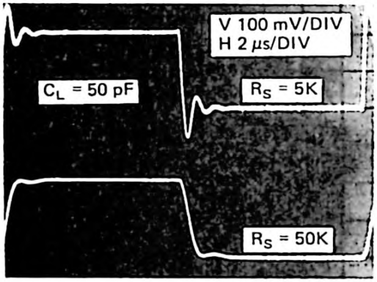


FIGURE 4. Small Signal Transient Response of LM108 with Feedforward Compensation

The LM108 is unusually insensitive to power supply bypassing with the new compensation. Even with several feet of wire between the device and power supply, it does not become unstable. However, it is still wise to bypass the supplies for drill since noise on the V^+ line can be injected to the summing junction by the 500 pF feedforward capacitor.

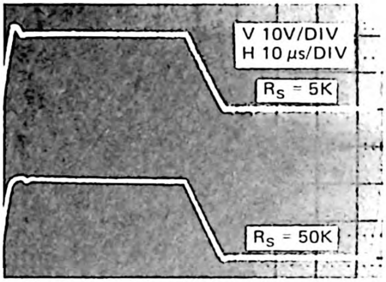


FIGURE 5. Large Signal Transient Response of LM108 with Feedforward Compensation

The new feedforward compensation is easy to use and offers a factor of five improvement over standard compensation. Slew rate is increased to 1.3V/μs and power bandwidth extended to 20 kHz. Also, gain error at high frequencies is reduced. This makes the LM108 more useful in precision applications where low dc error as well as low ac error is desired.

REFERENCE:

1. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2,* March, 1969.

High Stability Regulators

National Semiconductor
Linear Brief 15
Robert C. Dobkin
January 1971

Monolithic IC's have greatly simplified the design of general purpose power supplies. With an IC regulator and a few external components 0.1% regulation with 1% stability can be obtained. However, if the application requires better performance, it is advisable to use some other design approach.

Precision regulators can be built using an IC op amp as the control amplifier and a discrete zener as a reference, where the performance is determined by the reference. Figures 1 and 2 show schematics of simple positive and negative regulators. They are capable of providing better than 0.01% regulation for worst case changes of line, load and temperature. Typically, the line rejection is 120 dB to 1 kHz; and the load regulation is better than 10 µV for a 1A change. Temperature is the worst source of error; however, it is possible to achieve less than a 0.01% change in the output voltage over a −55°C to +125°C range.

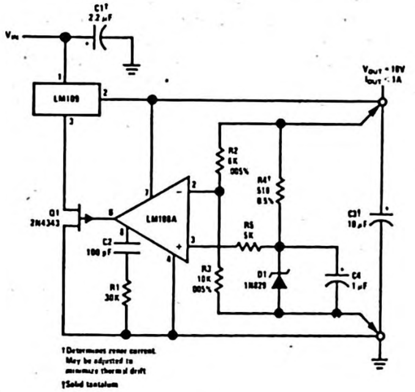


FIGURE 1. High Stability Positive Regulator

The operation of both regulators is straightforward. An internal voltage reference is provided by a high-stability zener diode. The LM108A[1] operational amplifier compares a fraction of the output voltage with reference. In the positive regulator, the output of the op amp controls the ground terminal of an LM109[2] regulator through source follower, Q_1. Frequency compensation for the regulator is provided by both the $R_1 C_2$ combination and output capacitor, C_3.

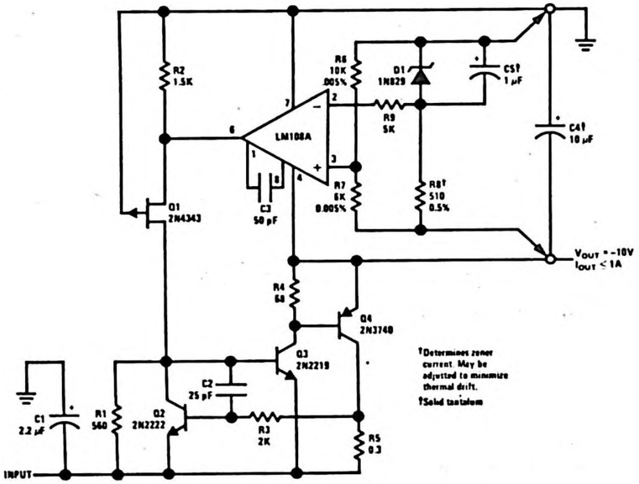
The negative regulator shown in Figure 2 operates similarly, except that discrete transistors are used for the pass element. A transistor, Q_1, level shifts the output of the LM108 to drive output transistors, Q_3 and Q_4. Current limiting is provided by Q_2. Capacitors C_3 and C_4 frequency compensate the regulator.

In the positive regulator the use of an LM109 instead of discrete power transistors has several advantages. First, the LM109 contains all the biasing and current limit circuitry needed to supply a 1A load. This simplifies the regulator. Second, and probably most important, the LM109 has thermal overload protection, making the regulator virtually burn-out proof. If the power dissipation becomes excessive or if there is inadequate heat sinking, the LM109 will turn off when the chip temperature reaches 175°C, preventing the device from being destroyed. Since no such device is available for use in the negative regulator, the heat sink should be large enough to keep the junction temperature of the pass transistors at an acceptable level for worst case conditions of maximum ambient temperature, maximum input voltage and shorted output.

Although the regulators are relatively simple, some precautions must be taken to eliminate possible problems. A solid tantalum output capacitor must be used. Unlike electrolytics, solid tantalum capacitors have low internal impedance at high frequencies. Low impedance is needed both for frequency compensation and to eliminate possible minor loop oscillations. The power transistor recommended for the negative regulator is a single-diffused wide-base device. This transistor type has fewer oscillation problems than double diffused transistors. Also, it seems less prone to failure under overload conditions.

Some unusual problems are encountered in the construction of a high stability regulator. Component choice is most important since the resistors, amplifier and zener can contribute to temperature drift. Also, good circuit layout is needed to eliminate the effect of lead drops, pickup, and thermal gradients.

The resistors must be low-temperature-coefficient wirewound or precision metal film. Ordinary 1% carbon film, tin oxide or metal film units are not suitable since they may drift as much as 0.5% over temperature. The resistor accuracy need not be 0.005% as shown in the schematic; however, they should track better than 1 ppm/°C. Additionally, wirewound resistors usually have lower thermoelectric effects than film types. The resistor driving



†Determines zener current. May be adjusted to minimize thermal drift.

†Solid tantalum

FIGURE 2. High Stability Negative Regulator

the zener is not quite as critical; but it should change less than 0.2% over temperature.

The excellent dc characteristics of the LM108A make it a good choice as the control amplifier. The offset voltage drift of less than 5 μV/°C contributes little error to the regulator output. Low input current allows standard cells to be used for the voltage reference instead of a reference diode. Also the LM108 is easily frequency compensated for regulator applications.

Of course, the most important item is the reference. The IN829 diode is representative of the better zeners available. However, it still has a temperature coefficient of 0.0005%/°C or a maximum drift of 0.05% over a −55°C to 125°C temperature range. The drift of the zener is usually linear with temperature and may be varied by changing the operating current from its nominal value of 7.5 mA. The temperature coefficient changes by about 50 μV/°C for a 15% change in operating current. Therefore, by adjusting the zener current, the temperature drift of the regulator may be minimized.

Good construction techniques are important. It is necessary to use remote sensing at the load, as is shown on the schematics. Even an inch of wire will degrade the load regulation. The voltage setting resistors, zener, and the amplifier should also be shielded. Board leakages or stray capacitance can easily introduce 100 μV of ripple or dc error into the regulator. Generally, short wire length and single-point grounding are helpful in obtaining proper operation.

REFERENCES:

1. R.J. Widlar, "IC Op Amp Beats FETs on Input Current," *National Semiconductor AN-29,* December, 1969.
2. R.J. Widlar, "New Developments in IC Voltage Regulators," in *1970 International Solid-State Circuits Conference Digest of Technical Papers,* Vol. XIII, pp. 158-159.

Easily Tuned Sine Wave Oscillators

National Semiconductor
Linear Brief 16
Robert C. Dobkin
March 1971

One approach to generating sine waves is to filter a square wave. This leaves only the sine wave fundamental as the output. Since a square wave is easily amplitude stabilized by clipping, the sine wave output is also amplitude stabilized. A clipping oscillator eliminates the problems encountered with agc stablized oscillators such as those using Wein bridges. Additionally, since there is no slow agc loop, the oscillator starts quickly and reaches final amplitude within a few cycles.

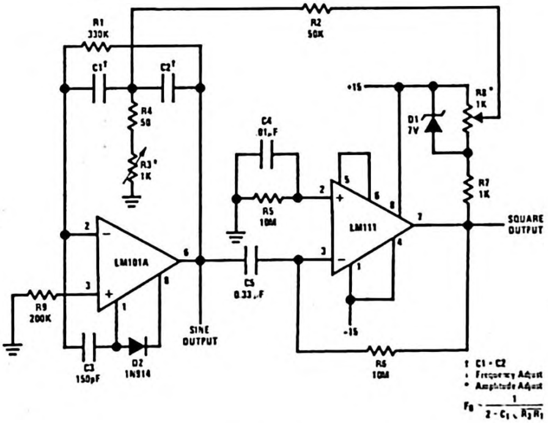


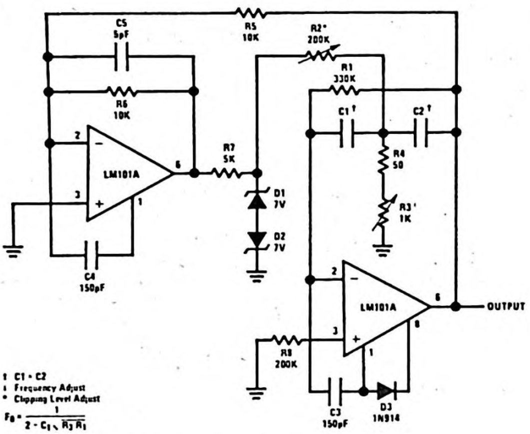
FIGURE 1. Easily Tuned Sine Wave Oscillator

The circuit in Figure 1 will provide both a sine and square wave output for frequencies from below 20 Hz to above 20 kHz. The frequency of oscillation is easily tuned by varying a single resistor. This is a considerable advantage over Wein bridge circuits where two elements must be tuned simultaneously to change frequency. Also, the output amplitude is relatively stable when the frequency is changed.

An operational amplifier is used as a tuned circuit, driven by square wave from a voltage comparator. Frequency is controlled by R_1, R_2, C_1, C_2, and R_3, with R_3 used for tuning. Tuning the filter does not affect its gain or bandwidth so the output amplitude does not change with frequency. A comparator is fed with the sine wave output to obtain a square wave. The square wave is then fed back to the input of the tuned circuit to cause oscillation. Zener diode, D_1, stabilizes the amplitude of the square wave fed back to the filter input. Starting is insured by R_6 and C_5 which provide dc negative feedback around the comparator. This keeps the comparator in the active region.

If a lower distortion oscillator is needed, the circuit in Figure 2 can be used. Instead of driving the tuned circuit with a square wave, a symmetrically clipped sine wave is used. The clipped sine wave, of course, has less distortion than a square wave and yields a low distortion output when filtered. This circuit is not as tolerant of component values as the one shown in Figure 1. To insure oscillation, it is necessary that sufficient signal is applied to the zeners for clipping to occur. Clipping about 20% of the sine wave is usually a good value. The level of clipping must be high enough to insure oscillation over the entire tuning range. If the clipping is too small, it is possible for the circuit to cease oscillation due to tuning, component aging, or temperature changes. Higher clipping levels increase distortion. As with the circuit in Figure 1, this circuit is self-starting.

Table 1 shows the component values for the various frequency ranges. Distortion from the circuit in Figure 1 ranges between 0.75% and 2% depending on the setting of R_3. Although greater tuning range can be accomplished by increasing the size of R_3 beyond 1kΩ, distortion becomes



† C1 = C2
‡ Frequency Adjust
* Clipping Level Adjust

$F_0 = \frac{1}{2\pi C_1 \sqrt{R_3 R_1}}$

FIGURE 2. Low Distortion Sine Wave Oscillator

excessive. Decreasing R_3 lower than 50Ω can make the filter oscillate by itself. The circuit in Figure 2 varies between 0.2% and 0.4% distortion for 20% clipping.

About 20 kHz is the highest usable frequency for these oscillators. At higher frequencies the tuned circuit is incapable of providing the high Q bandpass characteristic needed to filter the input into a clean sine wave. The low frequency end of oscillation is not limited except by capacitor size.

TABLE 1

C_1, C_2	MIN. FREQUENCY	MAX. FREQUENCY
0.47 μF	18 Hz	80 Hz
0.1 μF	80 Hz	380 Hz
.022 μF	380 Hz	1.7 kHz
.0047 μF	1.7 kHz	8 kHz
.002 μF	4.4 kHz	20 kHz

In both oscillators, feedforward compensation[3] is used on the LM101A amplifiers to increase their bandwidth. Feedforward increases the bandwidth to over 10 MHz and the slew rate to better than 10V/μs. With standard compensation the maximum output frequency would be limited to about 6 kHz.

Although these oscillators are not particularly tricky, good construction techniques are important. Since the amplifiers and the comparators are both wide band devices, proper power supply bypassing is in order. Both the positive and negative supplies should be bypassed with a 0.1μF disc ceramic capacitor. The fast transition at the output of the comparator can be coupled to the sine wave output by stray capacitance, causing spikes on the output. Therefore the output of the comparator with the associated circuitry should be shielded from the inputs of the op amp.

Component choice is also important. Good quality resistors and capacitors must be used to insure temperature stability. Capacitor should be mylar, polycarbonate, or polystyrene — electrolytics will not work. One percent resistors are usually adequate.

The circuits shown provide an easy method of generating a sine wave. The frequency of oscillation can be varied over greater than a 4 to 1 range by changing a single resistor. The ease of tuning as well as the elimination of critical agc loops make these oscillators well suited for high volume production since no component selection is necessary.

References:

1. N.P. Doyle, "Swift, Sure Design of Active Bandpass Filters," *EDN*, Vol. 15, No. 2, January 15, 1970.
2. R.J. Widlar, "Precision IC Comparator Runs from 5V Logic Supply," *National Semiconductor AN-41*, October, 1970.
3. Robert C. Dobkin, "Feedforward Compensation Speeds Op Amp," *National Semiconductor LB-2*, March, 1969.

LM118 Op Amp Slews 70V/μsec

National Semiconductor
Linear Brief 17
Robert C. Dobkin
September 1971

One of the greatest limitations of today's monolithic op amps is speed. With unity gain frequency compensation, general purpose op amps have 1 MHz bandwidth and 0.3 V/μs slew rate. Optimized compensation as well as feedforward compensation can improve op amp speed for some applications. Specialized devices such as fast, unity-gain buffers are available which provide partial solutions. This paper will describe a new high speed monolithic amplifier that offers an order of magnitude increase in speed with no loss in flexibility over general purpose devices.

The LM118 is constructed by the standard six mask monolithic process and features 15 MHz bandwidth and 70 V/μs slew rate. It operates over a ±5 to ±18V supply range with little change in speed. Additionally, the device has internal unity-gain frequency compensation and needs no external components for operation. However, unlike other internally compensated amplifiers, external feedforward compensation may be added to approximately double the bandwidth and slew rate.

DESIGN CONCEPTS

In general purpose amplifiers the unity-gain bandwidth is limited by the lateral PNP transistors used for level shifting. The response above 2 MHz is so poor that they cannot be used in a feedback amplifier. If the PNP transistors are used for level shifting only at DC or low frequencies and the signal is fed forward around the PNP transistors at high frequencies, wide bandwidth can be obtained without the excessive phase shift of the PNP transistors.

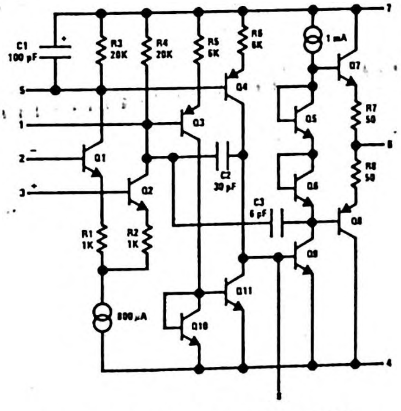


FIGURE 1. Simplified Circuit of the LM118

Figure 1 shows a simplified schematic of the LM118. Transistors Q_1 and Q_2 are a conventional differential input stage with emitter degeneration and resistive collector loads. Q_3 and Q_4 form the second stage which further amplify the signal and level shift the signal towards V^-. The collectors of Q_3 and Q_4 drive a current inverter, Q_{10} and Q_{11} to convert from differential to single ended. Q_9, which has a current source load for high gain, drives a class B output. The collectors of the input stage and the base of Q_9 are available for offset balancing and external compensation.

Frequency compensation is accomplished with three internal capacitors. C_1 rolls off on half the differential input stage so that the high frequency signal path is single-ended. Also, at high frequencies, the signal is fed forward around the lateral PNP transistors by a 30 pF capacitor, C_2. This eliminates the excessive phase shift. Overall frequency response is then set by capacitor, C_3, which rolls off the amplifier at 6 dB/octive. As previously mentioned feedforward compensation for inverting applications can be applied to the base of Q_9. Figure 2 shows the open loop frequency response of an LM118. Table 1 gives typical specifications for the new amplifier.

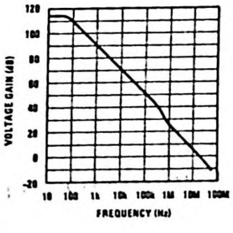


FIGURE 2. Open Loop Voltage Gain as a Function of Frequency for LM118.

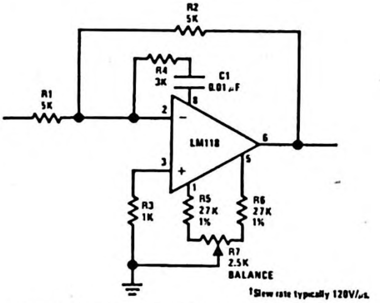
TABLE 1. Typical Specifications for the LM118

Input Offset Voltage	2 mV
Input Bias Current	200 nA
Offset Current	20 nA
Voltage Gain	200K
Common Mode Range	±11.5V
Output Voltage Swing	±13V
Small Signal Bandwidth	15 MHz
Slew Rate	70 V/μs

OPERATING CONFIGURATION

Although considerable effort was taken to make the LM118 trouble free, high frequency amplifiers are more prone to oscillations than low frequency devices such as the LM101A. Care must be taken to minimize the stray capacitance at the inverting input and at the output; however the LM118 will drive a 100 pF load. Good power supply bypassing is also in order—0.1 μF disc ceramic capacitors should be used within a few inches of the amplifier. Additionally, a small capacitor is usually necessary across the feedback resistor to compensate for unavoidable stray capacitance.

Figure 3 shows feedforward compensation of the LM118 for fast inverting applications. The signal is fed from the summing junction to the output stage driver by C_1 and R_4. Resistors R_5, R_6 and R_7 have two purposes: they increase the internal operating current of the output stage to increase slew rate and they provide offset balancing. The current boost is necessary to drive internal stray capacitance at the higher slew rate. Mismatch of the external resistors can cause large voltage offsets so offset balancing is necessary. For supply voltages other than ±15V, R_5 and R_6 should be selected to draw about 500 μA from Pins 1 and 5.

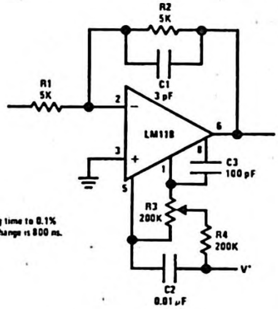


†Slew rate typically 120V/μs.

FIGURE 3. Feedforward Compensation for Greater Inverting Slew Rate†

When using feedforward, resistor R_4 should be optimized for the application. It is necessary to have about 8 kΩ in the path from the output of the amplifier through the feedback resistor and through feedforward network to Pin 8 of the device. The series resistance is needed to limit the bandwidth and prevent minor loop oscillation. At high gains, or with high value feedback resistors R_4 can be quite low—but not less than 100Ω. When the LM118 is used a fast integrator, with a large feedback capacitor or with low values of feedback resistance, R_4 must be increased to 8 kΩ to insure stability over a full −55°C to 125°C temperature range.

One of the more important considerations for a high speed amplifier is settling time. Poor settling time can cancel the advantages of having high slew rate and bandwidth. For example—an amplifier can have severe ringing after a step input. A relatively long time is then needed before the output voltage can be read accurately. Settling time is the time necessary for the output to slew through a defined voltage change and settle to within a defined error of its final output voltage. Figure 4 shows optimized compensation for settling to within 0.1% error. Typically the settling time is 800 ns for a simple inverter circuit as shown. Settling time is, of course, subject to operating conditions external to the IC such as closed loop gain, circuit layout, stray capacitance and source resistance. An optional offset balancing circuit, R_3 and R_4 is included.



†Slew and settling time to 0.1% for a 10V step change is 800 ns.

FIGURE 4. Compensation for Minimum Settling† Time

The LM118 opens up new fields for IC operational amplifiers. It is more than an order of magnitude faster than general purpose amplifiers while retaining the ease of use features. It is ideally suited for analog to digital converters, active filters, sample and hold circuits and wide band amplification. Further, the LM118 has the same pin configuration as the LM101A or LM741 and is interchangeable with these devices when speed is of prime concern.

+5 to −15 Volts DC Converter

National Semiconductor
Linear Brief 18
Helge H. Mortensen
July 1972

INTRODUCTION

It is frequently necessary to convert a DC voltage to another higher or lower DC-voltage while maximizing efficiency. Conventional switching regulators are capable of converting from a high input DC voltage to a lower output voltage and satisfying the efficiency criteria. The problem is a little more troublesome if a higher output voltage than the input voltage is desired. Particularly, generating DC voltage with opposite polarity to the input voltage usually involves a complicated design.

This brief demonstrates the use of the switching regulator idea for a +5 volts to −15 volts converter. The converter has an application as a power supply for MOS memories in a logic system where only +5 volts is available. However, the principle used can be applied for almost any input output combination.

OPERATION

The method by which the regulator generates the opposite polarity is explained in Figure 1. The transistor Q is turned ON and OFF with a given duty cycle. If the base drive is sufficient the voltage across the inductor is equal to the supply voltage minus V_{SAT}. The current change in the inductor is given by:

$$\Delta I = \frac{V_{SS} - V_{SAT}}{L} \times T_{ON} \approx \frac{V_{SS}}{L} T_{ON} \quad (1)$$

Turning OFF the transistor the inductor current has a path through the catch diode and this in turn builds up a negative voltage across R_L.

The figure also shows the current and voltage levels versus time. A capacitor in parallel to the resistor will prevent the voltage from dropping to zero during the transistor ON time.

Assuming a large capacitor, we can also write the current change as:

$$\Delta I = \frac{V_{OUT} - V_D}{L} \times T_{OFF} \approx \frac{V_{OUT}}{L} \times T_{OFF} \quad (2)$$

In order to get a general idea of the operation for certain input output conditions, we will develop a set of equations.

During the transistor ON time, energy is loaded into the inductor. In the same time interval, the capacitor is drained due to the load resistor R_L.

Drop in capacitor voltage:

$$\Delta V = \frac{I_{LOAD} \times T_{ON}}{C} \quad (3)$$

During the T_{OFF} time the stored energy in the inductor is transferred to the load and capacitor. A rough estimate of T_{OFF} can be expressed as:

$$T_{OFF} = \frac{V_{SS}}{V_{OUT}} \times T_{ON} \quad (4)$$

The capacitor voltage will be restored with a average current given by:

$$I_C = \frac{\Delta V \times C}{T_{OFF}} = \frac{I_{LOAD} \times V_{OUT}}{V_{SS}} \quad (5)$$

The total inductor current during the OFF time can be written as:

$$I_{INDUCTOR} = I_{LOAD} + I_C \quad (6)$$

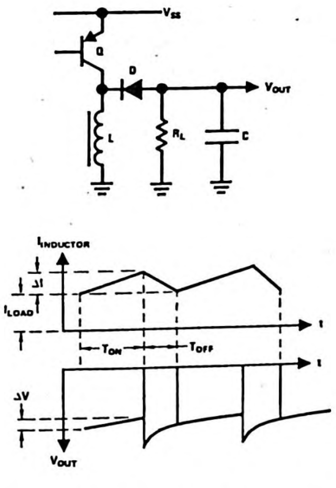
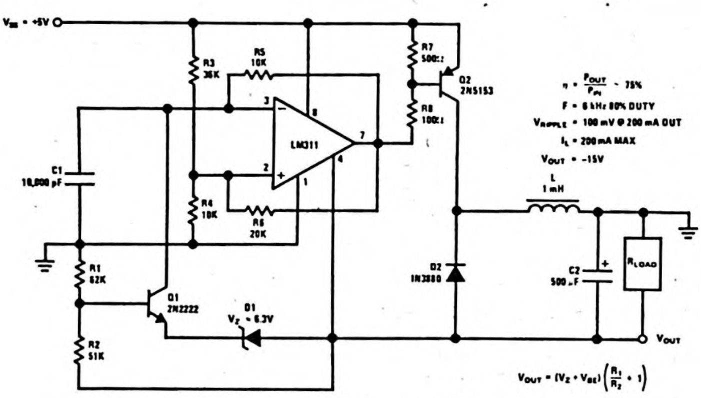


FIGURE 1. Switching Circuit for Voltage Conversion



V_{SS} = +5V
R3
36K
R5
10K
R7
500Ω
Q2
2N5153
R8
100Ω
$\eta = \frac{P_{OUT}}{P_{IN}} \sim 75\%$
F = 6 kHz 80% DUTY
V_{RIPPLE} = 100 mV @ 200 mA OUT
I_L = 200 mA MAX
V_{OUT} = −15V
L
1 mH
3
2
8
7
4
1
LM311
C1
10,000 pF
R4
10K
R6
20K
R1
62K
R2
51K
Q1
2N2222
D1
V_Z = 6.3V
D2
1N3880
C2
500 µF
R_{LOAD}
V_{OUT}
$V_{OUT} = (V_Z + V_{BE})\left(\frac{R_1}{R_2} + 1\right)$

FIGURE 2. Switching Regulator for Voltage Conversion

Inspecting Figure 1. We find:

$$I_C = \frac{\Delta I}{2} = \frac{V_{SS} \times T_{ON}}{2 \times L} \qquad (7)$$

which yields:

$$T_{ON} = \frac{2 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \qquad (8)$$

Taking into account that the efficiency is in the order of 75% the final expression is:

$$T_{ON} = \frac{1.5 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \qquad (9)$$

The above equations will be applied to the regulator shown at Figure 2. The regulator must deliver −15 volts at 200 mA from a +5 volt supply. Using a 1 mH inductor the T_{ON} time for Q_2 is 0.18 ms from equation 9. T_{OFF} is 60 µs from equation 4 and the oscillator frequency to:

$$F = \frac{1}{T_{ON} + T_{OFF}} \approx 4 \text{ kHz}$$

The LM311 performs a free running multivibrator with high duty cycle. The IC is designed to operate from a standard single 5 volt supply and has a high output current capability for driving the switching transistor Q_2. The duty cycle is given by the voltage divider R_3 and R_4 and the frequency of C_1 in conjunction with R_5.

By setting the duty cycle higher than first calculated, the output voltage will tend to increase above the desired output voltage of 15 volts. However, an extra loop performed by Q_1 and the zener diode in conjunction with the resistor network will modify the oscillator duty cycle until the desired output level is obtained.

The output voltage is given by:

$$V_{OUT} = (V_Z + V_{BE})\left(\frac{R_1}{R_2} + 1\right)$$

Data and results obtained with the design:

V_{IN} = 5 volts
V_{OUT} = −15 volts
I_{OUT} = max 200 mA
Efficiency ≅ 75%
Frequency ≅ 6 kHz 80% duty cycle
V_{RIPPLE} ≅ 100 mV @ 200 mA load
Line regulation: V_{IN} = 5V to 10V $< 3\%\ V_{OUT}$
I_{LOAD} = 200 mA
Load regulation: V_{IN} = 5V $< 3\%\ V_{OUT}$
I_{LOAD} = 0 – 100 mA

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Widlar, R. J., *"Designing Switching Regulators"*, AN2, National Semiconductor Corp.

Predicting Op Amp Slew Rate Limited Response

National Semiconductor
Linear Brief 19
Marvin Vander Kooi
August 1972

The following analysis of sine and step voltage responses applies to all single dominant pole op amps such as the LM101A, LM107, LM108A, LM112, LM118 and the LM741. Each of these op amps has an open loop response curve with a shape similar to the one shown in Figure 1. The distinguishing feature of this curve is the single low frequency turnover from a flat response to a uniform −20 dB per decade of frequency (−6 dB/octave) drop in gain, at least until the curve passes through the 0 dB line. Closing the loop to 40 dB (X100) as shown with a dotted line on Figure 1 does not change the shape of the curve, but it does move the turnover to a higher frequency. These open loop and closed loop response curves determine the gain applied to small signal inputs. The logical question then arises as to when a signal can no longer be treated as a small signal and the amplifier response begins to deviate from this curve.

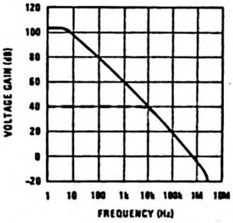

FIGURE 1. Open and Closed Loop Frequency Response

The answer lies in the slew rate limit of the op amp. The slew rate limit is the maximum rate of change of the amplifier's output voltage and is due to the fact that the compensation capacitor inside the amplifier only has finite currents[1] available for charging and discharging. A sinusoidal output signal will cease being small signal when its maximum rate of change equals the slew rate limit S_r of the amplifier. The maximum rate of change for a sine wave occurs at the zero crossing and may be derived as follows:

$$v_o = V_p \sin 2\pi\, ft \qquad (1)$$

$$\frac{dv_o}{dt} = 2\pi f V_p \cos 2\pi\, ft \qquad (2)$$

$$\left.\frac{dv_o}{dt}\right|_{t=0} = 2\pi f V_p \qquad (3)$$

$$S_r = 2\pi f_{max} V_p \qquad (4)$$

where: v_o = output voltage
V_p = peak output voltage
S_r = maximum $\frac{dv_o}{dt}$

The maximum sine wave frequency an amplifier with a given slew rate will sustain without causing the output to take on a triangular shape is therefore a function of the peak amplitude of the output and is expressed as:

$$f_{max} = \frac{S_r}{2\pi V_p} \qquad (5)$$

Equation 5 demonstrates that the borderline between small signal response and slew rate limited response is not just a function of the peak output signal but that by trading off either frequency or peak amplitude one can continue to have a distortion free output. Figure 2 shows a quick reference graphical presentation of equation 5 with the area above any V_{PEAK} line representing an undistorted small signal response and the area below a given V_{PEAK} line representing a distorted sine wave response due to slew rate limiting.

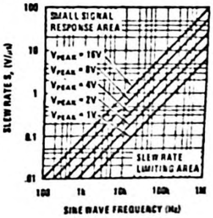

FIGURE 2. Sine Wave Response

As a matter of convenience, amplifier manufacturers often give a "full-power bandwidth" or "large signal response" on their specification sheets.

This frequency can be derived by inserting the amplifier slew rate and peak rated output voltage into equation 5. The bandwidth from DC to the resulting f_{max} is the full-power bandwidth or "large signal response" of the amplifier. For example the full-power bandwidth of the LM741 with a 0.5V µs S_r is approximately 6 kHz while the full-power bandwidth of the LM118 with an S_r of 70 V/µs is approximately 900 kHz.

The step voltage response at the output of an op amp can also be divided into a small signal response and a slew rate limited response. The single turnover and uniform −20 dB/decade slope shown in the small signal frequency response curve of Figure 1 are also characteristic of a low pass filter and one can in fact model an op amp as a low pass RC filter followed by a very wideband amplifier. Figure 3 shows a model of a X100 circuit with a 3 dB down rolloff frequency of 10 kHz. From basic filter theory[2] the 10% to 90% rise time of single pole low pass filter is:

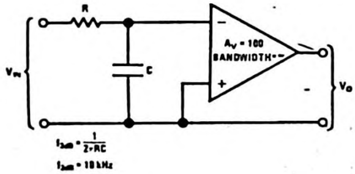

FIGURE 3. Small Signal Op Amp Model

$$t_r = \frac{0.35}{f_{3dB}} \tag{6}$$

which for this example would be 35 µs. Again this small signal or low pass filter response ceases when the required rate of change of the output voltage exceeds the slew rate limit S_r of the amplifier. Mathematically stated:

$$\frac{V_{STEP}}{t_r} \geq S_r \tag{7}$$

This means that as soon as the amplitude of the output step voltage divided by the rise time of the circuit exceeds the S_r of the amplifier, the amplifier will go into slew rate limiting. The output will then be a ramp function with a slope of S_r and a rise time equal to:

$$t_r' = \frac{V_{STEP}}{S_r} \tag{8}$$

Substituting equation 6 into equation 7 gives the critical value of V_{STEP} directly in terms of f_{3dB}:

$$\frac{V_{STEP}\, f_{3dB}}{0.35} \geq S_r \tag{9}$$

which can be graphed as shown in Figure 4. Any point in the area above a V_{STEP} line represents an undistored low pass filter type response and any point in the area below a given V_{STEP} line represents a slew rate limited response.

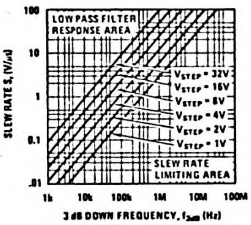

FIGURE 4. Step Voltage Response

The above equations and graphs should allow one to avoid the pitfalls of slew rate limiting and also provide a means of using engineering tradeoffs to extend the response of the single dominant pole type of amplifier.

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2. Millman, J. and Hawkias, C.C.: *"Electronic Devices and Circuits"*, pp 465–466, McGraw-Hill Book Company, New York, 1967.

A Fully Differential Input Voltage Amplifier

National Semiconductor
Linear Brief 20
Helge H. Mortensen
December 1972

INTRODUCTION

The instrumentation amplifier is useful for amplifying small differential signals which may be riding on high common mode voltage levels. These amplifiers are particularly useful in amplifying signals in the milli-volt range which are supplied from a high impedance source (>2kΩ).

This brief will demonstrate how a low cost, high performance instrumentation amplifier can be built using the newly introduced LM3900 quad amplifier. It is also indicated how a compact transducer bridge amplifier system can be developed to take advantage of the versatility of the LM3900.

BASIC AMPLIFIER OPERATION

Figure 1 shows the basic operation of the amplifier. The bias of the LM3900 is set by the resistors R_2 and R_3 (neglecting for now, the transistors Q_1 and Q_2). Current which enters the non-inverting input of the LM3900 will be "mirrored" about V^- and then will be drawn into the inverting input terminal. This causes the current to flow through the feedback resistor, R_3, which establishes the output voltage level. If $R_2 = R_3$ and further, if R_2 is connected to ground (0V), then the output voltage biasing level will also be exactly zero volts. It should be noticed that an *OUTPUT OFFSET CONTROL* can be implemented by supplying a reference voltage, E_R, between R_2 and ground.

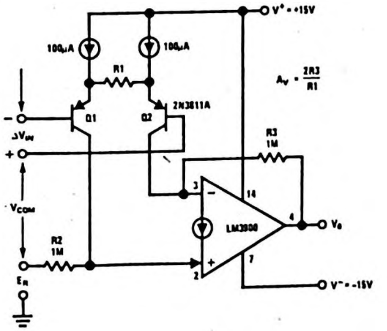


FIGURE 1. Basic Instrumentation Amplifier.

Adding transistors Q_1 and Q_2, as shown in Figure 1 will not disturb this biasing if the two collector currents of the transistors are well matched for a 0V differential input signal. The current sources which bias Q_1 and Q_2, are chosen to be 100μA each to guarantee high β and low offset voltage in Q_1 and Q_2.

The gain of the amplifier is calculated as follows: Any differential input voltage, ΔV_{IN}, appears across R_1, and produces a current change ΔI, which is given by:

$$\Delta I = \frac{\Delta V_{IN}}{R_1} \tag{1}$$

This current change will show up in the collectors of Q_1 and Q_2 with opposite polarity. The input mirror of the LM3900 returns ΔI_{Q1} to the inverting input terminal where it is added (with sign) to ΔI_{Q2} yielding a total current change of $2\Delta I$. This current flows through the feedback resistor, R_3, which causes an output voltage change, ΔVo, which is given by:

$$\Delta Vo = 2\Delta I \times R_3 = 2 \times \frac{\Delta V_{IN}}{R_1} \times R_3 \tag{2}$$

to yield a gain,

$$A_V = 2\,\frac{R_3}{R_1} \tag{3}$$

At this point it is convenient to evaluate the result obtained. The gain can be established by one resistor (R_1) according to equation (3). Conventional instrumentation amplifiers usually have a gain given by:

$$A_V = 1 + \frac{\text{Constant}}{R} \tag{4}$$

This means that the minimum gain of unity is obtained if R is left out ($R = \infty$). Note that this is different from the result indicated in equation (3) where unity gain is obtained for

$$R_1 = 2R_3 \tag{5}$$

and minimum gain (or maximum attenuation) is obtained if R_1 is left out ($R_1 = \infty$). This suggests that the amplifier can be turned OFF without disturbing the output voltage dc bias.

The two current sources for Q_1 and Q_2 are implemented with a dual transistor (Q_3 and Q_4) in conjunction with an additional amplifier of the LM3900 as shown in Figure 2. The operation can be easily understood if R_4 and R_5 are incorporated within the amplifier, which then takes the form of a conventional opamp closed loop regulator which maintains a reference voltage (the drop across R_6) at the emitter of Q_4.

PERFORMANCE

The performance of the complete instrumentation amplifier of Figure 2 is outlined below (Table 1 and Figure 3).

TABLE 1. Typical Performance Characteristics

GAIN	
Range of gain	34 dB ($R_1 = \infty$) to 72 dB ($R_1 = 0$)
Gain is set according to	$A_V = \frac{2R_3}{R_1}$
INPUT	
Voltage offset referred to input is adjustable to zero	
Common mode and differential input voltage	Pos. supply less 2.4V Neg. supply less 300 mV
Common mode rejection ratio at 10 Hz	115 dB (gain of 1000)
Bias current (either input)	200 nA
OUTPUT	
Output offset is adjustable to zero	
Output noise	12 mV$_{rms}$ (open loop) 3 mV$_{rms}$ (A_{CL} = 66 dB)
FREQUENCY RESPONSE	
Small signal frequency response (−3 dB)	1 MHz (gain of 1000) 3 MHz (gain of 1)

Since quantitative discussion of the sources of offset voltage is beyond the scope of this brief, only the procedure for nulling the amplifier will be included.

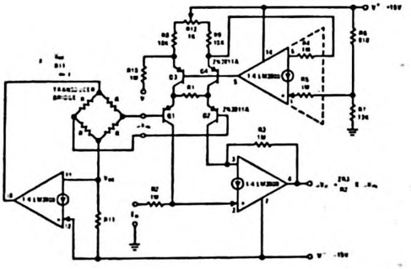


FIGURE 2. Bridge Amplifier

Letting R_1 go to zero causes the amplifier to operate in the open-loop mode. The main offset voltage source is now the V_{BE} mismatch of Q_1 and Q_2. The output can be nulled by the *OUTPUT OFFSET CONTROL* (the reference voltage for R_2) or by adjusting the value of R_2. With $R_1 = \infty$, the main offset voltage source is the mismatch in the collector currents of Q_3 and Q_4. This is easily adjusted via R_{12}. These first and second adjustments interact, however, after repeating the procedure a couple of times a good result is obtained.

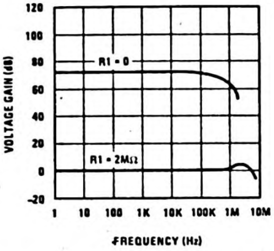


FIGURE 3. Frequency Response

TRANSDUCER BIAS SOURCE

Having in mind that the LM3900 consists of four independent amplifiers makes it relatively easy to bias a transducer bridge with a constant current source using only one more of the amplifiers and one resistor. The technique is self-explanatory and is also shown in Figure 2.

CONCLUSION

A brief review of a new concept for an instrumentation amplifier has been presented. Many applications can be derived from this basic connection which require amplifying the low level differential signals which are obtained from sensors such as strain gages, pressure transducers, and thermocouples. The performance of this instrumentation amplifier is adequate for many system applications. (See National Semiconductor Application Note 72, "The LM3900 – A New Current-Differencing Quad of ± Input Amplifiers" for further information.)

Wide Range Timer

National Semiconductor
Linear Brief
Robert C. Dobkin
February 1977

One of the problems encountered in potentiometer controlled circuits is dynamic range. With a linear pot, about a 100:1 range is the limit. Although the pot resolution may be better than 1%, the angular displacement for good control becomes too small. Usually, range switching is then used.

A logarithmic control is a possible solution. With log controls, the resolution is the same anywhere within the operating range. For example, if 40° rotation is equal to a change from 10% to 100% of full scale, then 40° rotation is also equal to a change from 0.01% to 0.1% of full scale. It is easy to control a function over a 1,000,000:1 range with good control anywhere within the range.

The exponential relationship between the emitter-base voltage of a transistor and its collector current is well known. This relationship holds true within a few percent over extremely wide ranges. Using a transistor pair, and an op amp, it is easy to make a current source controllable over a 6 decade range.

Figure 1 shows a timer which can be adjusted from 2 ms to 2000 seconds with a single control. An LM122 is

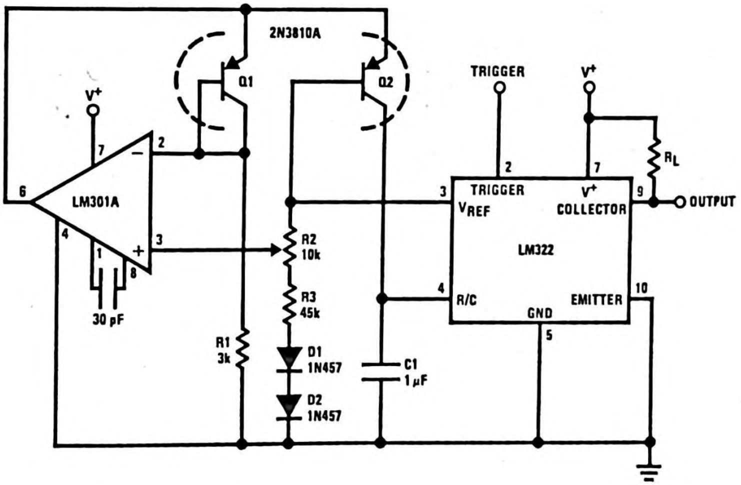

2N3810A
Q1
Q2
V+
LM301A
7
2
6
4
1
8
3
−
+
30 pF
R1
3k
R2
10k
R3
45k
D1
1N457
D2
1N457
C1
1 µF
TRIGGER
V+
RL
LM322
TRIGGER
VREF
V+
COLLECTOR
R/C
GND
EMITTER
2
7
3
9
4
10
5
OUTPUT

FIGURE 1. 2 ms to 2000 Second Timer

used for the timing function in conjunction with a current source that is logarithmically controlled from a pot. The operation is as follows:

Transistors Q1 and Q2 are a matched PNP pair. Resistor R1 and the op amp set up a constant current of 1 mA through Q1 using the internal 3V reference from the timer. With R2 at the most positive end of its range, the non-inverting input of the op amp is at V_{REF}. This forces the emitter-base voltage of Q2 to equal Q1 and since the transistors are matched, the collector current of Q2 is also 1 mA. A time-out period of 2 ms results.

Rotating R2 subtracts the voltage between the arm of the pot and V_{REF} from the emitter-base voltage of Q2—lowering its collector current. The current is decreased by a factor of 10 for every 60 mV developed. A total of 360 mV is dropped across the pot, allowing a reduction in Q2 collector current by a factor of 1,000,000 or from 1 mA to 1 nA. A 1 nA charging current gives a 2000 second time out. (At maximum time, there is about a 30% error due to the 0.3 nA input current of the comparator). Finally, diodes D1 and D2 temperature compensate the voltage across the pot.

Calibrating the circuit is relatively easy (except for obtaining a log dial for the pot). Resistor R1 is adjusted for the minimum operating time removing for mismatch in the transistors, capacitor tolerance, and the offset of the op amp. R3 is used to calibrate the full scale time by adjusting the drop across R2 to 360 mV.

This type of log control is not limited to timers. If used in oscillator or function generator circuits, an ultra wide range VCO can be made. Also, in power supply circuitry, it is possible for a regulator to have as much resolution when adjusted for 0.001V output as when the output is 10V. Finally, a log current generator makes an easily adjusted low value current source without high value resistors.

Circuit Techniques for Avoiding Oscillations in Comparator Applications

National Semiconductor
Linear Brief 39
Peter Lefferts
January 1978

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

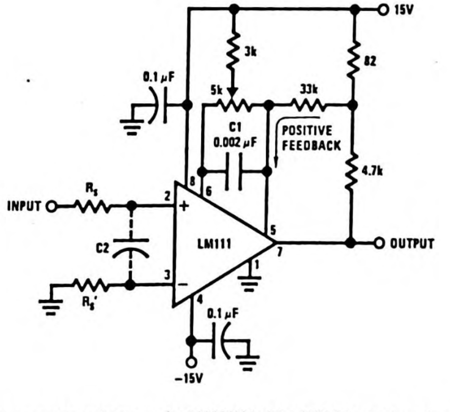
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trimpot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



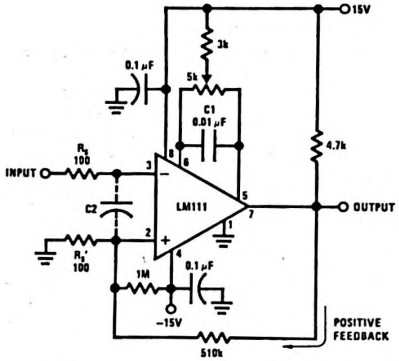
Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 1. Improved Positive Feedback

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2,* the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if the value of R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See paragraph 7, below, for the alternative.

7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and ensure sharp output transitions with input triangle waves from a few Hz to hundreds of kHz. The positive feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).


15V
3k
0.1 µF
5k
C1
0.01 µF
4.7k
R_s
100
INPUT
3
8
6
C2
LM111
5
7
1
2
4
R_s'
100
1M
0.1 µF
-15V
OUTPUT
POSITIVE
FEEDBACK
510k

Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

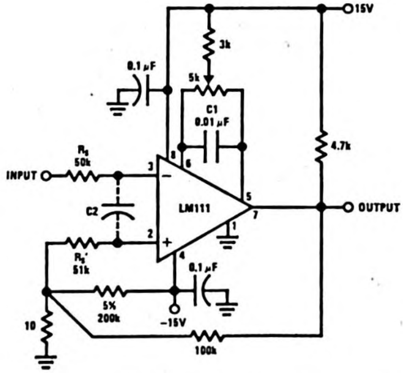

15V
3k
0.1 µF
5k
C1
0.01 µF
4.7k
R_s
50k
INPUT
3
8
6
C2
LM111
5
7
1
2
4
R_s'
51k
0.1 µF
5%
200k
10
-15V
100k
OUTPUT

FIGURE 3. Positive Feedback With High Source Resistance

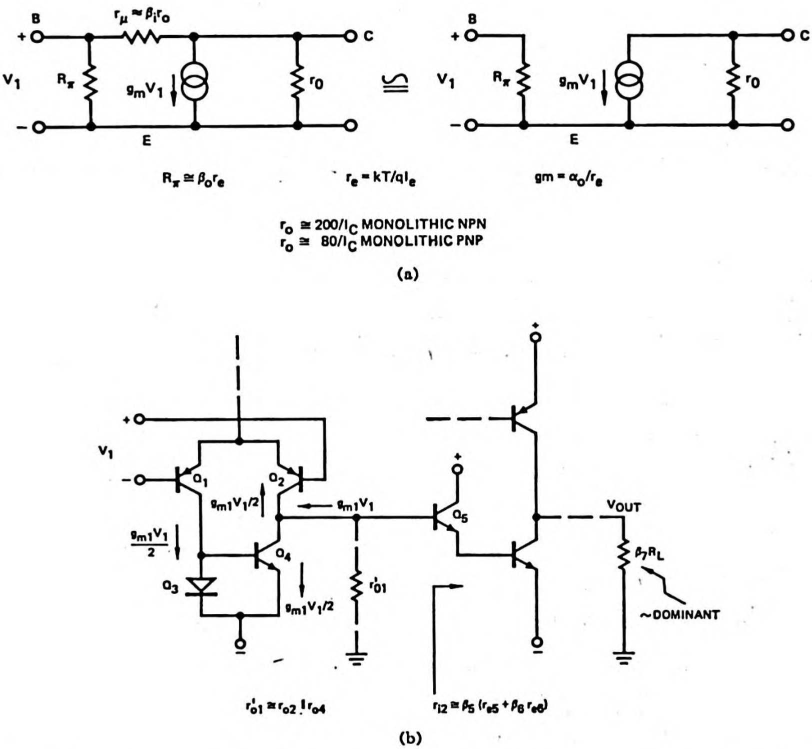

B
$r_\mu \approx \beta_i r_o$
+
C
V_1
R_π
$g_m V_1$
r_o
≅
−
E
$R_\pi \cong \beta_o r_e$
$r_e = kT/qI_e$
$gm = \alpha_o / r_e$
$r_o \cong 200/I_C$ MONOLITHIC NPN
$r_o \cong 80/I_C$ MONOLITHIC PNP
(a)
V_1
Q_1
Q_2
Q_3
Q_4
Q_5
$g_{m1}V_1/2$
$\frac{g_{m1}V_1}{2}$
$g_{m1}V_1$
r'_{01}
V_{OUT}
$\beta_7 R_L$
~DOMINANT
$r'_{01} \cong r_{o2} \| r_{o4}$
$r_{i2} \cong \beta_5 (r_{e5} + \beta_6 r_{e6})$
(b)

Fig. 3. (a) Approximate π model for CE transistor at dc. Feedback element $r_\mu \cong \beta_i r_o$ is ignored since this greatly simplifies hand calculations. The error caused is usually less than 10 percent because β_i, the intrinsic β under the emitter, is quite large. Base resistance r_x is also ignored for simplicity. (b) Circuit illustrating calculation of electronic gain for op amp of Fig. 1. Consideration is given only to the fully loaded condition ($R_L \cong 2$ kΩ) where β_7 is falling (to about 50) due to high current density. Under this condition, the output resistance of $Q6$ and $Q9$ are nondominant.

trical characteristics. A highly simplified thermal analysis is made, resulting in a gain equation containing only the maximum output current of the op amp and a thermal feedback constant.

The next three sections apply first-order models to the calculation of small-signal high frequency and large-signal slewing characteristics. Results obtained include an accurate equation for gain-bandwidth product, a general expression for slew rate, some important relationships between slew rate and bandwidth, and a solution for voltage follower behavior in a slewing mode. Due to the simplicity of the results in these sections, they are very useful to designers in the development of new amplifier circuits.

Section VI applies more accurate models to the calculation of important second-order effects. An effort is made in this section to isolate all of the major contributors to bandlimiting in the modern amp.

In the final section, some techniques for reduction of op amp die size are considered. Transconductance reduction and layout techniques are discussed which lead to fabrication of an extremely compact op amp cell. An example yielding 8000 possible op amps per 3-in wafer is given.

II. GAIN AT DC AND LOW FREQUENCIES

A. The Electronic Gain

The electronic voltage gain will first be calculated at dc using the circuit of Fig. 1. This calculation becomes straightforward if we employ the simplified transistor model shown in Fig. 3(a). The resulting gain from Fig. 3(b) is

$$A_V(0) = \frac{v_{\text{out}}}{v_{\text{in}}} \cong \frac{g_{m1}\beta_5\beta_6\beta_7 R_L}{1 + r_{i2}/r_{01}}, \tag{1}$$

where

$$r_{i2} \cong \beta_5(r_{e5} + \beta_6 r_{e6})$$

$$r_{01}' \cong r_{04}//r_{02}.$$

It has been assumed that

$$\beta_7 R_L < r_{06}//r_{09},\ g_{m1} = g_{m2},\ \beta_7 = \beta_8.$$

The numerical subscripts relate parameters to transistor Q numbers (i.e., r_{e5} is r_e of Q_5, β_6 is β_0 of Q_6, etc.). It has also been assumed that the current mirror transistors Q_3 and Q_4 have α's of unity, and the usually small loading of R_B has been ignored. Despite the several assumptions made in obtaining this simple form for (1), its accuracy is quite adequate for our needs.

An examination of (1) confirms the way in which the amplifier operates: the input pair and current mirror convert the input voltage to a current $g_{m1}v_{in}$ which drives the base of the second stage. Transistors Q_5, Q_6, and Q_7 simply multiply this current by β^3 and supply it to the load R_L. The finite output resistance of the first stage causes some loss when compared with second stage input resistance, as indicated by the term $1/(1 + r_{i2}/r_{01}')$. A numerical example will help our perspective: for the LM101A, $I_1 \cong 10\ \mu\text{A}$, $I_2 \cong 300\ \mu\text{A}$, $\beta_5 = \beta_6 \cong 150$, and $\beta_7 \cong 50$. From (1) and dc voltage gain with $R_L = 2\ \text{k}\Omega$ is

$$A_V(0) \cong 625\,000. \tag{2}$$

The number predicted by (2) agrees well with that measured on a discrete breadboard of the LM101A, but is much higher than that observed on the integrated circuit. The reason for this is explained in the next section.

B. Thermal Feedback Effects on Gain

The typical IC op amp is capable of delivering powers of 50–100 mW to a load. In the process of delivering this power, the output stage of the amp internally dissipates similar power levels, which causes the temperature of the IC chip to rise in proportion to the output dissipated power. The silicon chip and the package to which it is bonded are good thermal conductors, so the whole chip tends to rise to the same temperature as the output stage. Despite this, small temperature gradients from a few tenths to a few degrees centigrade develop across the chip with the output section being hotter than the rest. As illustrated in Fig. 4, these temperature gradients appear across the input components of the op amp and induce an input voltage which is proportional to the output dissipated power.

To a first order, it can be assumed that the temperature difference (T_2-T_1) across a pair of matched and closely spaced components is given simply by

$$(T_2 - T_1) \cong \pm K_T P_d \quad {}^\circ\text{C} \tag{3}$$

where

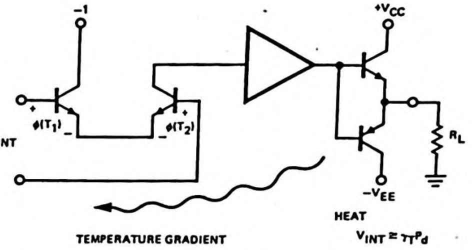


Fig. 4. Simple model illustrating thermal feedback in an IC op amp having a single dominant source of self-heat, the output stage. The constant $\gamma_T \cong 0.6$ mV/W and P_d is power dissipated in the output. For simplicity, we ignore input drift due to uniform heating of the package. This effect can be significant if the input stage drift is not low, see [7].

P_d power dissipated in the output circuit,

K_T a constant with dimensions of °C/W.

The plus/minus sign is needed because the direction of the thermal gradient is unknown. In fact, the sign may reverse polarity during the output swing as the dominant source of heat shifts from one transistor to another. If the dominant input components consist of the differential transistor pair of Fig. 4, the thermally induced input voltage V_{int} can be calculated as

$$\begin{aligned} V_{int} &\cong \pm K_T P_d (2 \times 10^{-3}) \\ &\cong \pm \gamma_T P_d \end{aligned} \tag{4}$$

where $\gamma_T = K_T(2 \times 10^{-3})$ V/W, since the transistor emitter-base drops change about −2 mV/°C.

For a thermally well designed IC op amp, in which the power output devices are made to approximate either a point or a line source and the input components are placed on the resulting isothermal lines (see below and Fig. 8), typical values measured for K_T are

$$K_T \approx 0.3\ {}^\circ\text{C/W} \tag{5}$$

in a TO-5 package.

The dissipated power in the class-AB output stage P_d is written by inspection of Fig. 4:

$$P_d = \frac{V_o V_s - V_o^2}{R_L} \tag{6}$$

where

$$V_s = +V_{cc} \quad \text{when } V_o > 0$$

$$V_s = -V_{ee} \quad \text{when } V_o < 0.$$

A plot of (6) in Fig. 5 resembles the well-known class-AB dissipation characteristics, with zero dissipation occurring for $V_o = 0, +V_{cc}, -V_{cc}$. Dissipation peaks occur for $V_o = +V_{cc}/2$ and $-V_{cc}/2$. Note also from (4) that the thermally induced input voltage V_{int} has this same double-humped shape since it is just equal to a constant times P_d at dc.

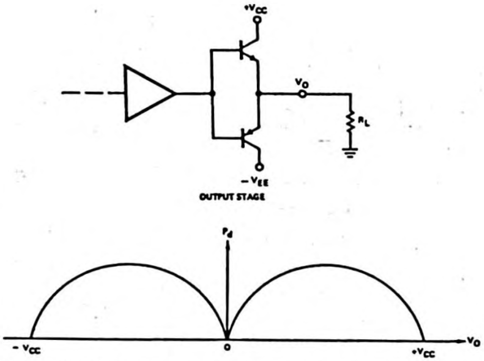


Fig. 5. Simple class-B output stage and plot of power dissipated in the stage, P_d, assuming device can swing to the power supplies. Equation (6) gives an expression for the plot.

Now examine Figs. 6(a) and (b) which are curves of open-loop V_o versus V_{in} for the IC op amp. Note first that the overall curve can be visualized to be made up of two components: a) a normal straight line electrical gain curve of the sort expected from (1) and b) a double-humped curve similar to that of Fig. 5. Further, note that the gain characteristic has either positive or negative slope depending on the value of output voltage. This means that the thermal feedback causes the open-loop gain of the feedback amplifier to change phase by 180°, apparently causing negative feedback to become positive feedback. If this is really true, the question arises: which input should be used as the inverting one for feedback? Further, is there any way to close the amplifier and be sure it will not find an unstable operating point and latch to one of the power supplies?

The answers to these questions can be found by studying a simple model of the op amp under closed-loop conditions, including the effects of thermal coupling. As shown in Fig. 7, the thermal coupling can be visualized as just an additional feedback path which acts in parallel with the normal electrical feedback. Noting that the electrical form of the thermal feedback factor is [see (4) and (6)]

$$\beta_T = \frac{\partial V_{int}}{\partial V_o} = \pm \frac{\gamma_T}{R_L} (V_s - 2V_o). \qquad (7)$$

The closed-loop gain, including thermal feedback is

$$A_V(0) = \frac{\mu}{1 + \mu(\beta_e \pm \beta_T)} \qquad (8)$$

where μ is the open-loop gain in the absence of thermal feedback [(1)] and β_e is the applied electrical feedback as in Fig. 7. Inspection of (8) confirms that as long as there is sufficient electrical feedback to swamp the thermal feedback (i.e., $\beta_e > \beta_T$), the amplifier will behave as a normal closed-loop device with characteristics determined principally by the electrical feedback (i.e., $A_V(0) \cong 1/\beta_e$). On the other hand, if β_e is small or nonexistant, the thermal term in (8) may dominate, giving an apparent open-loop gain characteristic determined by the thermal feedback factor β_T. Letting $\beta_e = 0$ and combining (7) and (8), $A_V(0)$ becomes

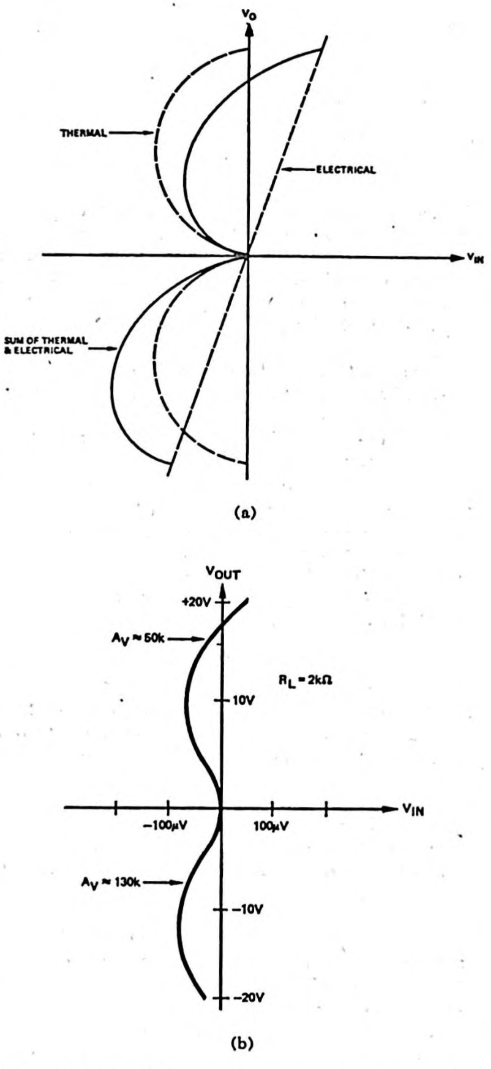


Fig. 6. (a) Idealized dc transfer curve for an IC op amp showing its electrical and thermal components. (b) Experimental open-loop transfer curve for a representative op amp (LM 101).

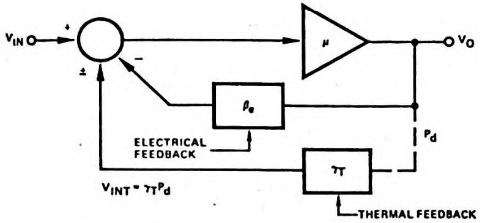


Fig. 7. Diagram used to calculate closed-loop gain with thermal feedback.

$$A_V(0) = \frac{\mu}{1 \pm \frac{\mu\gamma_T}{R_L}(V_S - 2V_o)}. \quad (9)$$

Recalling from (6) that V_0 ranges between 0 and V_S, we note that the incremental thermal feedback is greatest when $V_0 = 0$ or V_s, and it is at these points that the thermally limited gain is smallest. To use the amplifier in a predictable manner, one must always apply enough electrical feedback to reduce the gain below this minimum thermal gain. Thus, a *maximum usable gain* can be defined as that approximately equal to the value of (9) with $V_0 = 0$ or V_s which is

$$A_V(0)|_{max} \cong \frac{R_L}{\gamma_T V_S} \quad (10)$$

or

$$A_V(0)|_{max} \cong \frac{1}{\gamma_T I_{max}}. \quad (11)$$

It was assumed in (10) and (11) that thermal feedback dominates over the open-loop electrical gain, μ. Finally, in (11) a maximum current was defined $I_{max} = V_S/R_L$ as the maximum current which would flow if the amplifier output could swing all the way to the supplies.

Equation (11) is a strikingly simple and quite general result which can be used to predict the expected maximum usable gain for an amplifier if we know only the maximum output current and the thermal feedback constant γ_T.

Recall that typically $K_T \cong 0.3$°C/W and $\gamma_T = (2 \times 10^{-3})\ K_T \cong 0.6$ mV/W. Consider, as as example, the standard IC op amp operating with power supplies of $V_s = \pm 15$ V and a minimum load of 2 kΩ, which gives $I_{max} = 15$ V/2 kΩ = 7.5 mA. Then, from (11), the maximum thermally limited gain is about:

$$A_V(0)|_{max} \cong 1/(0.6 \times 10^{-3})(7.5 \times 10^{-3})$$

$$\cong 220\,000. \quad (12)$$

Comparing (2) and (12), it is apparent that the thermal characteristics dominate over the electrical ones if the minimum load resistor is used. For loads of 6 kΩ or more, the electrical characteristics should begin to dominate if thermal feedback from sources other than the output stage is negligible. It should be noted also that, in some high speed, high drain op amps, thermal feedback from the second stage dominates when there is no load.

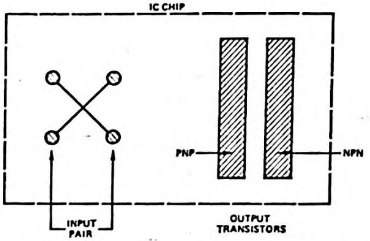


Fig. 8. One type layout in which a quad of input transistors is cross connected to reduce effect of nonuniform thermal gradients. The output transistors use distributed stripe geometries to generate predictable isothermal lines.

As a second example, consider the so-called "power op amp" or high gain audio amp which suffers from the same thermal limitations just discussed. For a device which can deliver 1 W into a 16-Ω load, the peak output current and voltage are 350 mA and 5.7 V. Typically, a supply voltage of about 16 V is needed to allow for the swing loss in the IC output stage. I_{max} is then 8 V/16 Ω or 0.5 A. If the device is in a TO-5 package γ_T is approximately 0.6 mV/W, so from (11) the maximum usable dc gain is

$$A_V(0)|_{max} \cong \frac{1}{(0.6 \times 10^{-3})(0.5)} \cong 3300. \quad (13)$$

This is quite low compared with electrical gains of, say, 100 000 which are easily obtainable. The situation can be improved considerably by using a large die to separate the power devices from the inputs and carefully placing the inputs on constant temperature (isothermal) lines as illustrated in Fig. 8. If one also uses a power package with a heavy copper base, γ_T's as low as 50 μV/W have been observed. For example, a well-designed 5-W amplifier driving an 8-Ω load and using a 24-V supply, would have a maximum gain of 13 000 in such a power package.

As a final comment, it should be pointed out that the most commonly observed effect of thermal feedback in high gain circuits is low frequency distortion due to the nonlinear transfer characteristic. Differential thermal coupling typically falls off at an initial rate of 6 dB/octave starting around 100–200 Hz, so higher frequencies are uneffected.

III. SMALL-SIGNAL FREQUENCY RESPONSE

At higher frequencies where thermal effects can be ignored, the behavior of the op amp is dependent on purely electronic phenomena. Most of the important small and large signal performance characteristics of the classical IC op amp can be accurately predicted from

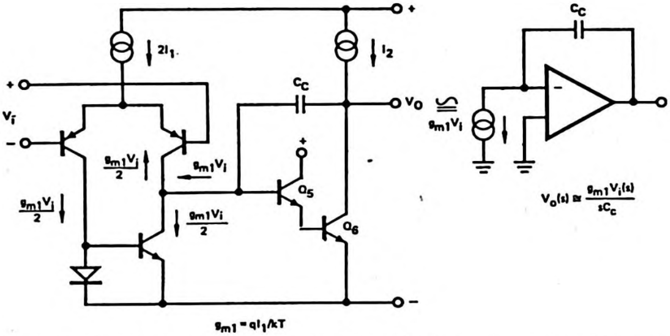


Fig. 9. First-order model of op amp used to calculate small signal high frequency gain. At frequencies of interest the input impedance of the second stage becomes low compared to first stage output impedance due to C_c feedback. Because of this, first stage output impedance can be assumed infinite, with no loss in accuracy.

very simple first-order models for the amplifier in Fig. 1[8]. The small-signal model that is used assumes that the input differential amplifier and current mirror can be replaced by a frequency independent voltage controlled current source, see Fig. 9. The second stage consisting essentially of transistors Q_5 and Q_6, and the current source load, is modeled as an ideal frequency independent amplifier block with a feedback or "integrating capacitor" identical to the compensation capacitor, C_c. The output stage is assumed to have unity voltage gain and is ignored in our calculations. From Fig. 9, the high frequency gain is calculated by inspection:

$$A_v(\omega) = \left|\frac{v_o}{v_i}(s)\right| = \left|\frac{g_{m1}}{sC_c}\right| = \frac{g_{m1}}{\omega C_c} \tag{14}$$

where dc and low frequency behavior have not been included since this was evaluated in the last section. Fig. 10 is a plot of the gain magnitude as predicted by (14). From this figure it is a simple matter to calculate the open-loop unity gain frequency ω_u, which is also the gain-bandwidth product for the op amp under closed-loop conditions:

$$\omega_u = \frac{g_{m1}}{C_c}. \tag{15}$$

In a practical amplifier, ω_u is set to a low enough frequency (by choosing a large C_c) so that negligible excess phase over the 90° due to C_c has built up. There are numerous contributors to excess phase including low f_t p-n-p's, stray capacitances, nondominant second stage poles, etc. These are discussed in more detail in a later section, but for now suffice it to say that, in the simple IC op amp, $\omega_u/2\pi$ is limited to about 1 MHz. As a simple test of (15), the LM101 or the μA741 has a first stage bias current I_1 of 10 μA per side, and a compensation capacitor for unity gain operation, C_c, of 30 pF. These amplifiers each have a first stage g_m which is half that of the simple differential amplifier in Fig. 1 so $g_{m1} = qI_1/2kT$. Equation (15) then predicts a unity gain corner of

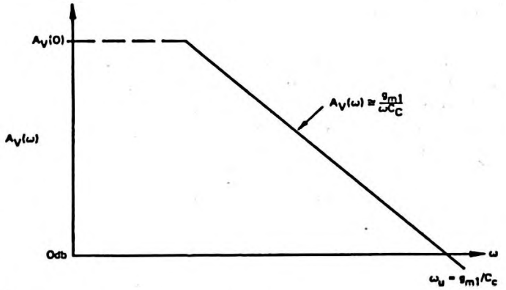


Fig. 10. Plot of open-loop gain calculated from model in Fig. 9. The dc and LF gain are given by (1), or (11) if thermal feedback dominates.

$$f_u = \frac{\omega_u}{2\pi} = \frac{g_{m1}}{2\pi C_c} = \frac{(0.192 \times 10^{-3})}{2\pi(30 \times 10^{-12})} = 1.02 \text{ MHz} \tag{16}$$

which agrees closely with the measured values.

IV. Slew Rate and Some Special Limits

A. A General Limit on Slew Rate

If an op amp is overdriven by a large-signal pulse or square wave having a fast enough rise time, the output does not follow the input immediately. Instead, it ramps or "slews" at some limiting rate determined by internal currents and capacitances, as illustrated in Fig. 11. The magnitude of input voltage required to make the amplifier reach its maximum slew rate varies, depending on the type of input stage used. For an op amp with a

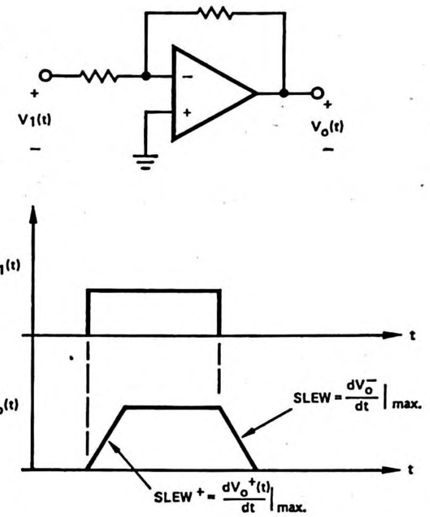

+
$V_1(t)$
−
+
$V_o(t)$
−
$V_1(t)$
t
$V_o(t)$
t
$SLEW^- = \frac{dV_o^-}{dt}\Big|_{max.}$
$SLEW^+ = \frac{dV_o^+(t)}{dt}\Big|_{max.}$

Fig. 11. Large signal "slewing" response observed if the input is overdriven.

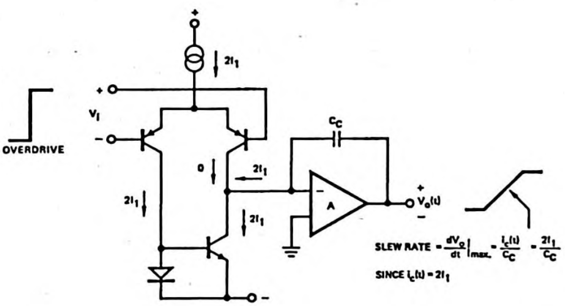

+
$2I_1$
OVERDRIVE
+
V_I
−
0
$2I_1$
$2I_1$
$2I_1$
C_C
A
+
$V_o(t)$
−
−
$SLEW\ RATE = \frac{dV_o}{dt}\Big|_{max.} = \frac{I_c(t)}{C_C} = \frac{2I_1}{C_C}$
$SINCE\ I_c(t) = 2I_1$

Fig. 12. Model used to calculate slew rate for the amp of Fig. 1 in the inverting mode. For simplicity, all transistor α's are assumed equal to unity, although results are essentially independent of α. An identical slew rate can be calculated for a negative-going output, obtained if the applied input polarity is reversed.

simple input differential amp, an input of about 60 mV will cause the output to slew at 90 percent of its maximum rate, while a μA741, which has half the input g_m, requires 120 mV. High speed amplifiers such as the LM 118 or a FET-input circuit require much greater overdrive, with 1–3 V being common. The reasons for these overdrive requirements will become clear below.

An adequate model to calculate slew limits for the representative op amp in the inverting mode is shown in Fig. 12, where the only important assumption made is that $I_2 \geq 2I_1$ in Fig. 1. This condition always holds in a well-designed op amp. (If one lets I_2 be less than $2I_1$, the slew is limited by I_2 rather than I_1, which results in lower speed than is otherwise possible.) Fig. 12 requires some modification for noninverting operation, and we will study this later.

The limiting slew rate is now calculated from Fig. 12. Letting the input voltage be large enough to fully switch the input differential amp, we see that all of the first stage tail current $2I_1$ is simply diverted into the integrator consisting of A and C_c. The resulting slew rate is then:

$$\text{slew rate} = \frac{dv_o}{dt}\bigg|_{\max} = \frac{i_c(t)}{C_c}. \tag{17}$$

Noting that $i_c(t)$ is a constant $2I_1$, this becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2I_1}{C_c}. \qquad (18)$$

As a check of this result, recall that the μA741 has $I_1 = 10\ \mu$A and $C_1 = 30$ pF, so we calculate:

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2 \times 10^{-5}}{30 \times 10^{-12}} = 0.67\ \frac{\text{V}}{\mu\text{s}} \qquad (19)$$

which agrees with measured values.

The large and small signal behavior of the op amp can be usefully related by combining (15) for ω_u with (18). The slew rate becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2\omega_u I_1}{g_{m1}}. \qquad (20)$$

Equation (20) is a general and very useful relationship. It shows that, for a given unity-gain frequency, ω_u, the slew rate is determined entirely by just the ratio of first stage operating current to first stage transconductance, I_1/g_{m1}. Recall that ω_u is set at the point where excess phase begins to build up, and this point is determined largely by technology rather than circuit limitations. Thus, the only effective means available to the circuit designer for increasing op amp slew rate is to *decrease* the ratio of first stage transconductance to operating current, g_{m1}/I_1.

B. Slew Limiting for Simple Bipolar Input Stage

The significance of (20) is best seen by considering the specific case of a simple differential bipolar input as in Fig. 1. For this circuit, the first stage transconductance (for $\alpha_1 = 1$) is[1]

$$g_{m1} = qI_1/kT \qquad (21)$$

so that

$$\frac{g_{m1}}{I_1} = q/kT. \qquad (22)$$

Using this in (20), the maximum bipolar slew rate is

$$\left.\frac{dv_0}{dt}\right|_{\max} = 2\omega_u \frac{kT}{q}. \qquad (23)$$

This provides us with the general (and somewhat dismal) conclusion that slew rate in an op amp with a simple bipolar input stage is dependent only upon the unity gain corner and fundamental constants. Slew rate can be increased only by increasing the unity gain corner, which we have noted is generally difficult to do. As a demonstration of the severity of this limit, imagine an op amp using highly advanced technology and clever design, which might have a stable unity gain frequency of 100 MHz. Equation (23) predicts that the slew rate for this advanced device is only

$$\left.\frac{dv_0}{dt}\right|_{\max} = 33\ \frac{\text{V}}{\mu\text{s}} \qquad (24)$$

which is good, but hardly impressive when compared with the difficulty of building a 100-MHz op amp.[2] But, there are some ways to get around this limit as we shall see shortly.

C. Power Bandwidth

Our intuition regarding slew rate will be enhanced somewhat if we relate it to a term called "power bandwidth." Power bandwidth is defined as the maximum frequency at which full output swing (usually 10 V peak) can be obtained without distortion. For a sinusoidal output voltage $v_0(t) = V_p \sin \omega t$, the rate of change of output, or slew rate, required to reproduce the output is

$$\frac{dv_0}{dt} = \omega V_p \cos \omega t. \qquad (25)$$

This has a maximum when $\cos \omega t = 1$ giving

$$\left.\frac{dv_0}{dt}\right|_{\max} = \omega V_p, \qquad (26)$$

so the highest frequency that can be reproduced without slew limiting, $\omega_{\max}$ (power bandwidth) is

$$\omega_{\max} = \frac{1}{V_p} \left.\frac{dv_0}{dt}\right|_{\max}. \qquad (27)$$

Thus, power bandwidth and slew rate are directly related by the inverse of the peak of the sine wave V_p. Fig. 13 shows the severe distortion of the output sine wave which results if one attempts to amplify a sine wave of frequency $\omega > \omega_{\max}$.

Some numbers illustrate typical op amp limits. For a μA741 or LM101 having a maximum slew rate of 0.67 V/μs, (27) gives a maximum frequency for an undistorted 10-V peak output of

$$f_{\max} = \frac{\omega_{\max}}{2\pi} = 10.7\ \text{kHz}, \qquad (28)$$

which is a quite modest frequency considering the much higher frequency small signal capabilities of these devices. Even the highly advanced 100-MHz amplifier considered above has a 10-V power bandwidth of only 0.5 MHz, so it is apparent that a need exists for finding ways to improve slew rate.

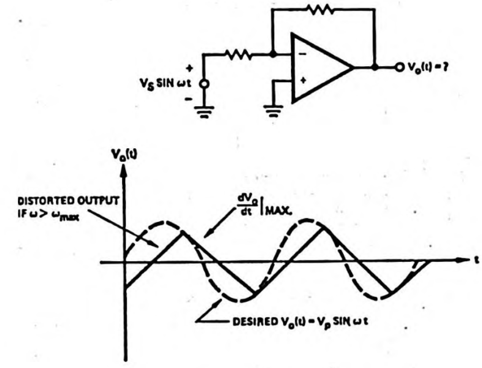
D. Techniques for Increasing Slew Rate

1) Resistive Enhancement of the Bipolar Stage: Equation (20) indicates that slew rate can be improved if we reduce first stage g_{m1}/I_1. One of the most effective ways

---

[1] Note that (21) applies only to the simple differential input stage of Fig. 12. For compound input stages as in the LM101 or μA741, g_{m1} is half that in (21), and the slew rate in (23) is doubled.

[2] We assume in all of these calculations that C_c is made large enough so that the amplifier has less than 180° phase lag at ω_u, thus making the amplifier stable for unity closed-loop gain. For higher gains one can of course reduce C_c (if the IC allows external compensation) and increase the slew rate according to (18).



V_S SIN ωt
+
−
$V_o(t) = ?$
$V_o(t)$
DISTORTED OUTPUT IF ω > ω_max
$\frac{dV_o}{dt}\Big|$ MAX
t
DESIRED $V_o(t) = V_p$ SIN ωt

Fig. 13. Slew limiting effects on output sinewave that occur if frequency is greater than power bandwidth, ω_{max}. The onset of slew limiting occurs very suddenly as ω reaches ω_{max}. No distortion occurs below ω_{max}, while almost complete triangularization occurs at frequencies just slightly above ω_{max}.

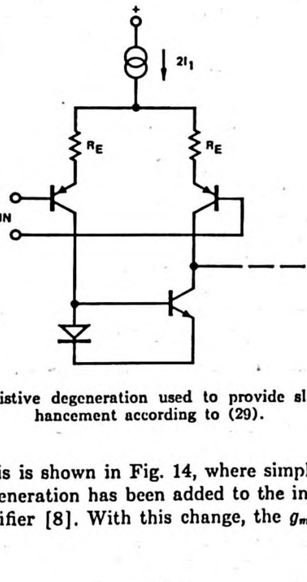


Fig. 14. Resistive degeneration used to provide slew rate enhancement according to (29).

of doing this is shown in Fig. 14, where simple resistive emitter degeneration has been added to the input differential amplifier [8]. With this change, the g_{m1}/I_1 drops to

$$\frac{g_{m1}}{I_1} = \frac{38.5}{1 + R_E I_1/26\ \text{mV}} \qquad (29)$$

at 25°C.

The quantity g_{m1}/I_1 is seen to decrease rapidly with added R_E as soon as the voltage drop across R_E exceeds 26 mV. The LM118 is a good example of a bipolar amplifier which uses emitter degeneration to enhance slew rate [4]. This device uses emitter resistors to produce $R_E I_1 = 500$ mV, and has a unity gain corner of 16 MHz. Equations (20) and (29) then predict a maximum inverting slew rate of

$$\frac{dv_o}{dt}\Big|_{max} = 2\omega_u \frac{I_1}{g_{m1}} = \omega_u = 100\,\frac{\text{V}}{\mu\text{s}} \qquad (30)$$

which is a twenty-fold improvement over a similar amplifier without emitter resistors.

A penalty is paid in using resistive slew enhancement, however. The two added emitter resistors must match extremely well or they add voltage offset and drift to the input. In the LM118, for example, the added emitter R's have values of 2.0 kΩ each and these contribute an input offset of 1 mV for each 4 Ω (0.2 percent) of mismatch. The thermal noise of the resistors also unavoidably degrades noise performance.

2) Slew Rate in the FET Input Op Amp: The FET (JFET or MOSFET) has a considerably lower transconductance than a bipolar device operating at the same current. While this is normally considered a drawback of the FET, we note that this "poor" behavior is in fact highly desirable in applications to fast amplifiers. To illustrate, the drain current for a JFET in the "current saturation" region can be approximated by

$$I_D \cong I_{DSS}(V_{GS}/V_T - 1)^2 \qquad (31)$$

where

I_{DSS} the drain current for $V_{GS} = 0$,
V_{GS} the gate source voltage having positive polarity for forward gate-diode bias,
V_T the threshold voltage having negative polarity for JFET's.

The small-signal transconductance is obtained from (31) as $g_m = \partial I_D/\partial V_G$. Dividing by I_D and simplifying, the ratio g_m/I_D for a JFET is

$$\frac{g_m}{I_D} \cong \frac{2}{(V_{GS} - V_T)} = \frac{2}{-V_T}\left[\frac{I_{DSS}}{I_D}\right]^{1/2}. \qquad (32)$$

Maximum amplifier slew rate occurs for minimum g_m/I_D and, from (32), this occurs when I_D (or V_{GS}) is maximum. Normally it is impractical to forward bias the gate junction so a practical minimum occurs for (32) when $V_{GS} \cong 0$ V and $I_D \cong I_{DSS}$. Then

$$\frac{g_m}{I_D}\Big|_{min} \cong -\frac{2}{V_T}. \qquad (33)$$

Comparing (33) with the analogous bipolar expression, (22), we find from (20) that the JFET slew rate is greater than bipolar by the factor

$$\frac{\text{JFET slew}}{\text{bipolar slew}} \approx \frac{-V_T}{2kT/q}\frac{\omega_{uf}}{\omega_{ub}} \qquad (34)$$

where ω_{uf} and ω_{ub} are unity-gain bandwidths for JFET and bipolar amps, respectively. Typical JFET thresholds are around 2 V ($V_T = -2$ V), so for equal bandwidths (34) tells us that a JFET-input op amp is about forty times faster than a simple bipolar input. Further, if

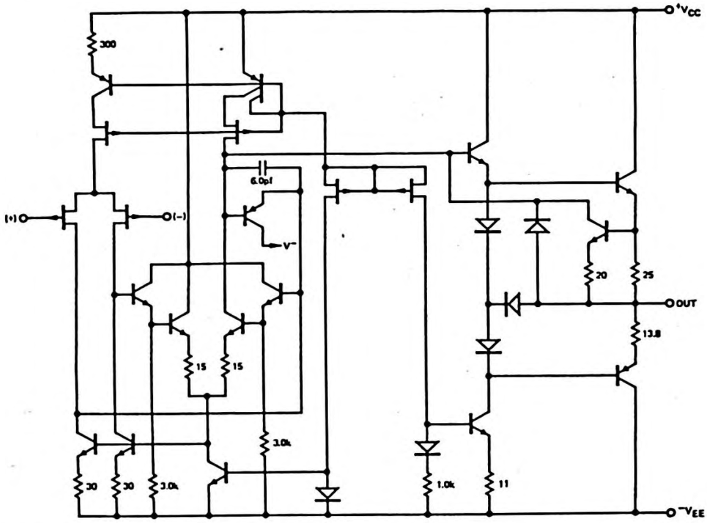


Fig. 15. Monolithic operational amplifier employing compatible p-channel JFET's on the same chip with normal bipolar components.

JFET's are properly substituted for the slow p-n-p's in a monolithic design, bandwidth improvements by at least a factor of ten are obtainable. JFET-input op amps, therefore, offer slew rate improvements by better than two orders of magnitude when compared with the conventional IC op amp. (Similar improvements are possible with MOSFET-input amplifiers.) This characteristic, coupled with picoamp input currents and reasonable offset and drift, make the JFET-input op amp a very desirable alternative to conventional bipolar designs.

As an example, Fig. 15, illustrates one design for an op amp employing compatible p-channel JFET's on the same chip with the normal bipolar components. This circuit exhibits a unity gain corner of 10 MHz, a 33 V/μs slew rate, an input current of 10 pA and an offset voltage and drift of 3 mV and 3 μV/°C [6]. Bandwidth and slew rate are thus improved over simple IC bipolar by factors of 10 and 100, respectively. At the same time input currents are smaller by about 10^3, and offset voltages and drifts are comparable to or better than slew enhanced bipolar circuits.

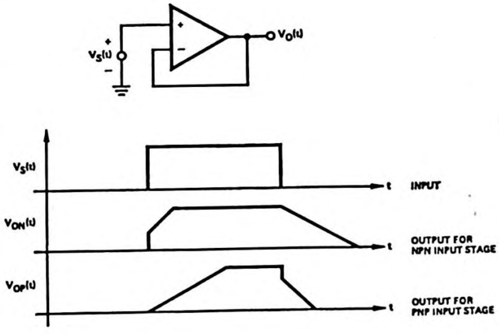


Fig. 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{on}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

V. SECOND-ORDER EFFECTS: VOLTAGE FOLLOWER SLEW BEHAVIOR

If the op amp is operated in the noninverting mode and driven by a large fast rising input, the output exhibits the characteristic waveform in Fig. 16. As shown, this waveform does not have the simple symmetrical slew characteristic of the inverter. In one direction, the output has a fast step (slew "enhancement") followed by a "normal" inverter slewing response. In the other direction, it suffers a slew "degradation" or reduced slope when compared with the inverter slewing response.

We will first study slew degradation in the voltage follower connection, since this represents a worst case slewing condition for the op amp. A model which adequately represents the follower under large-signal conditions can be obtained from that in Fig. 12 by simply

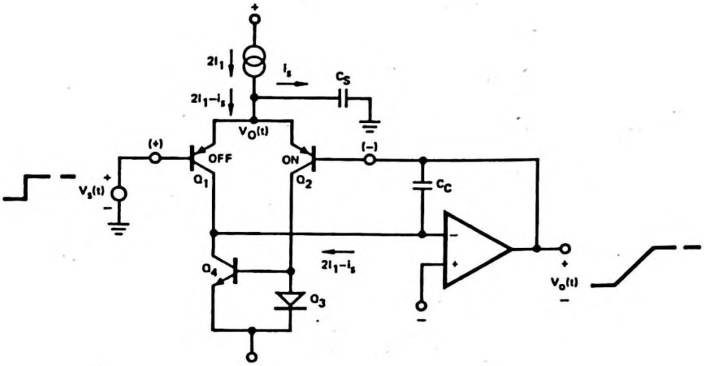


Fig. 17. Circuit used for calculation of slew "degradation" in the voltage follower. The degradation is caused by the capacitor C_s, which robs current from the tail, $2I_1$, thereby preventing the full $2I_1$ from slewing C_c.

tying the output to the inverting input, and including a capacitor C_s to account for the presence of any capacitance at the output of the first stage (tail) current source, see Fig. 17. This "input tail" capacitance is important in the voltage follower because the input stage undergoes rapid large-signal excursions in this connection, and the charging currents in C_s can be quite large.

Circuit behavior can be understood by analyzing Fig. 17 as follows. The large-signal input step causes Q_1 to turn OFF, leaving Q_2 to operate as an emitter follower with its emitter tracking the variational output voltage, $v_O(t)$. It is seen that $v_O(t)$ is essentially the voltage appearing across both C_s and C_c so we can write

$$\frac{dv_O}{dt} \cong \frac{i_c}{C_c} \cong \frac{i_s}{C_s}. \qquad (35)$$

Noting that $i_c \cong 2I_1 - i_s$ (unity α's assumed), (35) can be solved for i_s:

$$i_s \cong \frac{2I_1}{1 + C_c/C_s} \qquad (36)$$

which is seen to be constant with time. The degraded voltage follower slew rate is then obtained by substituting (36) into (35):

$$\left.\frac{dv_O}{dt}\right|_{\text{degr}} \cong \frac{i_s}{C_s} \cong \frac{2I_1}{C_c + C_s}. \qquad (37)$$

Comparing (37) with the slew rate for the inverter, (18), it is seen that the slew rate is reduced by the simple factor $1/(1 + C_s/C_c)$. As long as the input tail capacitance C_s is small compared with the compensation capacitor C_c, little degradation occurs. In high speed amplifiers where C_c is small, degradation becomes quite noticeable, and one is encouraged to develop circuits with small C_s.

As an example, consider the relatively fast LM118 which has $C_c \cong 5$ pF, $C_s \cong 2$ pF, $2I_1 = 500\ \mu$A. The calculated inverter slew rate is $2I_1/C_c \cong 100$ V/μs, and the degraded voltage follower slew rate is found to be $2I_1/(C_c + C_s) \cong 70$ V/μs. The slew degradation is seen to be about 30 percent, which is very significant. By contrast, a μA741 has $C_c \cong 30$ pF and $C_s \cong 4$ pF which results in a degradation of less than 12 percent.

The slew "enhanced" waveform can be similarly predicted from a simplified model. By reversing the polarity of the input and initially assuming a finite slope on the input step, the enhanced follower is analyzed, as shown in Fig. 18. Noting that Q_1 is assumed to be turned ON by the step input and Q_2 is OFF, the output voltage becomes

$$v_O(t) \cong -\frac{1}{C_c}\int_0^t [2I_1 + i_S(t)]\, dt. \qquad (38)$$

The voltage at the emitter of Q_1 is essentially the same as the input voltage, $v_i(t)$, so the current in the "tail" capacitance C_s is

$$i_s(t) \cong C_s\frac{dv_i}{dt} \cong \frac{C_sV_{ip}}{t_1} \qquad 0 < t < t_1. \qquad (39)$$

Combining (38) and (39), $v_O(t)$ is

$$-v_O(t) \cong \frac{1}{C_c}\int_0^t 2I_1\, dt + \frac{1}{C_c}\int_0^{t_1} \frac{C_sV_{ip}}{t_1}\, dt \qquad (40)'$$

or

$$-v_O(t) \cong \frac{C_s}{C_c} V_{ip} + \frac{2I_1t}{C_c}. \qquad (41)$$

Equation (41) tells us that the output has an initial negative step which is the fraction C_s/C_c of the input voltage. This is followed by a normal slewing response, in which the slew rate is identical to that of the inverter, see (18). This response is illustrated in Fig. 18.

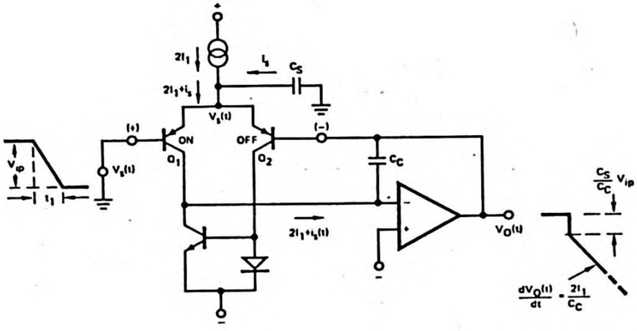


Fig. 18. Circuit used for calculation of slew "enhancement" in the voltage follower. The fast falling input causes a step output followed by a normal slew response as shown.

VI. Limitations on Bandwidth

In earlier sections, all bandlimiting effects were ignored except that of the compensation capacitor, C_c. The unity-gain frequency was set at a point sufficiently low so that negligible excess phase (over the 90° from the dominant pole) due to second-order (high frequency) poles had built up. In this section the major second-order poles which contribute to bandlimiting in the op amp are identified.

A. The Input Stage: p-n-p's, the Mirror Pole, and the Tail Pole

For many years it was popular to identify the lateral p-n-p's (which have f_t's $\cong$ 3 MHz) as the single dominant source of bandlimiting in the IC op amp. It is quite true that the p-n-p's do contribute significant excess phase to the amplifier, but it is not true that they are the sole contributor to excess phase [9]. In the input stage, alone, there is at least one other important pole, as illustrated in Fig. 19(a). For the simple differential input stage driving a differential-to-single ended converter ("mirror" circuit), it is seen that the inverting signal (which is the feedback signal) follows two paths, one of which passes through the capacitance C_s, and the other through C_m. These capacitances combine with the dynamic resistances at their nodes to form poles designated the mirror pole at

$$p_m \cong \frac{I_1}{C_m kT/q}, \qquad (42)$$

and the tail pole at

$$p_t \cong \frac{2I_1}{C_s kT/q}. \qquad (43)$$

It can be seen that if one attempts to operate the first stage at too low a current, these poles will bandlimit the amplifier. If, for example, we choose $I_1 = 1\ \mu$A, and assume $C_m \cong 7$ pF (consisting of 4-pF isolation ca-

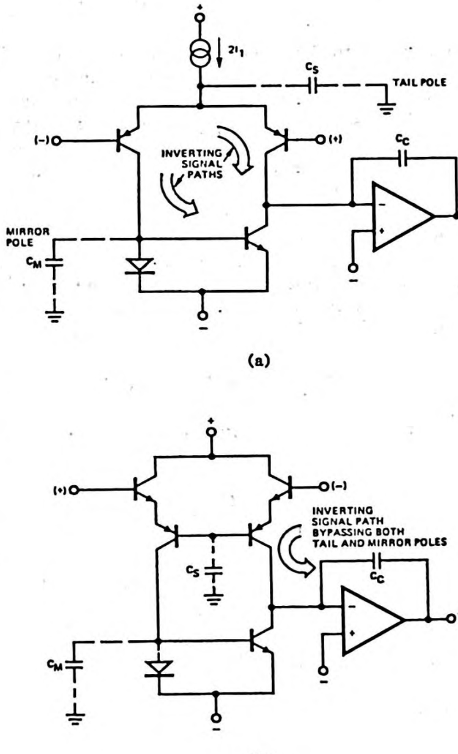


Fig. 19. (a) Circuit showing "mirror" pole due to C_m and "tail" pole due to C_s. One component of the signal due to an inverting input must pass through either the mirror or tail poles. (b) Alternate circuit to Fig. 19(a) (LM101, μA741) which has less excess phase. Reason is that half the inverting signal path need not pass through the mirror pole or the tail pole.

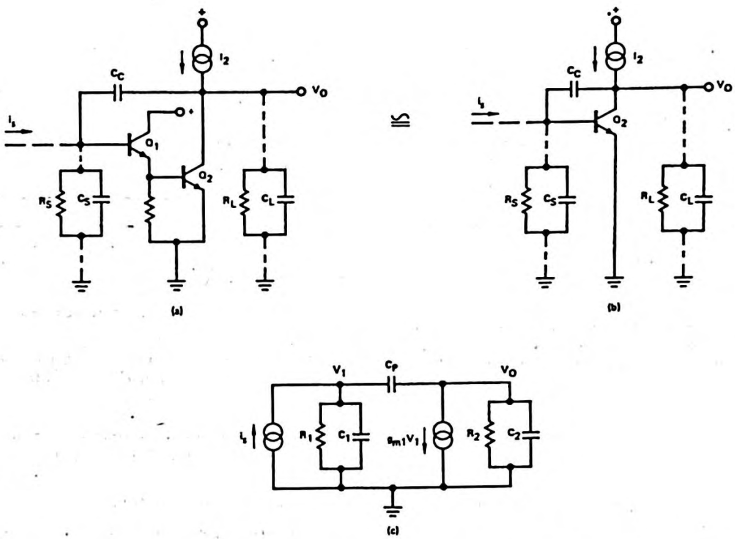


Fig. 20. Simplification of second stage used for pole-splitting analysis. (a) Complete second stage with input stage and output stage loading represented by R_s, C_s, and R_L, C_L, respectively. (b) Emitter follower ignored to simplify analysis. (c) Hybrid π model substituted for transistor in (b). Source and load impedances are absorbed into model with the total impedances represented by R_1, C_1, and R_2, C_2. Transistor base resistance is ignored and C_p includes both C_c and transistor collector-base capacitance.

pacitance and 3-pF emitter transition capacitance) and $C_s \cong 4$ pF,[3] $p_m/2\pi \cong 0.9$ MHz and $p_t/2\pi \cong 3$ MHz either of which would seriously degrade the phase margin of a 1-MHz amplifier.

If a design is chosen in which either the tail pole or the mirror pole is absent (or unimportant), the remaining pole rolls off only half the signal, so the overall response contains a pole-zero pair separated by one octave. Such a pair generally has a small effect on amplifier response unless it occurs near ω_u, where it can degrade phase margin by as much as 20°.

It is interesting to note that the compound input stage of the classical LM101 (and μA741) has a distinct advantage over the simple differential stage, as seen in Fig. 19(b). This circuit is noninverting across each half, thus it provides a path in which half the feedback signal bypasses both the mirror and tail poles.

B. The Second Stage: Pole Splitting

The assumption was made in Section III that the second stage behaved as an ideal integrator having a single dominant pole response. In practice, one must take care in designing the second stage or second-order poles can cause significant deviation from the expected response. Considerable insight into the basic way in which the second stage operates can be obtained by performing a small-signal analysis on a simplified version of the circuit as shown in Fig. 20 [10]. A straightforward two-node analysis of Fig. 20(c) produces the following expression for v_{out}.

$$\frac{v_{out}}{i_s} = \frac{-g_m R_1 R_2 (1 - sC_p/g_m)}{1 + s[R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_m R_1 R_2 C_p] + s^2 R_1 R_2 [C_1 C_2 + C_p(C_1 + C_2)]}. \tag{44}$$

The denominator of (44) can be approximately factored under conditions that its two poles are widely separated. Fortunately, the poles are, in fact, widely separated under most normal operating conditions. Therefore, one can assume that the denominator of (44) has the form

$$\begin{aligned} D(s) &= (1 + s/p_1)(1 + s/p_2) \\ &= 1 + s(1/p_1 + 1/p_2) + s^2/p_1 p_2. \end{aligned} \tag{45}$$

With the assumption that p_1 is the dominant pole and

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[3] C_s can have a wide range of values depending on circuit configuration. It is largest for n-p-n input differential amps since the current source has a collector-substrate capacitance ($C_s \cong$ 3–4 pF) at its output. For p-n-p input stages it can be as small as 1–2 pF.

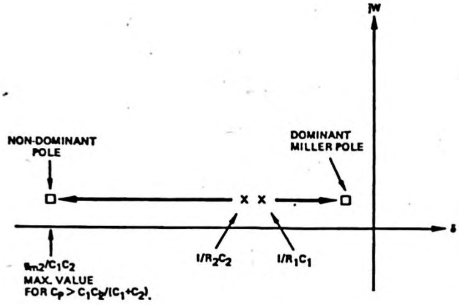


Fig. 21. Pole migration for second stage employing "pole-splitting" compensation. Plot is shown for increasing C_p and it is noted that the nondominant pole reaches a maximum value for large C_p.

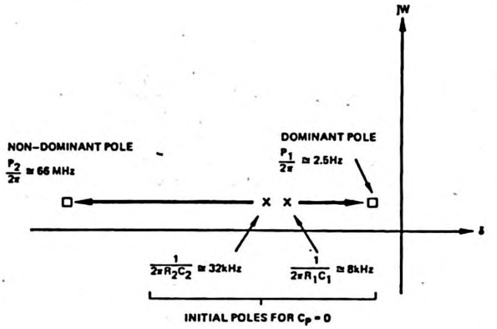

jw
NON–DOMINANT POLE
$\frac{P_2}{2\pi} \cong 66$ MHz
DOMINANT POLE
$\frac{P_1}{2\pi} \cong 2.5$Hz
s
$\frac{1}{2\pi R_2C_2} \cong 32$kHz
$\frac{1}{2\pi R_1C_1} \cong 8$kHz
INITIAL POLES FOR $C_p = 0$

Fig. 22. Example of pole-splitting compensation in the μA741 op amp. Values used in (48) and (49) are: $g_{m2} = 1/87\ \Omega$, $C_p = 30$ pF, $C_1 \cong C_2 = 10$ pF, $R_1 = 1.7$ MΩ, $R_2 = 100$ kΩ.

p_2 is nondominant, i.e., $p_1 \ll p_2$, (45) becomes

$$D(s) \cong 1 + s/p_1 + s^2/p_1p_2. \tag{46}$$

Equating coefficients of s in (44) and (46), the dominant pole p_1 is found directly:

$$p_1 \cong \frac{1}{R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_mR_1R_2C_p} \tag{47}$$

$$\cong \frac{1}{g_mR_1R_2C_p}. \tag{48}$$

The latter approximation, (48), normally introduces little error, because the g_m term is much larger than the other two. We note at this point that p_1, which represents the dominant pole of the amplifier, is due simply to the familiar Miller-multiplied feedback capacitance $g_mR_2C_p$ combined with input node resistance, R_1. The nondominant pole p_2 is found similarly by equating s^2 coefficients in (44) and (46) to get p_1p_2, and dividing by p_1 from (48). The result is

$$p_2 \cong \frac{g_mC_p}{C_1C_2 + C_p(C_1 + C_2)}. \tag{49}$$

Several interesting things can be seen in examining (48) and (49). First, we note that p_1 is inversely proportional to g_m (and C_p), while p_2 is directly dependent on g_m (and C_p). Thus, as either C_p or transistor gain are increased, the dominant pole decreases and the nondominant pole increases. The poles p_1 and p_2 are being "split-apart" by the increased coupling action in a kind of inverse root locus plot.

This *pole-splitting* action is shown in Fig. 21, where pole migration is plotted for C_p increasing from 0 to a large value. Fig. 22 further illustrates the action by giving specific pole positions for the μA741 op amp. It is seen that the initial poles (for $C_p = 0$) are both in the tens of kilohertz region and these are predicted to reach 2.5 Hz ($p_1/2\pi$) and 66 MHz ($p_2/2\pi$) after compensation is applied. This result is, of course, highly satisfactory since the second stage now has a single dominant pole effective over a wide frequency band.

C. Failure of Pole Splitting

There are several situations in which the application of pole-splitting compensation may not result in a single dominant pole response. One common case occurs in very wide-band op amps where the pole-splitting capacitor is small. In this situation the nondominant pole given by (49) may not become broadbanded sufficiently so that it can be ignored. To illustrate, suppose we attempt to minimize power dissipation by running the second stage of an LM118 (which has a small-signal bandwidth of 16 MHz) at 0.1 mA. For this op amp $C_p = 5$ pF, $C_1 \cong C_2 \cong 10$ pF. From (49), the nondominant pole is

$$\frac{p_2}{2\pi} \cong 16 \text{ MHz} \tag{50}$$

which lies right at the unity-gain frequency. This pole alone would degrade phase margin by 45°, so it is clear that we need to bias the second stage with a collector current greater than 0.1 mA to obtain adequate g_m. Insufficient pole-splitting can therefore occur; but the cure is usually a simple increase in second stage g_m.

A second type of pole-splitting failure can occur, and it is often much more difficult to cope with. If, for example, one gets over-zealous in his attempt to broadband the nondominant pole, he soon discovers that other poles exist within the second stage which can cause difficulties. Consider a more exact equivalent circuit for the second stage of Fig. 20(a) as shown in Fig. 23. If the follower is biased at low currents or if C_p, Q_2 g_m, and/or r_x are high, the circuit can contain at least four important poles rather than the two considered in simple pole splitting. Under these conditions, we no longer have a response with just negative real poles as in Fig. 21, but observe a root locus of the sort shown in Fig. 24. It is seen in this case that the circuit contains a pair of com-

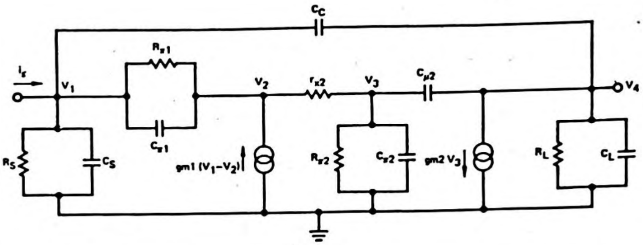


Fig. 23. More exact equivalent circuit for second stage of Fig. 20 (a) including a simplified π model for the emitter follower ($R_{\pi 1}$, $C_{\pi 1}$, g_{m1}) and a complete π for Q_2 (r_{x2}, $R_{\pi 2}$, etc.).

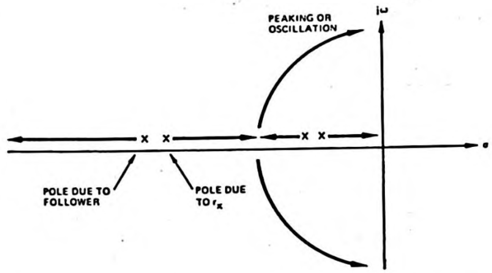


Fig. 24. Root locus for second stage illustrating failure of pole splitting due to high g_{m2}, r_{x2}, C_p, and/or low bias current in the emitter follower.

plex, possibly underdamped poles which, of course, can cause peaking or even oscillation. This effect occurs so commonly in the development of wide-band pole-split amplifiers that it has been (not fondly) dubbed "the second stage bump."

There are numerous ways to eliminate the "bump," but no single cure has been found which is effective in all situations. A direct hand analysis of Fig. 23 is possible, but the results are difficult to interpret. Computer analysis seems the best approach for this level of complexity, and numerous specific analyses have been made. The following is a list of circuit modifications that have been found effective in reducing the bump in the various studies: 1) reduce g_{m2}, r_{x2}, $C_{\mu 2}$, 2) add capacitance or a series RC network from the stage input to ground—this reduces the high frequency local feedback due to C_p, 3) pad capacitance at the output for similar reasons, 4) increase operating current of the follower, 5) reduce C_p, 6) use a higher f_t process.

D. Troubles in The Output Stage

Of all the circuitry in the modern IC op amp, the class-AB output stage probably remains the most troublesome. None of the stages in use today behave as well as one might desire when stressed under worst case conditions. To illustrate, one of the most commonly used output stages is shown in Fig. 2(b). The p-n-p's in this circuit are "substrate" p-n-p's having low current f_t's of around 20 MHz. Unfortunately, both β_0 and f_t begin to fall off rapidly at quite low current densities, so as one begins to sink just a few milliamps in the circuit, phase margin troubles can develop. The worst effect occurs when the amplifier is operated with a large capacitive load (>100 pF) while sinking high currents. As shown in Fig. 25, the load capacitance on the output follower causes it to have negative input conductance, while the driver follower can have an inductive output impedance. These elements combine with the capacitance at the interstage to generate the equivalent of a one-port oscillator. In a carefully designed circuit, oscillation is suppressed, but peaking (the "output bump") can occur in most amplifiers under appropriate conditions.

One new type of output circuit which does not use p-n-p's is shown in Fig. 26 [6]. This circuit employs compatible JFET's (or MOSFET's, see similar circuit in [11]) in a FET/bipolar quasi-complimentary output stage, which is insensitive to load capacitance. Unfortunately, this circuit is rather complex and employs extra process steps, so it does not appear to represent the cure for the very low cost op amps.

VII. THE GAIN CELL: LINEAR LARGE-SCALE INTEGRATION

As the true limitations of the basic op amp are more fully understood, this knowledge can be applied to the development of more "optimum" amplifiers. There are, of course, many ways in which one might choose to optimize the device. We might, for example, attempt to maximize speed (bandwidth, slew rate, settling time) without sacrificing dc characteristics. The compatible JFET/bipolar amp of Fig. 15 represents such an effort. An alternate choice might be to design an amplifier having all of the performance features of the most widely used general purpose op amps (i.e., μA741, LM107, etc.), but having minimum possible die area. Such a pursuit is parallel to the efforts of digital large-scale integration (LSI) designers in their development of minimum area

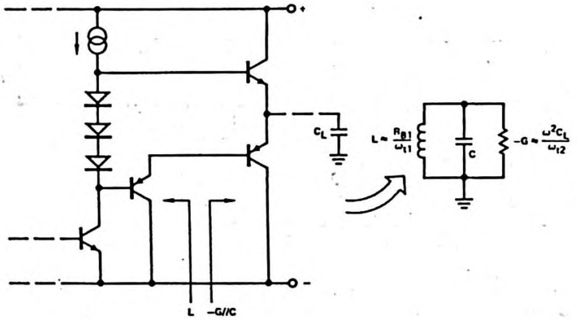

+
C_L
$L \approx \frac{R_{B1}}{\omega_{t1}}$
C
$-G \approx \frac{\omega^2 C_L}{\omega_{t2}}$
-
L
-G//C

Fig. 25. Troubles in the conventional class-AB output stage of Fig. 2(b). The low f_t output p-n-p's interact with load capacitance to form the equivalent of a one-port oscillator.

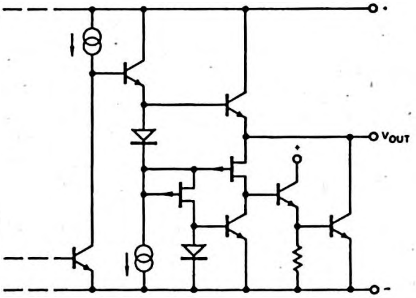


Fig. 26. The "BIFET" output stage employing JFET's and bipolar n-p-n's to eliminate sensitivity to load capacitance.

memory cells or gates. The object of such efforts, of course, is to develop lower cost devices which allow wide and highly economic usage.

In this section we briefly discuss certain aspects of the linear *gain cell,* a general purpose, internally compensated op amp having a die area which is significantly smaller than that of equivalent, present day, industry standard amplifiers.

A. Transconductance Reduction

The single largest area component in the internally compensated op amp is the compensation capacitor (about 30 pF, typically). A major interest in reducing amplifier die area, therefore, centers about finding ways in which this capacitor can be reduced in size. With this in mind, we find it useful to examine (15), which relates compensation capacitor size to two other parameters, unity gain corner frequency ω_u, and first stage transconductance g_{m1}. It is immediately apparent that for a fixed, predetermined unity gain corner (about $2\pi \times 1$ MHz in our case), there is only one change that can be made to reduce the size of C_c: *the transconductance of the first stage must be reduced.* If we restrict our interest to simple bipolar input stages (for low cost), we recall the $g_{m1} = qI_1/kT$. Only by reducing I_1 can g_{m1} be reduced, and we earlier found in Section VI–A and Fig. 19(a) and (b) that I_1 cannot be reduced much without causing phase margin difficulties due to the mirror pole and the tail pole.

An alternate basic approach to g_m reduction is illustrated in Fig. 27 [12]. Here, a multiple collector p-n-p structure, which is easily fabricated in IC form, is used to split the collector current into two components, one component (the larger) of which is simply tied to ground, thereby "throwing away" a major portion of the transistor output current. The result is that the g_m of the transistor is reduced by the ratio of $1/(1 + n)$ (see Fig. 27), and the compensation capacitance can be reduced directly by the same factor. It might appear that the mirror pole would still cause difficulties since the current mirror becomes current starved in Fig. 27, but the effect is not as severe as might be expected. The

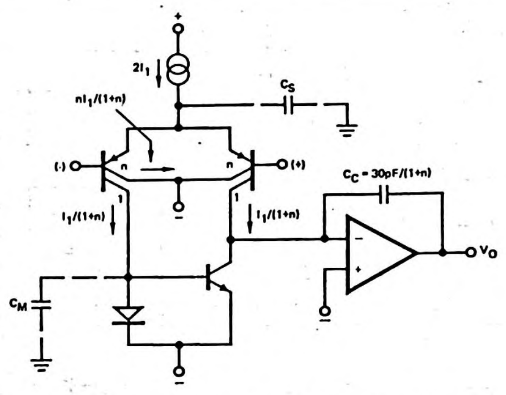
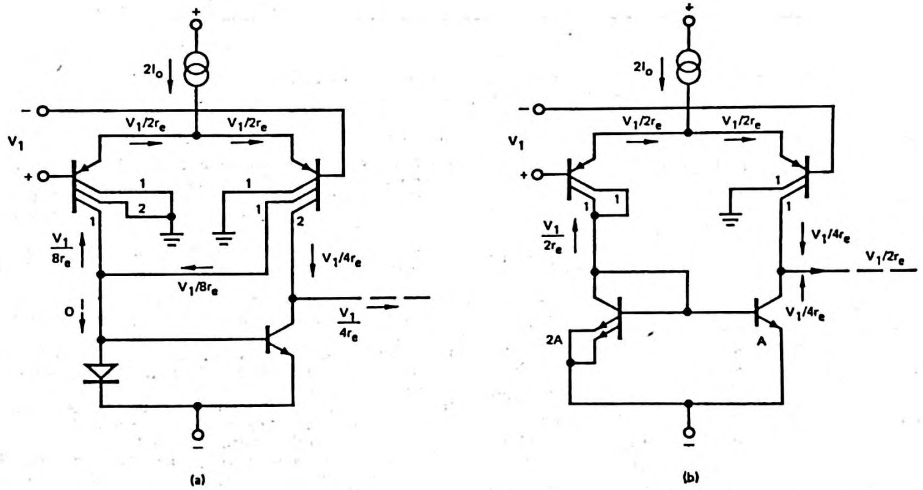


Fig. 27. Basic g_m reduction obtained by using split collector p-n-p's. C_c and area are reduced since $C_c = g_{m1}/\omega_u$.



(a)

(b)

Fig. 28. Variations on g_m reduction. (a) Cross-coupled connection eliminates all ac current passing through the mirror, yet maintains dc balance. (b) This approach maintains high current on the diode side of the mirror, thereby broadbanding the mirror pole.

reason is that the inverting signal can now pass through the high current wide-band path, across the differential amp emitters and into the second stage, so at least half the signal current does not become bandlimited. This partial bandlimiting can be further reduced by using one of the circuits in Fig. 28(a) or (b).[4] In (a), the p-n-p collectors are cross coupled in such a way that the ac signal is cancelled in the mirror circuit, while dc remains completely balanced. Thus the mirror pole is virtually eliminated. The circuit does have a drawback, however, in that the uncorrellated noise currents coming from the two p-n-p's add rather than subtract at the input to the mirror, thereby degrading noise performance. The circuit in Fig. 28(b) does not have this defect, but requires care in matching p-n-p collector ratios to n-p-n emitter areas. Otherwise offset and drift will degrade as one attempts to reduce g_m by large factors.

B. A Gain Cell Example

As one tries to make large reductions in die area for the gain cell, many factors must be considered in addition to novel circuit approaches. Of great importance are special layout/circuit techniques which combine a maximum number of components into minimum area.

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[4] The circuit in Fig. 28(a) is due to R. W. Russell and the variation in Fig. 28(b) was developed by D. W. Zobel.

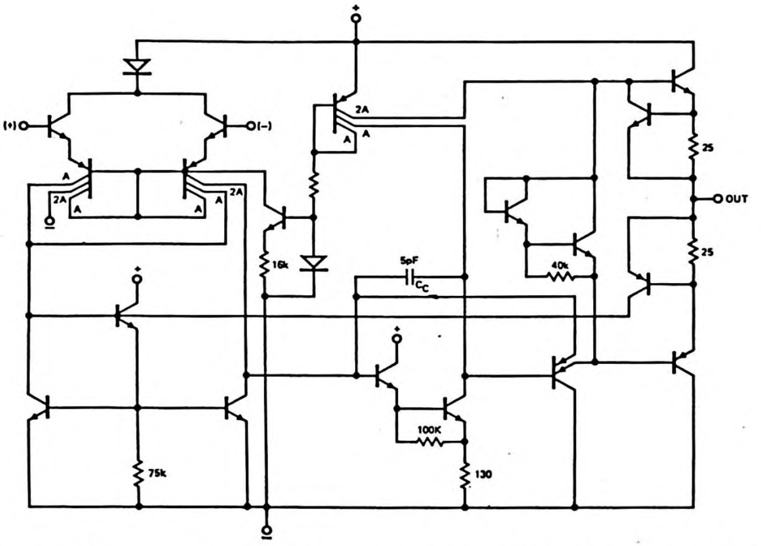

Fig. 29. Circuit for optimized gain cell which has been fabricated in one-fourth the die size of the equivalent μA741.

In a good layout, for example, all resistors are combined into islands with transistors. If this is not possible initially, circuit and device changes are made to allow it. The resulting device geometries within the islands are further modified in shape to allow maximum "packing" of the islands. That is, when the layout is complete, the islands should have shapes which fit together as in a picture puzzle, with no waste of space. Further area reductions can be had by modifying the isolation process to one having minimum spacing between the isolation diffusion and adjacent p-regions.

An example of a gain cell which employs both circuit and layout optimization is shown in Fig. 29. This circuit uses the g_m reduction technique of Fig. 28(a) which results in a compensation capacitor size of only 5 pF rather than the normal 30 pF. The device achieves a full 1-MHz bandwidth, a 0.67-V/μs slew rate, a gain greater than 100 000, typical offset voltages less than 1 mV, and other characteristics normally associated with an LM107 or μA741. In quad form each amplifier requires an area of only 23 × 35 mils which is one-fourth the size of today's industry standard μA741 (typically 56 × 56 mils). This allows over 8000 possible gain cells to be fabricated on a single 3-inch wafer. Further, it appears quite feasible to fabricate larger arrays of gain cells, with six or eight on a single chip. Only packaging and applications questions need be resolved before pursuing such a step.

ACKNOWLEDGMENT

Many important contributions were made in the gain cell and FET/bipolar op amp areas by R. W. Russell. The author gratefully acknowledges his very competent efforts.

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See also, as a general reference:

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A Color TV Primer for the E. E.

National Semiconductor
Appendix B
Milt Wilcox
October 1975

Section 1 — The Color TV Receiver

Let's look at a color TV in terms of signal flow, from antenna to picture tube.

Although the frequencies used will be for the American NTSC system (National Television System Committee), the basic theory also applies to the European PAL system (Phase Alternating Line). Only in the chroma section do the two systems differ significantly.

RF AND IF SECTIONS

The first part is easy — all signal components received from the antenna pass through a tuner and IF amplifier to the video detector as shown in *Figure 1.*

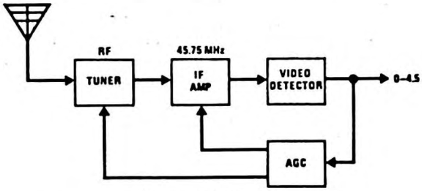

FIGURE 1

The RF signal received ranges in frequency from 55 MHz for channel 2 up to 885 MHz (tuned with the aid of a UHF converter) for channel 831 The tuner has the job of amplifying the desired channel frequency and converting it to an intermediate frequency (IF) of 45.75 MHz. It is then further amplified in the IF amplifier.

The 45.75 MHz signal being amplified is called the video carrier. It is amplitude-modulated (AM) with the picture information, so the video detector must strip this information from the carrier by using some form of envelope detection. So far we could be describing a basic AM radio, except for the signal being received — instead of having audio at the detector output, we have video.

The output level from the video detector is usually around 3 Vp-p. This level must be produced by as little as 10μVrms on the antenna, which works out to 110 dB conversion gain for the three blocks shown in *Figure 1.* However, the catch is the same TV may have to receive antenna signals of up to 0.5 Vrms, and *still produce the same 3 Vp-p* at the video detector. For this reason, a TV has a very effective automatic gain control (AGC) system which detects increases in the peak amplitude of the composite video signal and automatically reduces the gain of the tuner and IF amplifier to compensate.

SIGNAL INFORMATION

The picture you see on a color TV is actually formed by three electron beams, one each for red, blue and green being scanned horizontally and vertically over the screen. As these beams are scanned, their currents are changed to create the light and dark areas on the picture tube face which form the image you view. *Figure 2* shows the video detector output during the time that it takes the electron beams to make one horizontal scan across the screen. The output is actually a combination of four signal components which are required to form a color picture with sound. Let's look at them in turn:

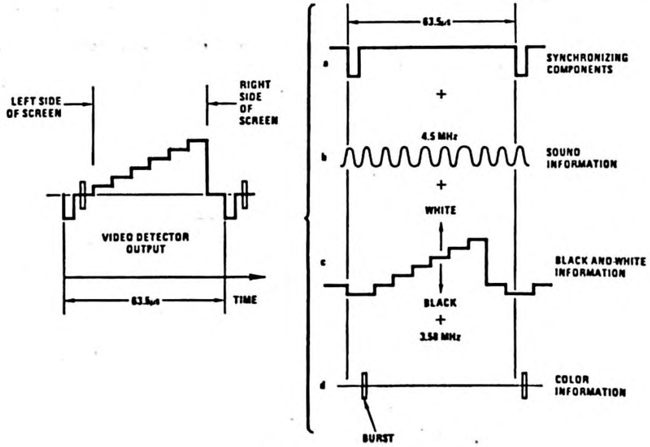

FIGURE 2

a) Synchronizing Components

The synchronizing information is a series of pulses which tell the horizontal section when to return to the left of the screen to start a new *line*, and the vertical section when to return to the top of the screen to start a new *frame*. In the NTSC system each frame contains 525 lines. This is done by scanning the horizontal at approximately 15,750 lines per second, and the vertical at 30 frames per second (the vertical scan rate is actually 60 Hz, but it takes two trips down the screen to complete one frame). The process of returning to start a new scan is called retrace or flyback.

b) Sound Information

The sound information is carried in the form of frequency-modulation (FM) of a 4.5 MHz carrier which in turn modulates the video carrier. (That makes the 4.5 MHz a "sub-carrier"). This sub-carrier is very similar to the IF signal in an FM radio. Although the sound sub-carrier is available at the video detector, a separate detector is often used to reduce crosstalk between signal components.

c) Black-and-White Information (called luminance)

This information determines the instantaneous brightness of the electron beams as they are scanned over the screen. In fact, it is all that is used for the single electron beam in a black-and-white TV set. A negative going video detector detects a luminance signal in which the negative signal extremes correspond to dark areas of the picture and positive signal extremes correspond to bright areas of the picture. Thus the waveform shown in *Figure 2(c)* would produce vertical bars of increasing brightness from left to right. Note that the output is at black during retrace so the electron beams will not be seen. The luminance signal is designated by the letter Y.

d) Color Information (called chrominance)

The color information (which is ignored in a black-and-white TV) is made up of the red, blue and green signals required to drive the picture tube, *minus* the luminance signal. These "color difference" signals, designated R-Y, B-Y and G-Y, modulate a second subcarrier which has a frequency of 3.58 MHz.

Although the type of modulation used on the sub-carrier is of a complex nature it boils down to a simple result:

1. The instantaneous *phase* of the 3.58 MHz signal determines *what* color will be displayed (called hue or tint).
2. The instantaneous *amplitude* of the 3.58 MHz signal determines *how much* color will be displayed (called saturation).

An obvious question is, the phase and amplitude of the 3.58 MHz signal relative to what? The answer is a short burst of 3.58 MHz (simply called the *burst*) which has constant phase and amplitude. The burst will be used to determine the tint and saturation of the color to be displayed. For the waveform shown in *Figure 2(d)* each bar would have a different saturation.

The four signal components are separated and sent to their respective sections in the TV according to the type of signal. Since the sync pulses are the negative peaks of the composite video signal, a peak-detector circuit called a *sync-separator* is used to separate them. The sound and chroma information is contained in sub-carriers which are separated with 4.5 MHz and 3.58 MHz tuned-circuits respectively. The luminance information combines frequency components from 0—4 MHz and therefore uses wideband dc-coupling.

SIGNAL PROCESSING

The remaining sections of the Receiver will now be covered.

Scanning and High Voltage

The sync section is shown in *Figure 3*.

The sync pulses separated in the sync-separator are divided into vertical and horizontal components according to their pulse widths, the vertical sync pulse being a string of wide horizontal sync pulses. When these wide pulses are fed through an integrator, they average to form the vertical sync pulse. The vertical oscillator is "injection-locked" by the vertical sync pulse to initiate vertical retrace at the correct time. The output stage then delivers a ramp of current to the vertical deflection coils to produce vertical scan.

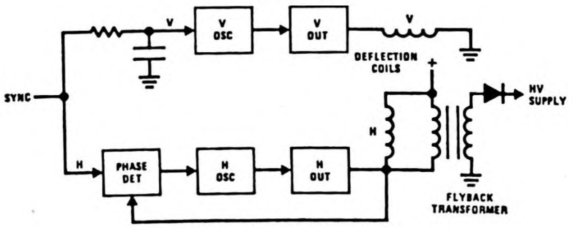

FIGURE 3

The horizontal section uses a different locking system, since horizontal retrace is started *before* the sync pulse is received in order to assure correct centering of the picture. This is done with a phase-locked loop (PLL) in which the oscillator is controlled by a phase detector to insure correct timing between the horizontal sync pulse and the flyback pulse produced by the output stage during horizontal retrace. The horizontal output stage does double duty — besides driving the horizontal deflection coils, it drives the flyback transformer for the picture tube anode high voltage supply. The 25–30 thousand volts dc required is generated either by directly rectifying or by tripling a hv flyback pulse derived from a large turns ratio on the flyback transformer.

The Sound Channel

The 4.5 MHz sound-subcarrier signal is amplified and limited in the sound IF to remove undesired amplitude information. The frequency modulation is then detected by an FM detector and applied to the audio amplifier.

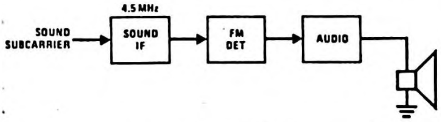

FIGURE 4

Limiting sensitivity for the sound section is typically 100μV and the output power requirement is from 1W to 4W depending on receiver size.

Luma Processing

The luminance signal Y must be amplified and delayed some 0.8μs on its way to the picture tube as shown in *Figure 5.* The delay is required to insure that the black and white information does not arrive at the picture tube before the color information, which is delayed by the comparatively narrow bandwidth of the 3.58 MHz chroma section.

The contrast and brightness controls are also located in the luminance amplifier. The *contrast* control changes the *peak-to-peak* amplitude of the signal, while the *brightness* control changes the *dc* level of the signal.

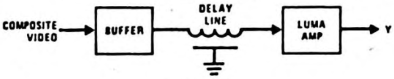

FIGURE 5

Chroma Processing

From the signal taken off the 3.58 MHz tuned circuit the chroma section must derive two signals:

1) The 3.58 MHz chroma sub-carrier signal of the correct amplitude and

2) A continuous 3.58 MHz chroma reference signal of the correct phase relative to the burst.

These two signals, when applied to the chroma demodulator, will produce the desired color difference signals R-Y, B-Y and G-Y. The chroma section is shown in *Figure 6.*

The first problem is that even though the AGC system holds the peak-to-peak video level constant, the chroma sub-carrier itself can vary in amplitude with transmission, antenna and fine-tuning changes, to name a few. Therefore, the chroma section requires an AGC loop of its own, which is called the Automatic Chroma Control stage, or ACC. This block compares the amplitude of the burst to a reference to keep the chroma output signal constant over a 20 dB input range.

The chroma signal is then gated into two components by a pulse derived from the horizontal section. The chroma sub-carrier (during horizontal scan) is sent to the chroma amplifier in which a gain control varies the saturation of the color picture. If *no* burst was present in the ACC stage, the output of the amplifier is "killed" completely for black and white reception.

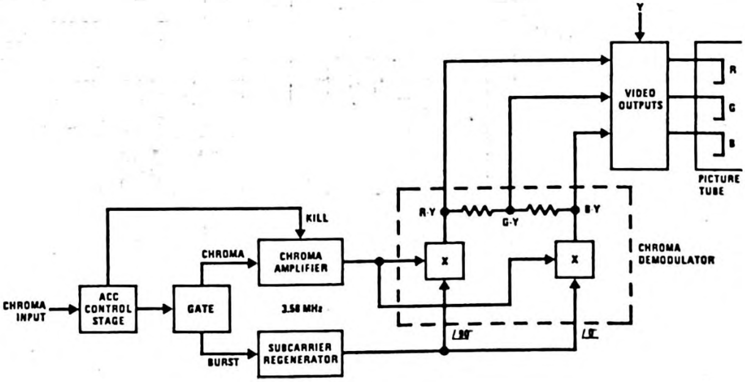

FIGURE 6

The burst (during horizontal retrace) is sent to the sub-carrier regenerator. This is actually a fancy name for a crystal-controlled 3.58 MHz oscillator which is locked to the frequency and phase of the incoming burst by either an injection-lock or phase-lock technique. This forms the reference output, which is passed through a variable phase-shift network to vary the tint of the color picture.

The outputs of the chroma amplifier and sub-carrier regenerator are the signals required by the chroma demodulator, which consists of two synchronous detectors operated in quadrature. What this means is that the reference phase applied to the B-Y detector makes it responsive only to chroma input phases corresponding to blue. The reference applied to the R-Y detector, which is 90° out of phase with the B-Y detector, makes it responsive only to red. The G-Y signal is derived by combining the R-Y and B-Y outputs in the correct ratios.

Finally, the luminance signal Y is added to the chroma difference signals R-Y, B-Y and G-Y to arrive at the desired red, blue and green signals. These signals are further amplified to 100 Vp-p in the video output stage and applied to the appropriate cathodes of the picture tube.

CONVERGENCE

One other messy, but needed, function remains in a color TV receiver — color convergence. The need for convergence results from the origination of the three electron beams in different locations and the fact that they are being scanned over a flat, instead of round, surface. Therefore, the deflection of each beam must be modified separately such that it lands in the same location as the other beams over the entire face of the picture tube.

A complete block diagram of the color TV receiver is shown for reference in *Figure 7.*

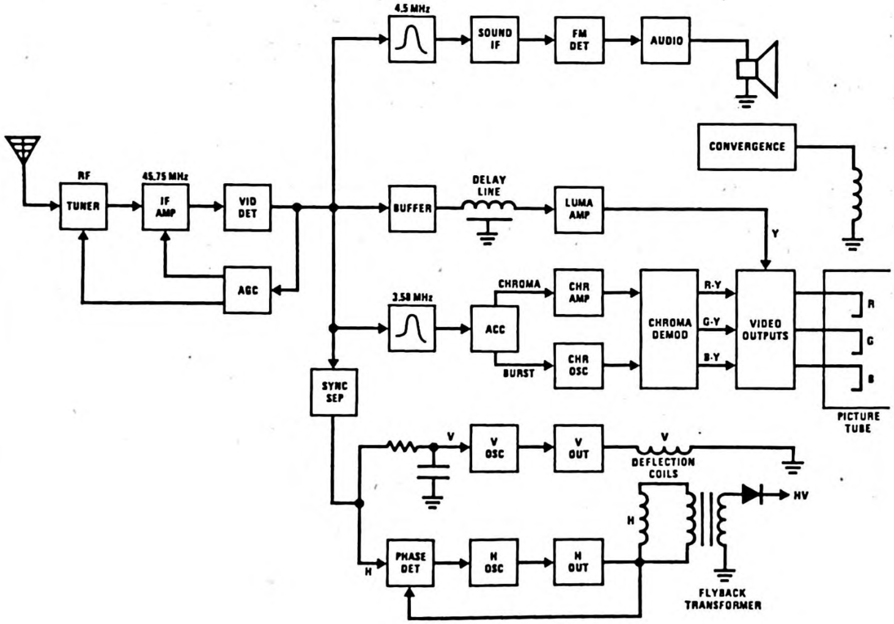
4.5 MHz
SOUND IF
FM DET
AUDIO
CONVERGENCE
RF
45.75 MHz
TUNER
IF AMP
VID DET
AGC
BUFFER
DELAY LINE
LUMA AMP
Y
CHROMA
CHR AMP
3.58 MHz
ACC
BURST
CHR OSC
CHROMA DEMOD
R-Y
G-Y
B-Y
VIDEO OUTPUTS
R
G
B
PICTURE TUBE
SYNC SEP
V
V OSC
V OUT
V
DEFLECTION COILS
HV
H
FLYBACK TRANSFORMER
H
PHASE DET
H OSC
H OUT

FIGURE 7

Section 2 — Integrated Circuits in Television

Here we will look at the integrated circuits used in television including a glimpse inside TV ICs.

Every area of the television which does not have too high a frequency or voltage requirement has been integrated at least once, and many are on second and third generation IC's. The only areas that have been "off-limits" to date are the tuner, video outputs, and horizontal/HV output sections.

RF AND IF SECTIONS

Monolithic circuits have been made to work very well at 45 MHz. The first IC IF systems used 2 chips: one for a 2-stage gain-controlled IF amplifier (Motorola MC1349, 52) and the second for a video detector with gain (Motorola MC1330). The major obstacle to combining these two chips into a single chip has been stability problems due to internal and/or external coupling output to input. However a one chip IF amplifier and video detector is now widely used in Europe (Telefunken TDA 440). The AGC system is also often included in these chips. Another IF function used in most color TV receivers today is automatic fine tuning (AFT) which keeps the tuner correctly tuned to the IF frequency (LM3064 type).

The first chip to incorporate all of the above functions into a single chip is the National LM1807. The chip uses a phase-locked loop to tune the tuner to the IF frequency set by a local oscillator on the chip. This concept is new to TV and is generating a lot of interest.

Rapid progress is also being made in periphery circuits to tuners. Present IC tuning systems control the voltage on a varactor in the tuner to tune the desired channel. However, new systems will actually "synthesize" the tuner local oscillator frequency for each channel.

SCANNING

The deflection area is one of the last to be integrated. While only low-level horizontal circuits have been integrated, vertical drivers and even output stages have been attempted. Current IC's include the Motorola MC1391 or Philips TBA 920 for horizontal and the SGS TDS 1270 for vertical.

In the standard U.S. television system, the vertical and horizontal scanning frequencies are related by the formula $f_v = 2f_H/525$. The National DM8890 makes use of this fact by dividing down a horizontal signal to generate vertical timing, thus eliminating the need for a vertical hold control. Although previous combined vertical/horizontal chips have been unsuccessful, the digital approach holds much promise and TI has announced a combined chip using I^2L.

THE SOUND CHANNEL

The LM3065 type sound IF/FM Detector is currently used in most TV receivers along with a class B discrete or IC audio amplifier. However, virtually every IC manufacturer has announced a one chip "sound system" combining the IF, detector, and audio amplifier. National's entry is the LM1808 which has been well received.

LUMA PROCESSING

Standard IC's have not been developed for the Luma area because of questionable economics. Instead, most of the efforts so far have been custom, with different IC's being used by Zenith, Sylvania and several European TV companies.

CHROMA PROCESSING

The first IC in TV was the chroma demodulator. Today every color TV has one, usually an LM746 or LM1828 type. In one variation the luminance signal is added to the color difference outputs on the chip (Motorola MC1324).

The chroma amplifier and subcarrier regenerator sections have been integrated using a phase-locked loop system with two chips (LM3070 and LM3071 types) and an injection-locked system with one chip (Motorola MC1398). Both of these systems are widely used. Second generation systems which do the phase-locked system with one chip (RCA CA3126 or Motorola MC1399) are gaining acceptance. All of these systems can be used with the above-mentioned demodulators.

Thus, so far the chroma section takes a minimum of two chips, including the demodulator. When will the demodulator be combined with the rest of the system for a true one-chip chroma? Hitachi has just introduced the first practical attempt and others are sure to follow.

WHAT'S A JUNGLE?

A "jungle" IC is a combination of miscellaneous TV functions on one chip. For example, the Zenith jungle (LM1845 type) does the sync-separator and AGC functions. The term is also sometimes applied to deflection IC's which include other functions.

INSIDE TV IC's

Next to the basic differential amplifier, the most widely used linear circuits in TV IC's are probably the current-sharing gain control stage and the linear multiplier.

Gain Control

The current-sharing gain control stage is so named because the input current is shared between two outputs depending on the dc control voltage V_C. For the circuit shown in *Figure 8,* the small signal gain at room temperature is given by:

$$A = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \cong \frac{R_L/R_e}{1 + \exp\left(\frac{V_C \text{ in mV}}{26}\right)}$$

As V_C is increased, the circuit acts as a logarithmic attenuator, yielding a gain reduction of approximately 20 dB for each 60 mV of applied voltage. This same basic gain control stage is used in IF AGC and chroma ACC circuits, as well as for volume, contrast, and chroma controls.

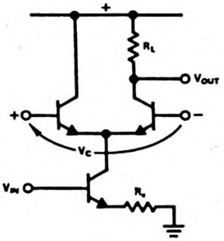

FIGURE 8

Multiplier

The multiplier is widely used in television IC's for amplitude, phase, and frequency detection. *Figure 9* shows a typical configuration in which the bottom pair is degenerated for linear operation while the top quad is switched. If $V_a(t)$ is an amplitude modulated carrier $F_m(t)\cos \omega t$ and $v_b(t)$ is a square wave of the same frequency ω and relative phase ϕ, then the filtered output is given by:

$$V_{OUT} \cong \frac{2}{\pi}\ \frac{R_L}{R_e}\ F_m(t)\cos\phi$$

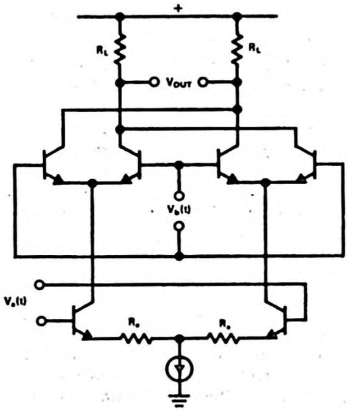

FIGURE 9

Thus the output depends on the amplitude of V_a and the relative phase ϕ between V_a and V_b.

If ϕ is made 0 degrees so COS ϕ is 1, then the multiplier acts as an amplitude detector and can be used to detect the video modulation on the IF carrier. Note that around 0 degrees COS ϕ changes very little with phase. To use the multiplier as a phase or frequency detector, $V_a(t)$ is limited to remove amplitude information and ϕ is centered at 90 degrees where COS ϕ produces the largest change in output for a given change in phase. This operation mode is used for chroma burst phase detectors and sound FM detectors. Both the amplitude and phase sensitive properties of the multiplier are used in chroma demodulators.

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Wide Range Timer

National Semiconductor
Linear Brief
Robert C. Dobkin
February 1977

One of the problems encountered in potentiometer controlled circuits is dynamic range. With a linear pot, about a 100:1 range is the limit. Although the pot resolution may be better than 1%, the angular displacement for good control becomes too small. Usually, range switching is then used.

A logarithmic control is a possible solution. With log controls, the resolution is the same anywhere within the operating range. For example, if 40° rotation is equal to a change from 10% to 100% of full scale, then 40° rotation is also equal to a change from 0.01% to 0.1% of full scale. It is easy to control a function over a 1,000,000:1 range with good control anywhere within the range.

The exponential relationship between the emitter-base voltage of a transistor and its collector current is well known. This relationship holds true within a few percent over extremely wide ranges. Using a transistor pair, and an op amp, it is easy to make a current source controllable over a 6 decade range.

Figure 1 shows a timer which can be adjusted from 2 ms to 2000 seconds with a single control. An LM122 is

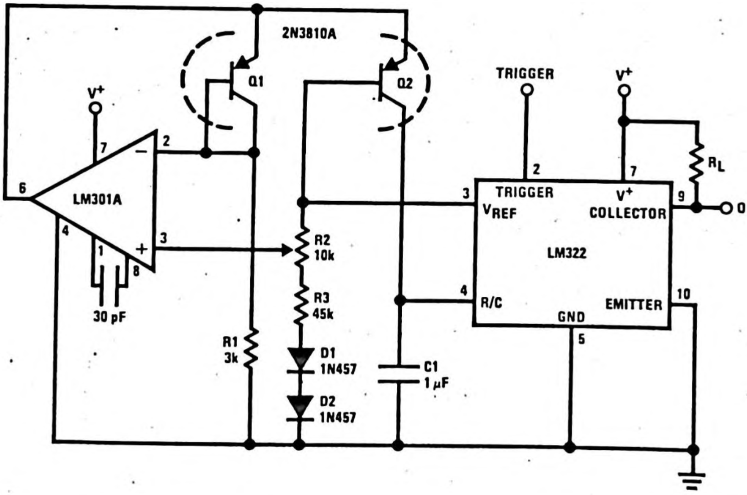

2N3810A
Q1
Q2
V+
7
2
6
LM301A
4
3
1
8
30 pF
R1
3k
R2
10k
R3
45k
D1
1N457
D2
1N457
C1
1 μF
TRIGGER
V+
2
7
RL
3
TRIGGER
VREF
V+
COLLECTOR
9
OUTPUT
LM322
4
R/C
EMITTER
10
GND
5

FIGURE 1. 2 ms to 2000 Second Timer

used for the timing function in conjunction with a current source that is logarithmically controlled from a pot. The operation is as follows:

Transistors Q1 and Q2 are a matched PNP pair. Resistor R1 and the op amp set up a constant current of 1 mA through Q1 using the internal 3V reference from the timer. With R2 at the most positive end of its range, the non-inverting input of the op amp is at V_{REF}. This forces the emitter-base voltage of Q2 to equal Q1 and since the transistors are matched, the collector current of Q2 is also 1 mA. A time-out period of 2 ms results.

Rotating R2 subtracts the voltage between the arm of the pot and V_{REF} from the emitter-base voltage of Q2—lowering its collector current. The current is decreased by a factor of 10 for every 60 mV developed. A total of 360 mV is dropped across the pot, allowing a reduction in Q2 collector current by a factor of 1,000,000 or from 1 mA to 1 nA. A 1 nA charging current gives a 2000 second time out. (At maximum time, there is about a 30% error due to the 0.3 nA input current of the comparator). Finally, diodes D1 and D2 temperature compensate the voltage across the pot.

Calibrating the circuit is relatively easy (except for obtaining a log dial for the pot). Resistor R1 is adjusted for the minimum operating time removing for mismatch in the transistors, capacitor tolerance, and the offset of the op amp. R3 is used to calibrate the full scale time by adjusting the drop across R2 to 360 mV.

This type of log control is not limited to timers. If used in oscillator or function generator circuits, an ultra wide range VCO can be made. Also, in power supply circuitry, it is possible for a regulator to have as much resolution when adjusted for 0.001V output as when the output is 10V. Finally, a log current generator makes an easily adjusted low value current source without high value resistors.

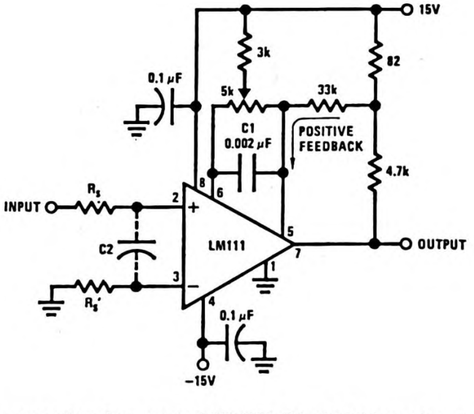
Circuit Techniques for Avoiding Oscillations in Comparator Applications

National Semiconductor
Linear Brief 39
Peter Lefferts
January 1978

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1.*
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



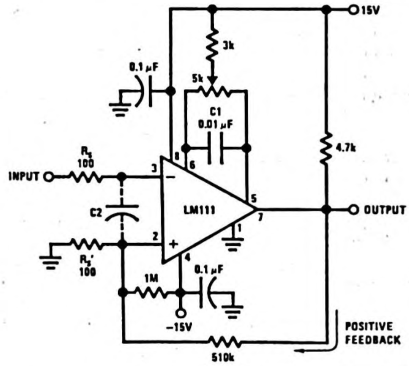
Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 1. Improved Positive Feedback

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2,* the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if the value of R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See paragraph 7, below, for the alternative.

7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and ensure sharp output transitions with input triangle waves from a few Hz to hundreds of kHz. The positive feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).


15V
3k
0.1 µF
5k
C1
0.01 µF
4.7k
R_S
100
INPUT
3
8
6
LM111
5
7
OUTPUT
C2
2
1
R_S'
100
4
0.1 µF
1M
−15V
POSITIVE
FEEDBACK
510k

Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 2. Conventional Positive Feedback

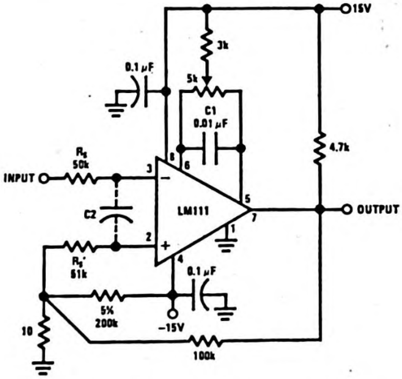

15V
3k
0.1 µF
5k
C1
0.01 µF
4.7k
R_S
50k
INPUT
3
8
6
LM111
5
7
OUTPUT
C2
2
1
R_S'
51k
4
0.1 µF
5%
200k
−15V
10
100k

FIGURE 3. Positive Feedback With High Source Resistance

The Monolithic Operational Amplifier: A Tutorial Study

National Semiconductor
Appendix A
James E. Solomon
December 1974

Invited Paper—
IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6

***Abstract*—A study is made of the integrated circuit operational amplifier (IC op amp) to explain details of its behavior in a simplified and understandable manner. Included are analyses of thermal feedback effects on gain, basic relationships for bandwidth and slew rate, and a discussion of pole-splitting frequency compensation. Sources of second-order bandlimiting in the amplifier are also identified and some approaches to speed and bandwidth improvement are developed. Brief sections are included on new JFET-bipolar circuitry and die area reduction techniques using transconductance reduction.**

I. INTRODUCTION

THE integrated circuit operational amplifier (IC op amp) is the most widely used of all linear circuits in production today. Over one hundred million of the devices will be sold in 1974 alone, and production costs are falling low enough so that op amps find applications in virtually every analog area. Despite this wide usage, however, many of the basic performance characteristics of the op amp are poorly understood.

It is the intent of this study to develop an understanding for op amp behavior in as direct and intuitive a manner as possible. This is done by using a variety of simplified circuit models which can be analyzed in some cases by inspection, or in others by writing just a few equations. These simplified models are generally developed from the single representative op amp configuration shown in Figs. 1 and 2.

The rationale for starting with the particular circuit of Fig. 1 is based on the following: this circuit contains, in simplified form, all of the important elements of the most commonly used integrated op amps. It consists essentially of two voltage gain stages, an input differential amp and a common emitter second stage, followed by a class-AB output emitter follower which provides low impedance drive to the load. The two interstages are frequency compensated by a single small "pole-splitting" capacitor (see below) which is usually included on the op amp chip. In most respects this circuit is directly equivalent to the general purpose LM101 [1], μA 741 [2], and the newer dual and quad op amps [3], so the results of our study relate directly to these devices. Even for more exotic designs, such as wide-band amps using feedforward [4], [5], or the new FET input circuits [6], the basic analysis approaches still apply, and performance details can be accurately predicted. It has also been found that a good understanding of the limitations of the circuit in Fig. 1 provides a reasonable starting point from which higher performance amplifiers can be developed.

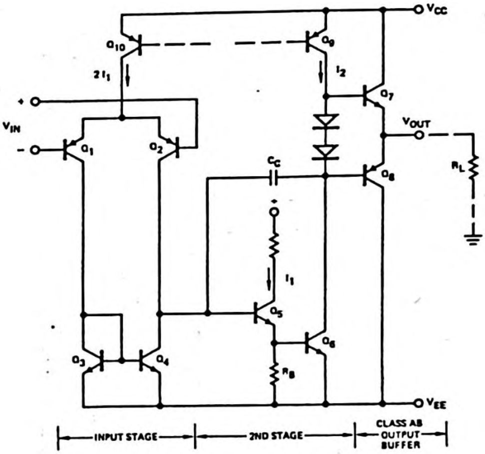


Fig. 1. Basic two-stage IC op amp used for study. Minimal modifications used in actual IC are shown in Fig. 2.

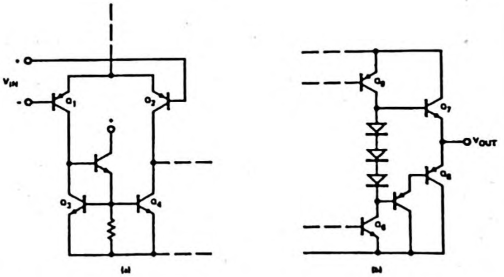


Fig. 2. (a) Modified current mirror used to reduce dc offset caused by base currents in $Q3$ and $Q4$ in Fig. 1. (b) Darlington p-n-p output stage needed to minimize gain fall-off when sinking large output currents. This is needed to offset the rapid β drop which occurs in IC p-n-p's.

The study begins in Section II, with an analysis of dc and low frequency gain. It is shown that the gain is typically limited by thermal feedback rather than elec-

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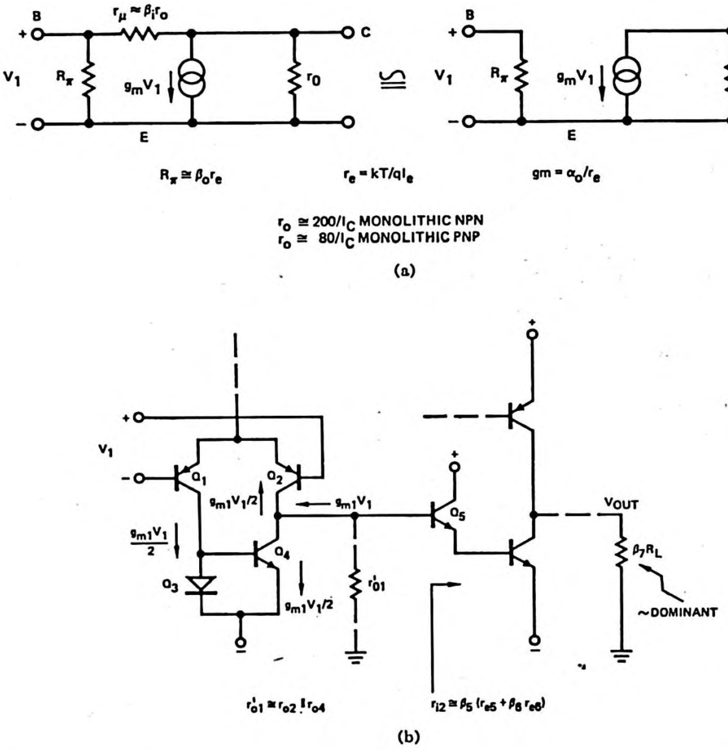

B
$r_\mu \approx \beta_i r_o$
C
+
V_1
R_π
$g_m V_1$
r_o
−
E
≅
B
+
C
V_1
R_π
$g_m V_1$
r_o
−
E
$R_\pi \cong \beta_o r_e$
$r_e = kT/qI_e$
$g_m = \alpha_o/r_e$
$r_o \cong 200/I_C$ MONOLITHIC NPN
$r_o \cong 80/I_C$ MONOLITHIC PNP
(a)
+
+
V_1
−
Q_1
Q_2
$g_{m1}V_1/2$
$g_{m1}V_1$
Q_5
V_{OUT}
$\frac{g_{m1}V_1}{2}$
Q_4
$\beta_7 R_L$
Q_3
r'_{01}
$g_{m1}V_1/2$
~DOMINANT
+
$r'_{01} \cong r_{o2} \| r_{o4}$
$r_{i2} \cong \beta_5 (r_{e5} + \beta_6 r_{e6})$
(b)

Fig. 3. (a) Approximate π model for CE transistor at dc. Feedback element $r_\mu \cong \beta_i r_o$ is ignored since this greatly simplifies hand calculations. The error caused is usually less than 10 percent because β_i, the intrinsic β under the emitter, is quite large. Base resistance r_x is also ignored for simplicity. (b) Circuit illustrating calculation of electronic gain for op amp of Fig. 1. Consideration is given only to the fully loaded condition ($R_L \cong 2$ kΩ) where β_7 is falling (to about 50) due to high current density. Under this condition, the output resistance of $Q6$ and $Q9$ are nondominant.

trical characteristics. A highly simplified thermal analysis is made, resulting in a gain equation containing only the maximum output current of the op amp and a thermal feedback constant.

The next three sections apply first-order models to the calculation of small-signal high frequency and large-signal slewing characteristics. Results obtained include an accurate equation for gain-bandwidth product, a general expression for slew rate, some important relationships between slew rate and bandwidth, and a solution for voltage follower behavior in a slewing mode. Due to the simplicity of the results in these sections, they are very useful to designers in the development of new amplifier circuits.

Section VI applies more accurate models to the calculation of important second-order effects. An effort is made in this section to isolate all of the major contributors to bandlimiting in the modern amp.

In the final section, some techniques for reduction of op amp die size are considered. Transconductance reduction and layout techniques are discussed which lead to fabrication of an extremely compact op amp cell. An example yielding 8000 possible op amps per 3-in wafer is given.

II. GAIN AT DC AND LOW FREQUENCIES

A. The Electronic Gain

The electronic voltage gain will first be calculated at dc using the circuit of Fig. 1. This calculation becomes straightforward if we employ the simplified transistor model shown in Fig. 3(a). The resulting gain from Fig. 3(b) is

$$A_V(0) = \frac{v_{\text{out}}}{v_{\text{in}}} \cong \frac{g_{m1}\beta_5\beta_6\beta_7 R_L}{1 + r_{i2}/r_{01}'}. \tag{1}$$

where

$$r_{i2} \cong \beta_5(r_{e5} + \beta_6 r_{e6})$$

$$r_{o1}' \cong r_{o4}//r_{o2}.$$

It has been assumed that

$$\beta_7 R_L < r_{o6}//r_{o9},\ g_{m1} = g_{m2},\ \beta_7 = \beta_8.$$

The numerical subscripts relate parameters to transistor Q numbers (i.e., r_{e5} is r_e of Q_5, β_6 is β_0 of Q_6, etc.). It has also been assumed that the current mirror transistors Q_3 and Q_4 have α's of unity, and the usually small loading of R_B has been ignored. Despite the several assumptions made in obtaining this simple form for (1), its accuracy is quite adequate for our needs.

An examination of (1) confirms the way in which the amplifier operates: the input pair and current mirror convert the input voltage to a current $g_{m1}v_{in}$ which drives the base of the second stage. Transistors Q_5, Q_6, and Q_7 simply multiply this current by β^3 and supply it to the load R_L. The finite output resistance of the first stage causes some loss when compared with second stage input resistance, as indicated by the term $1/(1 + r_{i2}/r_{01}')$. A numerical example will help our perspective: for the LM101A, $I_1 \cong 10\ \mu A$, $I_2 \cong 300\ \mu A$, $\beta_5 = \beta_6 \cong 150$, and $\beta_7 \cong 50$. From (1) and dc voltage gain with $R_L = 2\ k\Omega$ is

$$A_V(0) \cong 625\,000. \tag{2}$$

The number predicted by (2) agrees well with that measured on a discrete breadboard of the LM101A, but is much higher than that observed on the integrated circuit. The reason for this is explained in the next section.

B. Thermal Feedback Effects on Gain

The typical IC op amp is capable of delivering powers of 50–100 mW to a load. In the process of delivering this power, the output stage of the amp internally dissipates similar power levels, which causes the temperature of the IC chip to rise in proportion to the output dissipated power. The silicon chip and the package to which it is bonded are good thermal conductors, so the whole chip tends to rise to the same temperature as the output stage. Despite this, small temperature gradients from a few tenths to a few degrees centigrade develop across the chip with the output section being hotter than the rest. As illustrated in Fig. 4, these temperature gradients appear across the input components of the op amp and induce an input voltage which is proportional to the output dissipated power.

To a first order, it can be assumed that the temperature difference (T_2-T_1) across a pair of matched and closely spaced components is given simply by

$$(T_2 - T_1) \cong \pm K_T P_d \quad {}^\circ C \tag{3}$$

where

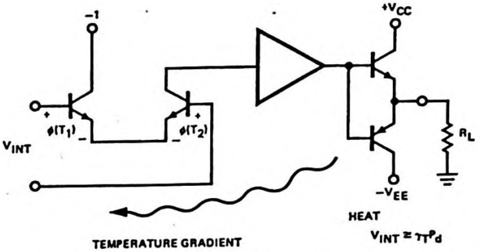


Fig. 4. Simple model illustrating thermal feedback in an IC op amp having a single dominant source of self-heat, the output stage. The constant $\gamma_T \cong 0.6$ mV/W and P_d is power dissipated in the output. For simplicity, we ignore input drift due to uniform heating of the package. This effect can be significant if the input stage drift is not low, see [7].

P_d power dissipated in the output circuit,

K_T a constant with dimensions of °C/W.

The plus/minus sign is needed because the direction of the thermal gradient is unknown. In fact, the sign may reverse polarity during the output swing as the dominant source of heat shifts from one transistor to another. If the dominant input components consist of the differential transistor pair of Fig. 4, the thermally induced input voltage V_{int} can be calculated as

$$V_{int} \cong \pm K_T P_d (2 \times 10^{-3})$$

$$\cong \pm \gamma_T P_d \tag{4}$$

where $\gamma_T = K_T(2 \times 10^{-3})$ V/W, since the transistor emitter-base drops change about -2 mV/°C.

For a thermally well designed IC op amp, in which the power output devices are made to approximate either a point or a line source and the input components are placed on the resulting isothermal lines (see below and Fig. 8), typical values measured for K_T are

$$K_T \approx 0.3\ {}^\circ C/W \tag{5}$$

in a TO-5 package.

The dissipated power in the class-AB output stage P_d is written by inspection of Fig. 4:

$$P_d = \frac{V_0 V_s - V_0^2}{R_L} \tag{6}$$

where

$$V_s = +V_{cc} \qquad \text{when } V_0 > 0$$

$$V_s = -V_{cc} \qquad \text{when } V_0 < 0.$$

A plot of (6) in Fig. 5 resembles the well-known class-AB dissipation characteristics, with zero dissipation occurring for $V_0 = 0$, $+V_{cc}$, $-V_{cc}$. Dissipation peaks occur for $V_0 = +V_{cc}/2$ and $-V_{cc}/2$. Note also from (4) that the thermally induced input voltage V_{int} has this same double-humped shape since it is just equal to a constant times P_d at dc.

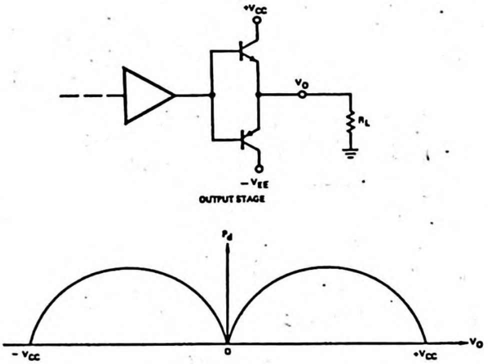
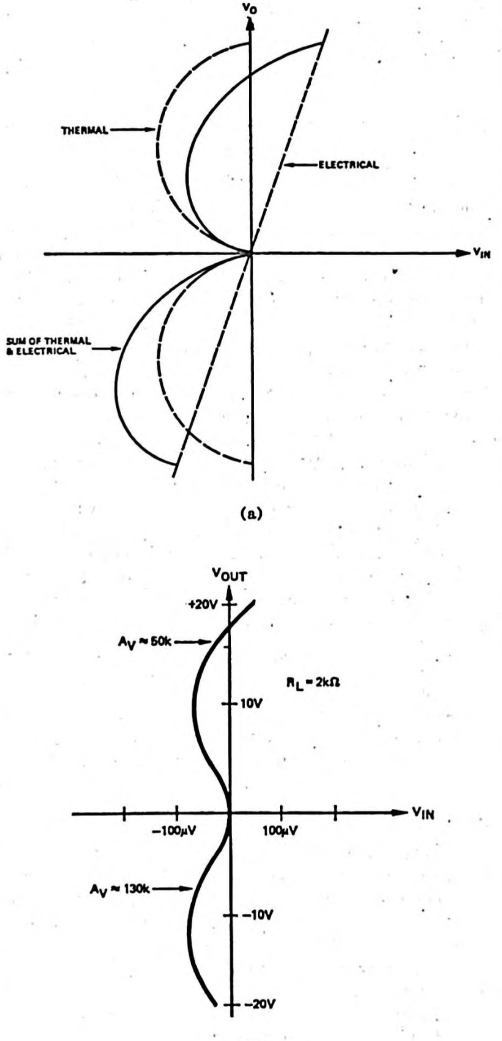


Fig. 5. Simple class-B output stage and plot of power dissipated in the stage, P_d, assuming device can swing to the power supplies. Equation (6) gives an expression for the plot.



(a)

(b)

Fig. 6. (a) Idealized dc transfer curve for an IC op amp showing its electrical and thermal components. (b) Experimental open-loop transfer curve for a representative op amp (LM 101).

Now examine Figs. 6(a) and (b) which are curves of open-loop V_o versus V_{in} for the IC op amp. Note first that the overall curve can be visualized to be made up of two components: a) a normal straight line electrical gain curve of the sort expected from (1) and b) a double-humped curve similar to that of Fig. 5. Further, note that the gain characteristic has either positive or negative slope depending on the value of output voltage. This means that the thermal feedback causes the open-loop gain of the feedback amplifier to change phase by 180°, apparently causing negative feedback to become positive feedback. If this is really true, the question arises: which input should be used as the inverting one for feedback? Further, is there any way to close the amplifier and be sure it will not find an unstable operating point and latch to one of the power supplies?

The answers to these questions can be found by studying a simple model of the op amp under closed-loop conditions, including the effects of thermal coupling. As shown in Fig. 7, the thermal coupling can be visualized as just an additional feedback path which acts in parallel with the normal electrical feedback. Noting that the electrical form of the thermal feedback factor is [see (4) and (6)]

$$\beta_T = \frac{\partial V_{\rm int}}{\partial V_o} = \pm\frac{\gamma_T}{R_L}(V_s - 2V_o). \qquad (7)$$

The closed-loop gain, including thermal feedback is

$$A_V(0) = \frac{\mu}{1 + \mu(\beta_e \pm \beta_T)} \qquad (8)$$

where μ is the open-loop gain in the absence of thermal feedback [(1)] and β_e is the applied electrical feedback as in Fig. 7. Inspection of (8) confirms that as long as there is sufficient electrical feedback to swamp the thermal feedback (i.e., $\beta_e > \beta_T$), the amplifier will behave as a normal closed-loop device with characteristics determined principally by the electrical feedback (i.e., $A_V(0) \cong 1/\beta_e$). On the other hand, if β_e is small or nonexistant, the thermal term in (8) may dominate, giving an apparent open-loop gain characteristic determined by the thermal feedback factor β_T. Letting $\beta_e = 0$ and combining (7) and (8), $A_V(0)$ becomes

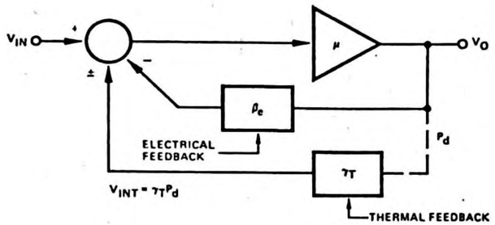


Fig. 7. Diagram used to calculate closed-loop gain with thermal feedback.

$$A_V(0) = \frac{\mu}{1 \pm \frac{\mu\gamma_T}{R_L}(V_S - 2V_o)}. \tag{9}$$

Recalling from (6) that V_0 ranges between 0 and V_S, we note that the incremental thermal feedback is greatest when $V_0 = 0$ or V_s, and it is at these points that the thermally limited gain is smallest. To use the amplifier in a predictable manner, one must always apply enough electrical feedback to reduce the gain below this minimum thermal gain. Thus, a *maximum usable gain* can be defined as that approximately equal to the value of (9) with $V_0 = 0$ or V_s which is

$$A_V(0)|_{\max} \cong \frac{R_L}{\gamma_T V_S} \tag{10}$$

or

$$A_V(0)|_{\max} \cong \frac{1}{\gamma_T I_{\max}}. \tag{11}$$

It was assumed in (10) and (11) that thermal feedback dominates over the open-loop electrical gain, μ. Finally, in (11) a maximum current was defined $I_{\max} = V_S/R_L$ as the maximum current which would flow if the amplifier output could swing all the way to the supplies.

Equation (11) is a strikingly simple and quite general result which can be used to predict the expected maximum usable gain for an amplifier if we know only the maximum output current and the thermal feedback constant γ_T.

Recall that typically $K_T \cong 0.3°\text{C/W}$ and $\gamma_T = (2 \times 10^{-3})\ K_T \cong 0.6\ \text{mV/W}$. Consider, as as example, the standard IC op amp operating with power supplies of $V_S = \pm 15$ V and a minimum load of 2 kΩ, which gives $I_{\max} = 15\ \text{V}/2\ \text{k}\Omega = 7.5$ mA. Then, from (11), the maximum thermally limited gain is about:

$$A_V(0)|_{\max} \cong 1/(0.6 \times 10^{-3})(7.5 \times 10^{-3})$$

$$\cong 220\,000. \tag{12}$$

Comparing (2) and (12), it is apparent that the thermal characteristics dominate over the electrical ones if the minimum load resistor is used. For loads of 6 kΩ or more, the electrical characteristics should begin to dominate if thermal feedback from sources other than the output stage is negligible. It should be noted also that, in some high speed, high drain op amps, thermal feedback from the second stage dominates when there is no load.

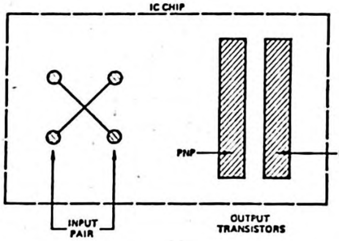


Fig. 8. One type layout in which a quad of input transistors is cross connected to reduce effect of nonuniform thermal gradients. The output transistors use distributed stripe geometries to generate predictable isothermal lines.

As a second example, consider the so-called "power op amp" or high gain audio amp which suffers from the same thermal limitations just discussed. For a device which can deliver 1 W into a 16-Ω load, the peak output current and voltage are 350 mA and 5.7 V. Typically, a supply voltage of about 16 V is needed to allow for the swing loss in the IC output stage. $I_{\max}$ is then 8 V/16 Ω or 0.5 A. If the device is in a TO-5 package γ_T is approximately 0.6 mV/W, so from (11) the maximum usable dc gain is

$$A_V(0)|_{\max} \cong \frac{1}{(0.6 \times 10^{-3})(0.5)} \cong 3300. \tag{13}$$

This is quite low compared with electrical gains of, say, 100 000 which are easily obtainable. The situation can be improved considerably by using a large die to separate the power devices from the inputs and carefully placing the inputs on constant temperature (isothermal) lines as illustrated in Fig. 8. If one also uses a power package with a heavy copper base, γ_T's as low as 50 μV/W have been observed. For example, a well-designed 5-W amplifier driving an 8-Ω load and using a 24-V supply, would have a maximum gain of 13 000 in such a power package.

As a final comment, it should be pointed out that the most commonly observed effect of thermal feedback in high gain circuits is low frequency distortion due to the nonlinear transfer characteristic. Differential thermal coupling typically falls off at an initial rate of 6 dB/octave starting around 100–200 Hz, so higher frequencies are uneffected.

III. Small-Signal Frequency Response

At higher frequencies where thermal effects can be ignored, the behavior of the op amp is dependent on purely electronic phenomena. Most of the important small and large signal performance characteristics of the classical IC op amp can be accurately predicted from

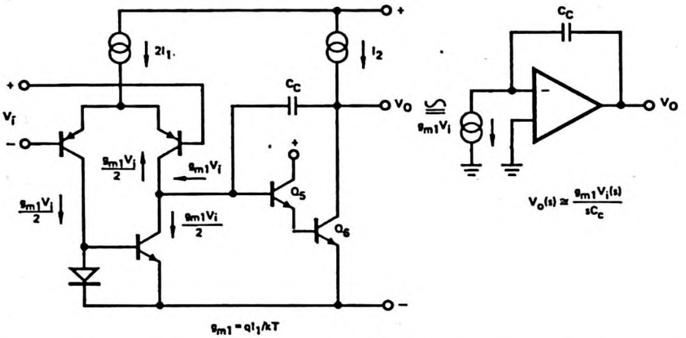


Fig. 9. First-order model of op amp used to calculate small signal high frequency gain. At frequencies of interest the input impedance of the second stage becomes low compared to first stage output impedance due to C_c feedback. Because of this, first stage output impedance can be assumed infinite, with no loss in accuracy.

very simple first-order models for the amplifier in Fig. 1[8]. The small-signal model that is used assumes that the input differential amplifier and current mirror can be replaced by a frequency independent voltage controlled current source, see Fig. 9. The second stage consisting essentially of transistors Q_5 and Q_6, and the current source load, is modeled as an ideal frequency independent amplifier block with a feedback or "integrating capacitor" identical to the compensation capacitor, C_c. The output stage is assumed to have unity voltage gain and is ignored in our calculations. From Fig. 9, the high frequency gain is calculated by inspection:

$$A_v(\omega) = \left|\frac{v_0}{v_i}(s)\right| = \left|\frac{g_{m1}}{sC_c}\right| = \frac{g_{m1}}{\omega C_c} \tag{14}$$

where dc and low frequency behavior have not been included since this was evaluated in the last section. Fig. 10 is a plot of the gain magnitude as predicted by (14). From this figure it is a simple matter to calculate the open-loop unity gain frequency ω_u, which is also the gain-bandwidth product for the op amp under closed-loop conditions:

$$\omega_u = \frac{g_{m1}}{C_c}. \tag{15}$$

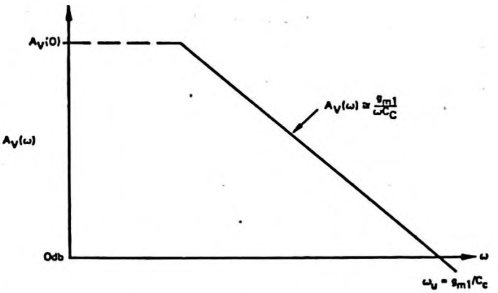


Fig. 10. Plot of open-loop gain calculated from model in Fig. 9. The dc and LF gain are given by (1), or (11) if thermal feedback dominates.

In a practical amplifier, ω_u is set to a low enough frequency (by choosing a large C_c) so that negligible excess phase over the 90° due to C_c has built up. There are numerous contributors to excess phase including low f_t p-n-p's, stray capacitances, nondominant second stage poles, etc. These are discussed in more detail in a later section, but for now suffice it to say that, in the simple IC op amp, $\omega_u/2\pi$ is limited to about 1 MHz. As a simple test of (15), the LM101 or the μA741 has a first stage bias current I_1 of 10 μA per side, and a compensation capacitor for unity gain operation, C_c, of 30 pF. These amplifiers each have a first stage g_m which is half that of the simple differential amplifier in Fig. 1 so $g_{m1} = qI_1/2kT$. Equation (15) then predicts a unity gain corner of

$$f_u = \frac{\omega_u}{2\pi} = \frac{g_{m1}}{2\pi C_c} = \frac{(0.192 \times 10^{-3})}{2\pi(30 \times 10^{-12})} = 1.02 \text{ MHz} \tag{16}$$

which agrees closely with the measured values.

IV. SLEW RATE AND SOME SPECIAL LIMITS

A. A General Limit on Slew Rate

If an op amp is overdriven by a large-signal pulse or square wave having a fast enough rise time, the output does not follow the input immediately. Instead, it ramps or "slews" at some limiting rate determined by internal currents and capacitances, as illustrated in Fig. 11. The magnitude of input voltage required to make the amplifier reach its maximum slew rate varies, depending on the type of input stage used. For an op amp with a

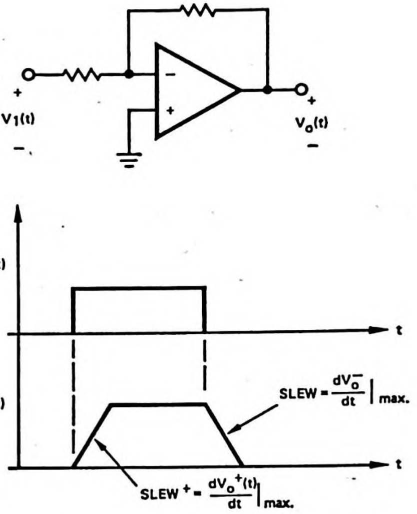


Fig. 11. Large signal "slewing" response observed if the input is overdriven.

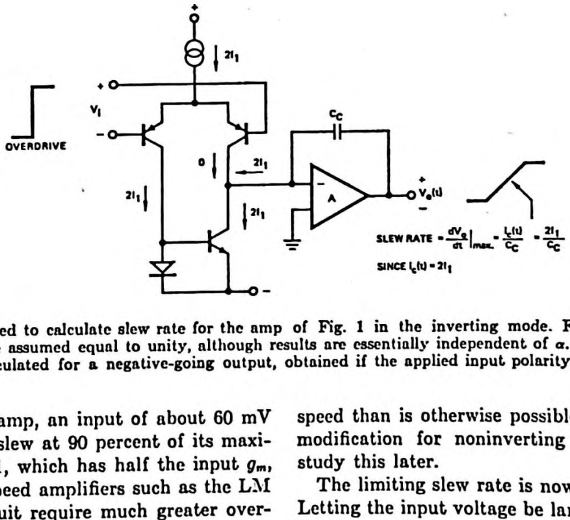


Fig. 12. Model used to calculate slew rate for the amp of Fig. 1 in the inverting mode. For simplicity, all transistor α's are assumed equal to unity, although results are essentially independent of α. An identical slew rate can be calculated for a negative-going output, obtained if the applied input polarity is reversed.

simple input differential amp, an input of about 60 mV will cause the output to slew at 90 percent of its maximum rate, while a μA741, which has half the input g_m, requires 120 mV. High speed amplifiers such as the LM 118 or a FET-input circuit require much greater overdrive, with 1–3 V being common. The reasons for these overdrive requirements will become clear below.

An adequate model to calculate slew limits for the representative op amp in the inverting mode is shown in Fig. 12, where the only important assumption made is that $I_2 \geq 2I_1$ in Fig. 1. This condition always holds in a well-designed op amp. (If one lets I_2 be less than $2I_1$, the slew is limited by I_2 rather than I_1, which results in lower speed than is otherwise possible.) Fig. 12 requires some modification for noninverting operation, and we will study this later.

The limiting slew rate is now calculated from Fig. 12. Letting the input voltage be large enough to fully switch the input differential amp, we see that all of the first stage tail current $2I_1$ is simply diverted into the integrator consisting of A and C_c. The resulting slew rate is then:

$$\text{slew rate} = \left.\frac{dv_0}{dt}\right|_{\max} = \frac{i_c(t)}{C_c}. \tag{17}$$

Noting that $i_c(t)$ is a constant $2I_1$, this becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2I_1}{C_c}. \tag{18}$$

As a check of this result, recall that the μA741 has $I_1 = 10\ \mu\text{A}$ and $C_1 = 30$ pF, so we calculate:

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2\times 10^{-5}}{30\times 10^{-12}} = 0.67\,\frac{\text{V}}{\mu\text{s}} \tag{19}$$

which agrees with measured values.

The large and small signal behavior of the op amp can be usefully related by combining (15) for ω_u with (18). The slew rate becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2\omega_u I_1}{g_{m1}}. \tag{20}$$

Equation (20) is a general and very useful relationship. It shows that, for a given unity-gain frequency, ω_u, the slew rate is determined entirely by just the ratio of first stage operating current to first stage transconductance, I_1/g_{m1}. Recall that ω_u is set at the point where excess phase begins to build up, and this point is determined largely by technology rather than circuit limitations. Thus, the only effective means available to the circuit designer for increasing op amp slew rate is to *decrease* the ratio of first stage transconductance to operating current, g_{m1}/I_1.

B. Slew Limiting for Simple Bipolar Input Stage

The significance of (20) is best seen by considering the specific case of a simple differential bipolar input as in Fig. 1. For this circuit, the first stage transconductance (for $\alpha_1 = 1$) is[1]

$$g_{m1} = qI_1/kT \tag{21}$$

so that

$$\frac{g_{m1}}{I_1} = q/kT. \tag{22}$$

Using this in (20), the maximum bipolar slew rate is

$$\left.\frac{dv_0}{dt}\right|_{\max} = 2\omega_u\frac{kT}{q}. \tag{23}$$

This provides us with the general (and somewhat dismal) conclusion that slew rate in an op amp with a simple bipolar input stage is dependent only upon the unity gain corner and fundamental constants. Slew rate can be increased only by increasing the unity gain corner, which we have noted is generally difficult to do. As a demonstration of the severity of this limit, imagine an op amp using highly advanced technology and clever design, which might have a stable unity gain frequency of 100 MHz. Equation (23) predicts that the slew rate for this advanced device is only

$$\left.\frac{dv_0}{dt}\right|_{\max} = 33\,\frac{\text{V}}{\mu\text{s}} \tag{24}$$

which is good, but hardly impressive when compared with the difficulty of building a 100-MHz op amp.[2] But, there are some ways to get around this limit as we shall see shortly.

C. Power Bandwidth

Our intuition regarding slew rate will be enhanced somewhat if we relate it to a term called "power bandwidth." Power bandwidth is defined as the maximum frequency at which full output swing (usually 10 V peak) can be obtained without distortion. For a sinusoidal output voltage $v_0(t) = V_p \sin \omega t$, the rate of change of output, or slew rate, required to reproduce the output is

$$\frac{dv_0}{dt} = \omega V_p \cos \omega t. \tag{25}$$

This has a maximum when $\cos \omega t = 1$ giving

$$\left.\frac{dv_0}{dt}\right|_{\max} = \omega V_p, \tag{26}$$

so the highest frequency that can be reproduced without slew limiting, $\omega_{\max}$ (power bandwidth) is

$$\omega_{\max} = \frac{1}{V_p}\left.\frac{dv_0}{dt}\right|_{\max}. \tag{27}$$

Thus, power bandwidth and slew rate are directly related by the inverse of the peak of the sine wave V_p. Fig. 13 shows the severe distortion of the output sine wave which results if one attempts to amplify a sine wave of frequency $\omega > \omega_{\max}$.

Some numbers illustrate typical op amp limits. For a μA741 or LM101 having a maximum slew rate of 0.67 V/μs, (27) gives a maximum frequency for an undistorted 10-V peak output of

$$f_{\max} = \frac{\omega_{\max}}{2\pi} = 10.7\ \text{kHz}, \tag{28}$$

which is a quite modest frequency considering the much higher frequency small signal capabilities of these devices. Even the highly advanced 100-MHz amplifier considered above has a 10-V power bandwidth of only 0.5 MHz, so it is apparent that a need exists for finding ways to improve slew rate.

D. Techniques for Increasing Slew Rate

1) Resistive Enhancement of the Bipolar Stage: Equation (20) indicates that slew rate can be improved if we reduce first stage g_{m1}/I_1. One of the most effective ways

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[1] Note that (21) applies only to the simple differential input stage of Fig. 12. For compound input stages as in the LM101 or μA741, g_{m1} is half that in (21), and the slew rate in (23) is doubled.

[2] We assume in all of these calculations that C_c is made large enough so that the amplifier has less than 180° phase lag at ω_u, thus making the amplifier stable for unity closed-loop gain. For higher gains one can of course reduce C_c (if the IC allows external compensation) and increase the slew rate according to (18).

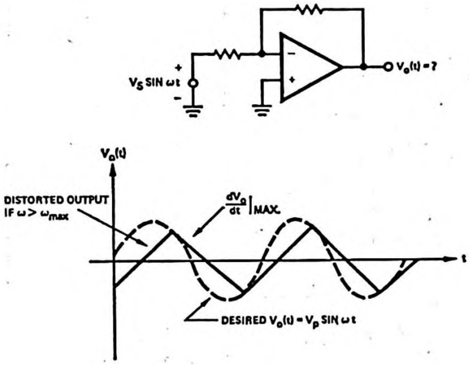

+
V_S SIN ωt
-
$V_o(t)$ = ?
$V_o(t)$
DISTORTED OUTPUT IF ω > ω_{max}
$\frac{dV_o}{dt}\big|_{MAX}$
t
DESIRED $V_o(t) = V_p$ SIN ωt

Fig. 13. Slew limiting effects on output sinewave that occur if frequency is greater than power bandwidth, ω_{max}. The onset of slew limiting occurs very suddenly as ω reaches ω_{max}. No distortion occurs below ω_{max}, while almost complete triangularization occurs at frequencies just slightly above ω_{max}.

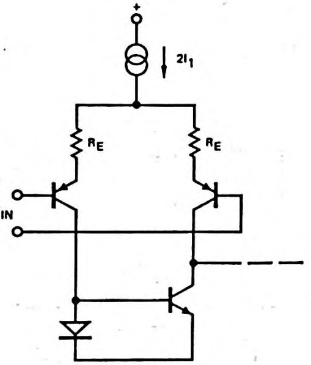


Fig. 14. Resistive degeneration used to provide slew rate enhancement according to (29).

of doing this is shown in Fig. 14, where simple resistive emitter degeneration has been added to the input differential amplifier [8]. With this change, the g_{m1}/I_1 drops to

$$\frac{g_{m1}}{I_1} = \frac{38.5}{1 + R_E I_1/26\text{ mV}} \tag{29}$$

at 25°C.

The quantity g_{m1}/I_1 is seen to decrease rapidly with added R_E as soon as the voltage drop across R_E exceeds 26 mV. The LM118 is a good example of a bipolar amplifier which uses emitter degeneration to enhance slew rate [4]. This device uses emitter resistors to produce $R_E I_1 = 500$ mV, and has a unity gain corner of 16 MHz. Equations (20) and (29) then predict a maximum inverting slew rate of

$$\left.\frac{dv_0}{dt}\right|_{\max} = 2\omega_u \frac{I_1}{g_{m1}} = \omega_u = 100\,\frac{\text{V}}{\mu\text{s}} \tag{30}$$

which is a twenty-fold improvement over a similar amplifier without emitter resistors.

A penalty is paid in using resistive slew enhancement, however. The two added emitter resistors must match extremely well or they add voltage offset and drift to the input. In the LM118, for example, the added emitter R's have values of 2.0 kΩ each and these contribute an input offset of 1 mV for each 4 Ω (0.2 percent) of mismatch. The thermal noise of the resistors also unavoidably degrades noise performance.

2) Slew Rate in the FET Input Op Amp: The FET (JFET or MOSFET) has a considerably lower transconductance than a bipolar device operating at the same current. While this is normally considered a drawback of the FET, we note that this "poor" behavior is in fact highly desirable in applications to fast amplifiers. To illustrate, the drain current for a JFET in the "current saturation" region can be approximated by

$$I_D \cong I_{DSS}(V_{GS}/V_T - 1)^2 \tag{31}$$

where

I_{DSS} the drain current for $V_{GS} = 0$,
V_{GS} the gate source voltage having positive polarity for forward gate-diode bias,
V_T the threshold voltage having negative polarity for JFET's.

The small-signal transconductance is obtained from (31) as $g_m = \partial I_D/\partial V_G$. Dividing by I_D and simplifying, the ratio g_m/I_D for a JFET is

$$\frac{g_m}{I_D} \cong \frac{2}{(V_{GS} - V_T)} = \frac{2}{-V_T}\left[\frac{I_{DSS}}{I_D}\right]^{1/2}. \tag{32}$$

Maximum amplifier slew rate occurs for minimum g_m/I_D and, from (32), this occurs when I_D (or V_{GS}) is maximum. Normally it is impractical to forward bias the gate junction so a practical minimum occurs for (32) when $V_{GS} \cong 0$ V and $I_D \cong I_{DSS}$. Then

$$\left.\frac{g_m}{I_D}\right|_{\min} \cong -\frac{2}{V_T}. \tag{33}$$

Comparing (33) with the analogous bipolar expression, (22), we find from (20) that the JFET slew rate is greater than bipolar by the factor

$$\frac{\text{JFET slew}}{\text{bipolar slew}} \approx \frac{-V_T}{2kT/q}\,\frac{\omega_{uf}}{\omega_{ub}} \tag{34}$$

where ω_{uf} and ω_{ub} are unity-gain bandwidths for JFET and bipolar amps, respectively. Typical JFET thresholds are around 2 V ($V_T = -2$ V), so for equal bandwidths (34) tells us that a JFET-input op amp is about forty times faster than a simple bipolar input. Further, if

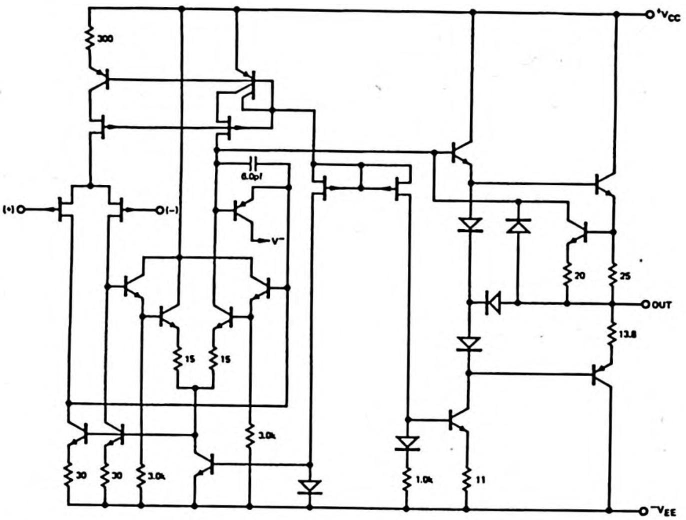


Fig. 15. Monolithic operational amplifier employing compatible p-channel JFET's on the same chip with normal bipolar components.

JFET's are properly substituted for the slow p-n-p's in a monolithic design, bandwidth improvements by at least a factor of ten are obtainable. JFET-input op amps, therefore, offer slew rate improvements by better than two orders of magnitude when compared with the conventional IC op amp. (Similar improvements are possible with MOSFET-input amplifiers.) This characteristic, coupled with picoamp input currents and reasonable offset and drift, make the JFET-input op amp a very desirable alternative to conventional bipolar designs.

As an example, Fig. 15, illustrates one design for an op amp employing compatible p-channel JFET's on the same chip with the normal bipolar components. This circuit exhibits a unity gain corner of 10 MHz, a 33 V/μs slew rate, an input current of 10 pA and an offset voltage and drift of 3 mV and 3 μV/°C [6]. Bandwidth and slew rate are thus improved over simple IC bipolar by factors of 10 and 100, respectively. At the same time input currents are smaller by about 10^3, and offset voltages and drifts are comparable to or better than slew enhanced bipolar circuits.

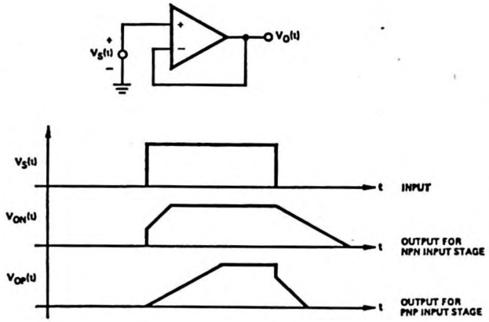


Fig. 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{on}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

V. Second-Order Effects: Voltage Follower Slew Behavior

If the op amp is operated in the noninverting mode and driven by a large fast rising input, the output exhibits the characteristic waveform in Fig. 16. As shown, this waveform does not have the simple symmetrical slew characteristic of the inverter. In one direction, the output has a fast step (slew "enhancement") followed by a "normal" inverter slewing response. In the other direction, it suffers a slew "degradation" or reduced slope when compared with the inverter slewing response.

We will first study slew degradation in the voltage follower connection, since this represents a worst case slewing condition for the op amp. A model which adequately represents the follower under large-signal conditions can be obtained from that in Fig. 12 by simply

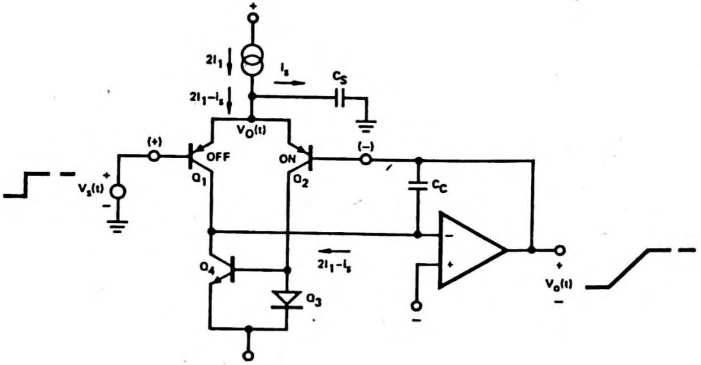


Fig. 17. Circuit used for calculation of slew "degradation" in the voltage follower. The degradation is caused by the capacitor C_s, which robs current from the tail, $2I_1$, thereby preventing the full $2I_1$ from slewing C_c.

tying the output to the inverting input, and including a capacitor C_s to account for the presence of any capacitance at the output of the first stage (tail) current source, see Fig. 17. This "input tail" capacitance is important in the voltage follower because the input stage undergoes rapid large-signal excursions in this connection, and the charging currents in C_s can be quite large.

Circuit behavior can be understood by analyzing Fig. 17 as follows. The large-signal input step causes Q_1 to turn OFF, leaving Q_2 to operate as an emitter follower with its emitter tracking the variational output voltage, $v_O(t)$. It is seen that $v_O(t)$ is essentially the voltage appearing across both C_s and C_c so we can write

$$\frac{dv_O}{dt} \cong \frac{i_c}{C_c} \cong \frac{i_s}{C_s}. \tag{35}$$

Noting that $i_c \cong 2I_1 - i_s$ (unity α's assumed), (35) can be solved for i_s:

$$i_s \cong \frac{2I_1}{1 + C_c/C_s} \tag{36}$$

which is seen to be constant with time. The degraded voltage follower slew rate is then obtained by substituting (36) into (35):

$$\left.\frac{dv_O}{dt}\right|_{\text{degr}} \cong \frac{i_s}{C_s} \cong \frac{2I_1}{C_c + C_s}. \tag{37}$$

Comparing (37) with the slew rate for the inverter, (18), it is seen that the slew rate is reduced by the simple factor $1/(1 + C_s/C_c)$. As long as the input tail capacitance C_s is small compared with the compensation capacitor C_c, little degradation occurs. In high speed amplifiers where C_c is small, degradation becomes quite noticeable, and one is encouraged to develop circuits with small C_s.

As an example, consider the relatively fast LM118 which has $C_c \cong 5$ pF, $C_s \cong 2$ pF, $2I_1 = 500$ µA. The calculated inverter slew rate is $2I_1/C_c \cong 100$ V/µs, and the degraded voltage follower slew rate is found to be $2I_1/(C_c + C_s) \cong 70$ V/µs. The slew degradation is seen to be about 30 percent, which is very significant. By contrast, a µA741 has $C_c \cong 30$ pF and $C_s \cong 4$ pF which results in a degradation of less than 12 percent.

The slew "enhanced" waveform can be similarly predicted from a simplified model. By reversing the polarity of the input and initially assuming a finite slope on the input step, the enhanced follower is analyzed, as shown in Fig. 18. Noting that Q_1 is assumed to be turned ON by the step input and Q_2 is OFF, the output voltage becomes

$$v_O(t) \cong -\frac{1}{C_c}\int_0^t [2I_1 + i_S(t)]\, dt. \tag{38}$$

The voltage at the emitter of Q_1 is essentially the same as the input voltage, $v_i(t)$, so the current in the "tail" capacitance C_s is

$$i_s(t) \cong C_s \frac{dv_i}{dt} \cong \frac{C_s V_{ip}}{t_1} \qquad 0 < t < t_1. \tag{39}$$

Combining (38) and (39), $v_O(t)$ is

$$-v_O(t) \cong \frac{1}{C_c}\int_0^t 2I_1\, dt + \frac{1}{C_c}\int_0^{t_1} \frac{C_s V_{ip}}{t_1}\, dt \tag{40}$$

or

$$-v_O(t) \cong \frac{C_s}{C_c} V_{ip} + \frac{2I_1 t}{C_c}. \tag{41}$$

Equation (41) tells us that the output has an initial negative step which is the fraction C_s/C_c of the input voltage. This is followed by a normal slewing response, in which the slew rate is identical to that of the inverter, see (18). This response is illustrated in Fig. 18.

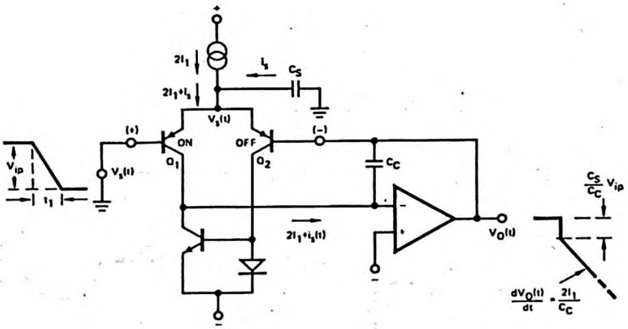


Fig. 18. Circuit used for calculation of slew "enhancement" in the voltage follower. The fast falling input causes a step output followed by a normal slew response as shown.

VI. Limitations on Bandwidth

In earlier sections, all bandlimiting effects were ignored except that of the compensation capacitor, C_c. The unity-gain frequency was set at a point sufficiently low so that negligible excess phase (over the 90° from the dominant pole) due to second-order (high frequency) poles had built up. In this section the major second-order poles which contribute to bandlimiting in the op amp are identified.

A. The Input Stage: p-n-p's, the Mirror Pole, and the Tail Pole

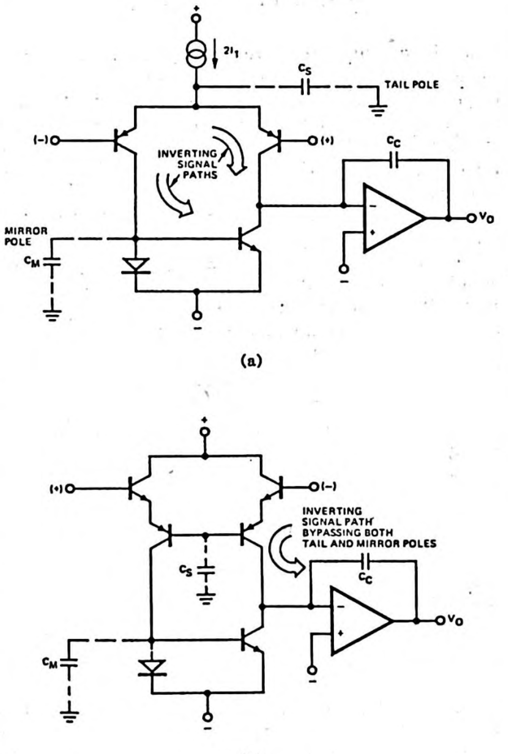
For many years it was popular to identify the lateral p-n-p's (which have f_t's ≅ 3 MHz) as the single dominant source of bandlimiting in the IC op amp. It is quite true that the p-n-p's do contribute significant excess phase to the amplifier, but it is not true that they are the sole contributor to excess phase [9]. In the input stage, alone, there is at least one other important pole, as illustrated in Fig. 19(a). For the simple differential input stage driving a differential-to-single ended converter ("mirror" circuit), it is seen that the inverting signal (which is the feedback signal) follows two paths, one of which passes through the capacitance C_s, and the other through C_m. These capacitances combine with the dynamic resistances at their nodes to form poles designated the mirror pole at

$$p_m \cong \frac{I_1}{C_m kT/q}, \tag{42}$$

and the tail pole at

$$p_t \cong \frac{2I_1}{C_s kT/q}. \tag{43}$$

It can be seen that if one attempts to operate the first stage at too low a current, these poles will bandlimit the amplifier. If, for example, we choose $I_1 = 1\ \mu$A, and assume $C_m \cong 7$ pF (consisting of 4-pF isolation ca-



(a)

(b)

Fig. 19. (a) Circuit showing "mirror" pole due to C_m and "tail" pole due to C_s. One component of the signal due to an inverting input must pass through either the mirror or tail poles. (b) Alternate circuit to Fig. 19(a) (LM101, μA741) which has less excess phase. Reason is that half the inverting signal path need not pass through the mirror pole or the tail pole.

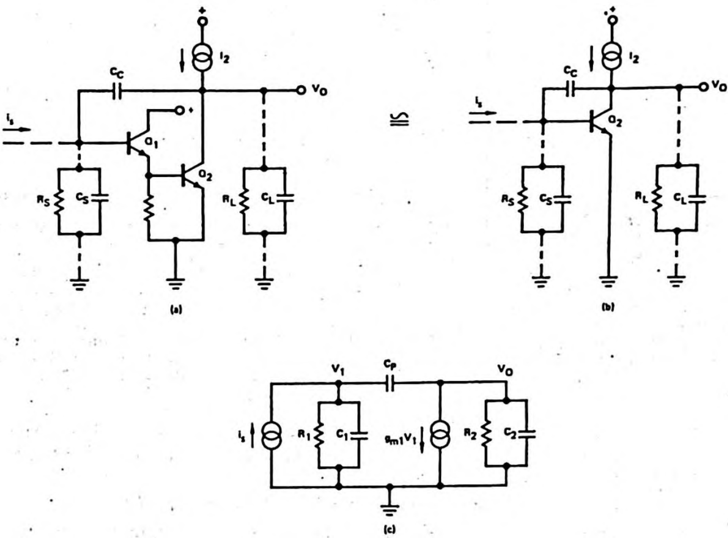


Fig. 20. Simplification of second stage used for pole-splitting analysis. (a) Complete second stage with input stage and output stage loading represented by R_s, C_s, and R_L, C_L, respectively. (b) Emitter follower ignored to simplify analysis. (c) Hybrid π model substituted for transistor in (b). Source and load impedances are absorbed into model with the total impedances represented by R_1, C_1, and R_2, C_2. Transistor base resistance is ignored and C_p includes both C_c and transistor collector-base capacitance.

pacitance and 3-pF emitter transition capacitance) and $C_s \cong 4$ pF,[3] $p_m/2\pi \cong 0.9$ MHz and $p_t/2\pi \cong 3$ MHz either of which would seriously degrade the phase margin of a 1-MHz amplifier.

If a design is chosen in which either the tail pole or the mirror pole is absent (or unimportant), the remaining pole rolls off only half the signal, so the overall response contains a pole-zero pair separated by one octave. Such a pair generally has a small effect on amplifier response unless it occurs near ω_u, where it can degrade phase margin by as much as 20°.

It is interesting to note that the compound input stage of the classical LM101 (and μA741) has a distinct advantage over the simple differential stage, as seen in Fig. 19(b). This circuit is noninverting across each half, thus it provides a path in which half the feedback signal bypasses both the mirror and tail poles.

B. *The Second Stage: Pole Splitting*

The assumption was made in Section III that the second stage behaved as an ideal integrator having a single dominant pole response. In practice, one must take care in designing the second stage or second-order poles can cause significant deviation from the expected response. Considerable insight into the basic way in which the second stage operates can be obtained by performing a small-signal analysis on a simplified version of the circuit as shown in Fig. 20 [10]. A straightforward two-node analysis of Fig. 20(c) produces the following expression for v_{out}.

$$\frac{v_{\text{out}}}{i_s} = \frac{-g_m R_1 R_2 (1 - sC_p/g_m)}{1 + s[R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_m R_1 R_2 C_p] + s^2 R_1 R_2 [C_1 C_2 + C_p(C_1 + C_2)]}. \tag{44}$$

The denominator of (44) can be approximately factored under conditions that its two poles are widely separated. Fortunately, the poles are, in fact, widely separated under most normal operating conditions. Therefore, one can assume that the denominator of (44) has the form

$$\begin{aligned} D(s) &= (1 + s/p_1)(1 + s/p_2) \\ &= 1 + s(1/p_1 + 1/p_2) + s^2/p_1 p_2. \end{aligned} \tag{45}$$

With the assumption that p_1 is the dominant pole and

---

[3] C_s can have a wide range of values depending on circuit configuration. It is largest for n-p-n input differential amps since the current source has a collector-substrate capacitance ($C_s \cong$ 3–4 pF) at its output. For p-n-p input stages it can be as small as 1–2 pF.

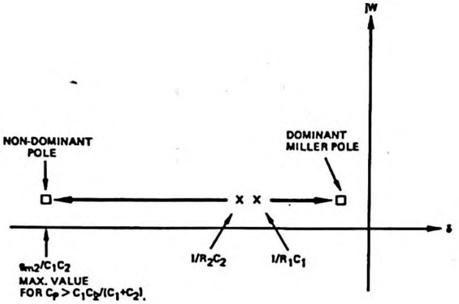


Fig. 21. Pole migration for second stage employing "pole-splitting" compensation. Plot is shown for increasing C_p and it is noted that the nondominant pole reaches a maximum value for large C_p.

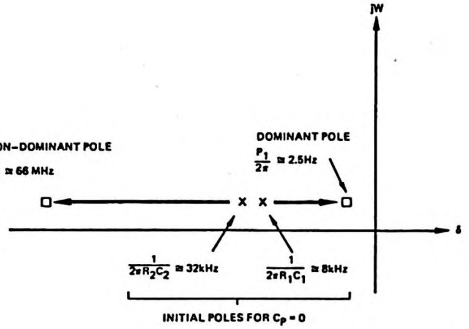

jw
NON-DOMINANT POLE
$\frac{P_2}{2\pi} \cong 66$ MHz
DOMINANT POLE
$\frac{P_1}{2\pi} \cong 2.5$Hz
s
$\frac{1}{2\pi R_2C_2} \cong 32$kHz
$\frac{1}{2\pi R_1C_1} \cong 8$kHz
INITIAL POLES FOR $C_p = 0$

Fig. 22. Example of pole-splitting compensation in the μA741 op amp. Values used in (48) and (49) are: $g_{m2} = 1/87\ \Omega$, $C_p = 30$ pF, $C_1 \cong C_2 = 10$ pF, $R_1 = 1.7$ MΩ, $R_2 = 100$ kΩ.

p_2 is nondominant, i.e., $p_1 \ll p_2$, (45) becomes

$$D(s) \cong 1 + s/p_1 + s^2/p_1p_2. \tag{46}$$

Equating coefficients of s in (44) and (46), the dominant pole p_1 is found directly:

$$p_1 \cong \frac{1}{R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_mR_1R_2C_p} \tag{47}$$

$$\cong \frac{1}{g_mR_1R_2C_p}. \tag{48}$$

The latter approximation, (48), normally introduces little error, because the g_m term is much larger than the other two. We note at this point that p_1, which represents the dominant pole of the amplifier, is due simply to the familiar Miller-multiplied feedback capacitance $g_mR_2C_p$ combined with input node resistance, R_1. The nondominant pole p_2 is found similarly by equating s^2 coefficients in (44) and (46) to get p_1p_2, and dividing by p_1 from (48). The result is

$$p_2 \cong \frac{g_mC_p}{C_1C_2 + C_p(C_1 + C_2)}. \tag{49}$$

Several interesting things can be seen in examining (48) and (49). First, we note that p_1 is inversely proportional to g_m (and C_p), while p_2 is directly dependent on g_m (and C_p). Thus, as either C_p or transistor gain are increased, the dominant pole decreases and the nondominant pole increases. The poles p_1 and p_2 are being "split-apart" by the increased coupling action in a kind of inverse root locus plot.

This *pole-splitting* action is shown in Fig. 21, where pole migration is plotted for C_p increasing from 0 to a large value. Fig. 22 further illustrates the action by giving specific pole positions for the μA741 op amp. It is seen that the initial poles (for $C_p = 0$) are both in the tens of kilohertz region and these are predicted to reach 2.5 Hz ($p_1/2\pi$) and 66 MHz ($p_2/2\pi$) after compensation is applied. This result is, of course, highly satisfactory since the second stage now has a single dominant pole effective over a wide frequency band.

C. Failure of Pole Splitting

There are several situations in which the application of pole-splitting compensation may not result in a single dominant pole response. One common case occurs in very wide-band op amps where the pole-splitting capacitor is small. In this situation the nondominant pole given by (49) may not become broadbanded sufficiently so that it can be ignored. To illustrate, suppose we attempt to minimize power dissipation by running the second stage of an LM118 (which has a small-signal bandwidth of 16 MHz) at 0.1 mA. For this op amp $C_p = 5$ pF, $C_1 \cong C_2 \cong 10$ pF. From (49), the nondominant pole is

$$\frac{p_2}{2\pi} \cong 16 \text{ MHz} \tag{50}$$

which lies right at the unity-gain frequency. This pole alone would degrade phase margin by 45°, so it is clear that we need to bias the second stage with a collector current greater than 0.1 mA to obtain adequate g_m. Insufficient pole-splitting can therefore occur; but the cure is usually a simple increase in second stage g_m.

A second type of pole-splitting failure can occur, and it is often much more difficult to cope with. If, for example, one gets over-zealous in his attempt to broadband the nondominant pole, he soon discovers that other poles exist within the second stage which can cause difficulties. Consider a more exact equivalent circuit for the second stage of Fig. 20(a) as shown in Fig. 23. If the follower is biased at low currents or if C_p, Q_2 g_m, and/or r_x are high, the circuit can contain at least four important poles rather than the two considered in simple pole splitting. Under these conditions, we no longer have a response with just negative real poles as in Fig. 21, but observe a root locus of the sort shown in Fig. 24. It is seen in this case that the circuit contains a pair of com-

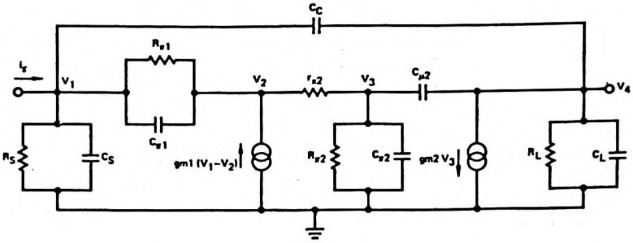


Fig. 23. More exact equivalent circuit for second stage of Fig. 20 (a) including a simplified π model for the emitter follower ($R_{\pi1}$, $C_{\pi1}$, g_{m1}) and a complete π for Q_2 (r_{x2}, $R_{\pi2}$, etc.).

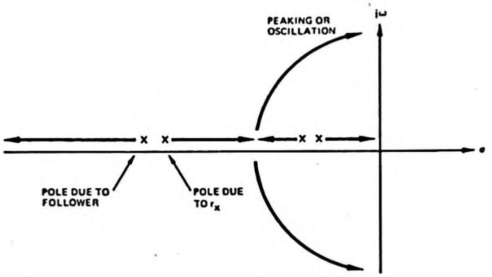


Fig. 24. Root locus for second stage illustrating failure of pole splitting due to high g_{m2}, r_{x2}, C_p, and/or low bias current in the emitter follower.

plex, possibly underdamped poles which, of course, can cause peaking or even oscillation. This effect occurs so commonly in the development of wide-band pole-split amplifiers that it has been (not fondly) dubbed "the second stage bump."

There are numerous ways to eliminate the "bump," but no single cure has been found which is effective in all situations. A direct hand analysis of Fig. 23 is possible, but the results are difficult to interpret. Computer analysis seems the best approach for this level of complexity, and numerous specific analyses have been made. The following is a list of circuit modifications that have been found effective in reducing the bump in the various studies: 1) reduce g_{m2}, r_{x2}, $C_{\mu2}$, 2) add capacitance or a series *RC* network from the stage input to ground—this reduces the high frequency local feedback due to C_p, 3) pad capacitance at the output for similar reasons, 4) increase operating current of the follower, 5) reduce C_p, 6) use a higher f_t process.

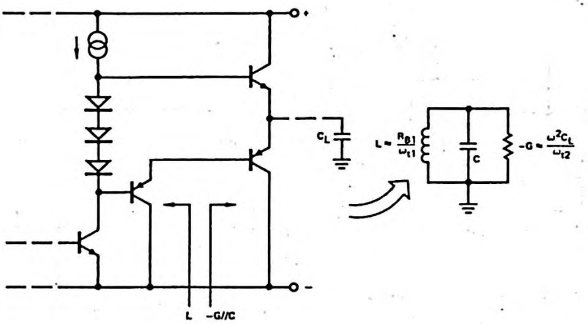
D. Troubles in The Output Stage

Of all the circuitry in the modern IC op amp, the class-AB output stage probably remains the most troublesome. None of the stages in use today behave as well as one might desire when stressed under worst case conditions. To illustrate, one of the most commonly used output stages is shown in Fig. 2(b). The p-n-p's in this circuit are "substrate" p-n-p's having low current f_t's of around 20 MHz. Unfortunately, both β_0 and f_t begin to fall off rapidly at quite low current densities, so as one begins to sink just a few milliamps in the circuit, phase margin troubles can develop. The worst effect occurs when the amplifier is operated with a large capacitive load (>100 pF) while sinking high currents. As shown in Fig. 25, the load capacitance on the output follower causes it to have negative input conductance, while the driver follower can have an inductive output impedance. These elements combine with the capacitance at the interstage to generate the equivalent of a one-port oscillator. In a carefully designed circuit, oscillation is suppressed, but peaking (the "output bump") can occur in most amplifiers under appropriate conditions.

One new type of output circuit which does not use p-n-p's is shown in Fig. 26 [6]. This circuit employs compatible JFET's (or MOSFET's, see similar circuit in [11]) in a FET/bipolar quasi-complimentary output stage, which is insensitive to load capacitance. Unfortunately, this circuit is rather complex and employs extra process steps, so it does not appear to represent the cure for the very low cost op amps.

VII. THE GAIN CELL: LINEAR LARGE-SCALE INTEGRATION

As the true limitations of the basic op amp are more fully understood, this knowledge can be applied to the development of more "optimum" amplifiers. There are, of course, many ways in which one might choose to optimize the device. We might, for example, attempt to maximize speed (bandwidth, slew rate, settling time) without sacrificing dc characteristics. The compatible JFET/bipolar amp of Fig. 15 represents such an effort. An alternate choice might be to design an amplifier having all of the performance features of the most widely used general purpose op amps (i.e., μA741, LM107, etc.), but having minimum possible die area. Such a pursuit is parallel to the efforts of digital large-scale integration (LSI) designers in their development of minimum area



C_L
$L \approx \frac{R_{\beta 1}}{\omega_{t1}}$
C
$-G \approx \frac{\omega^2 C_L}{\omega_{t2}}$
L
-G//C

Fig. 25. Troubles in the conventional class-AB output stage of Fig. 2(b). The low f_t output p-n-p's interact with load capacitance to form the equivalent of a one-port oscillator.

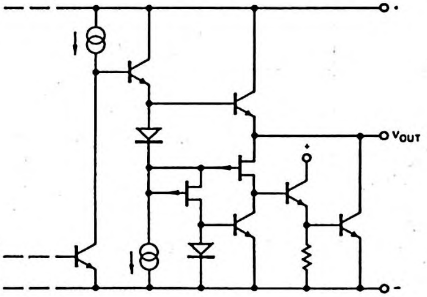


Fig. 26. The "BIFET" output stage employing JFET's and bipolar n-p-n's to eliminate sensitivity to load capacitance.

memory cells or gates. The object of such efforts, of course, is to develop lower cost devices which allow wide and highly economic usage.

In this section we briefly discuss certain aspects of the linear *gain cell*, a general purpose, internally compensated op amp having a die area which is significantly smaller than that of equivalent, present day, industry standard amplifiers.

A. Transconductance Reduction

The single largest area component in the internally compensated op amp is the compensation capacitor (about 30 pF, typically). A major interest in reducing amplifier die area, therefore, centers about finding ways in which this capacitor can be reduced in size. With this in mind, we find it useful to examine (15), which relates compensation capacitor size to two other parameters, unity gain corner frequency ω_u, and first stage transconductance g_{m1}. It is immediately apparent that for a fixed, predetermined unity gain corner (about $2\pi \times 1$ MHz in our case), there is only one change that can be made to reduce the size of C_c: *the transconductance of the first stage must be reduced.* If we restrict our interest to simple bipolar input stages (for low cost), we recall the $g_{m1} = qI_1/kT$. Only by reducing I_1 can g_{m1} be reduced, and we earlier found in Section VI–A and Fig. 19(a) and (b) that I_1 cannot be reduced much without causing phase margin difficulties due to the mirror pole and the tail pole.

An alternate basic approach to g_m reduction is illustrated in Fig. 27 [12]. Here, a multiple collector p-n-p structure, which is easily fabricated in IC form, is used to split the collector current into two components, one component (the larger) of which is simply tied to ground, thereby "throwing away" a major portion of the transistor output current. The result is that the g_m of the transistor is reduced by the ratio of $1/(1 + n)$ (see Fig. 27), and the compensation capacitance can be reduced directly by the same factor. It might appear that the mirror pole would still cause difficulties since the current mirror becomes current starved in Fig. 27, but the effect is not as severe as might be expected. The

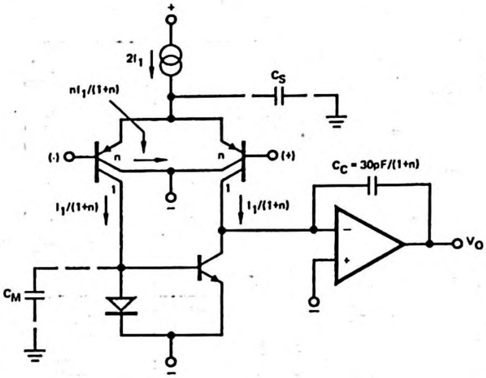


Fig. 27. Basic g_m reduction obtained by using split collector p-n-p's. C_c and area are reduced since $C_c = g_{m1}/\omega_u$.

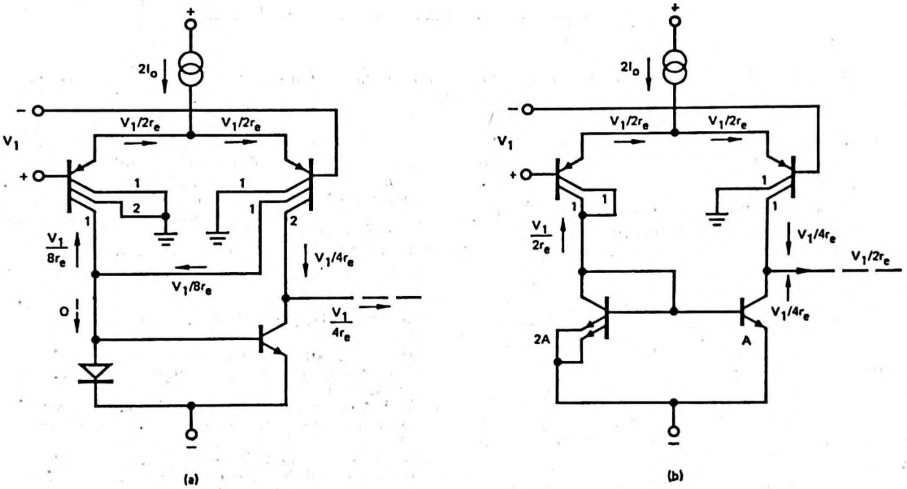


Fig. 28. Variations on g_m reduction. (a) Cross-coupled connection eliminates all ac current passing through the mirror, yet maintains dc balance. (b) This approach maintains high current on the diode side of the mirror, thereby broadbanding the mirror pole.

reason is that the inverting signal can now pass through the high current wide-band path, across the differential amp emitters and into the second stage, so at least half the signal current does not become bandlimited. This partial bandlimiting can be further reduced by using one of the circuits in Fig. 28(a) or (b).[4] In (a), the p-n-p collectors are cross coupled in such a way that the ac signal is cancelled in the mirror circuit, while dc remains completely balanced. Thus the mirror pole is virtually eliminated. The circuit does have a drawback, however, in that the uncorrellated noise currents coming from the two p-n-p's add rather than subtract at the input to the mirror, thereby degrading noise performance. The circuit in Fig. 28(b) does not have this defect, but requires care in matching p-n-p collector ratios to n-p-n emitter areas. Otherwise offset and drift will degrade as one attempts to reduce g_m by large factors.

B. A Gain Cell Example

As one tries to make large reductions in die area for the gain cell, many factors must be considered in addition to novel circuit approaches. Of great importance are special layout/circuit techniques which combine a maximum number of components into minimum area.

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[4] The circuit in Fig. 28(a) is due to R. W. Russell and the variation in Fig. 28(b) was developed by D. W. Zobel.

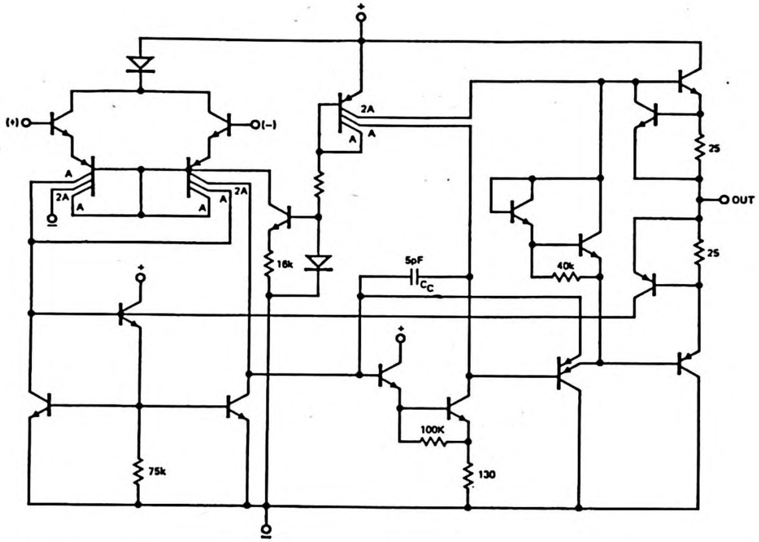

Fig. 29. Circuit for optimized gain cell which has been fabricated in one-fourth the die size of the equivalent μA741.

In a good layout, for example, all resistors are combined into islands with transistors. If this is not possible initially, circuit and device changes are made to allow it. The resulting device geometries within the islands are further modified in shape to allow maximum "packing" of the islands. That is, when the layout is complete, the islands should have shapes which fit together as in a picture puzzle, with no waste of space. Further area reductions can be had by modifying the isolation process to one having minimum spacing between the isolation diffusion and adjacent p-regions.

An example of a gain cell which employs both circuit and layout optimization is shown in Fig. 29. This circuit uses the g_m reduction technique of Fig. 28(a) which results in a compensation capacitor size of only 5 pF rather than the normal 30 pF. The device achieves a full 1-MHz bandwidth, a 0.67-V/μs slew rate, a gain greater than 100 000, typical offset voltages less than 1 mV, and other characteristics normally associated with an LM107 or μA741. In quad form each amplifier requires an area of only 23 × 35 mils which is one-fourth the size of today's industry standard μA741 (typically 56 × 56 mils). This allows over 8000 possible gain cells to be fabricated on a single 3-inch wafer. Further, it appears quite feasible to fabricate larger arrays of gain cells, with six or eight on a single chip. Only packaging and applications questions need be resolved before pursuing such a step.

ACKNOWLEDGMENT

Many important contributions were made in the gain cell and FET/bipolar op amp areas by R. W. Russell. The author gratefully acknowledges his very competent efforts.

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A Color TV Primer for the E. E.

National Semiconductor
Appendix B
Milt Wilcox
October 1975

Section 1 — The Color TV Receiver

Let's look at a color TV in terms of signal flow, from antenna to picture tube.

Although the frequencies used will be for the American NTSC system (National Television System Committee), the basic theory also applies to the European PAL system (Phase Alternating Line). Only in the chroma section do the two systems differ significantly.

RF AND IF SECTIONS

The first part is easy — all signal components received from the antenna pass through a tuner and IF amplifier to the video detector as shown in *Figure 1.*

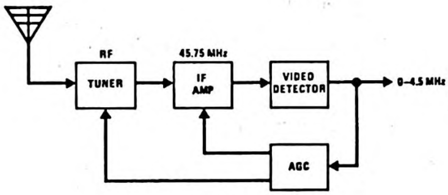

FIGURE 1

The RF signal received ranges in frequency from 55 MHz for channel 2 up to 885 MHz (tuned with the aid of a UHF converter) for channel 83! The tuner has the job of amplifying the desired channel frequency and converting it to an intermediate frequency (IF) of 45.75 MHz. It is then further amplified in the IF amplifier.

The 45.75 MHz signal being amplified is called the video carrier. It is amplitude-modulated (AM) with the picture information, so the video detector must strip this information from the carrier by using some form of envelope detection. So far we could be describing a basic AM radio, except for the signal being received — instead of having audio at the detector output, we have video.

The output level from the video detector is usually around 3 Vp-p. This level must be produced by as little as 10μVrms on the antenna, which works out to 110 dB conversion gain for the three blocks shown in *Figure 1.* However, the catch is the same TV may have to receive antenna signals of up to 0.5 Vrms, and *still produce the same 3 Vp-p* at the video detector. For this reason, a TV has a very effective automatic gain control (AGC) system which detects increases in the peak amplitude of the composite video signal and automatically reduces the gain of the tuner and IF amplifier to compensate.

SIGNAL INFORMATION

The picture you see on a color TV is actually formed by three electron beams, one each for red, blue and green being scanned horizontally and vertically over the screen. As these beams are scanned, their currents are changed to create the light and dark areas on the picture tube face which form the image you view. *Figure 2* shows the video detector output during the time that it takes the electron beams to make one horizontal scan across the screen. The output is actually a combination of four signal components which are required to form a color picture with sound. Let's look at them in turn:

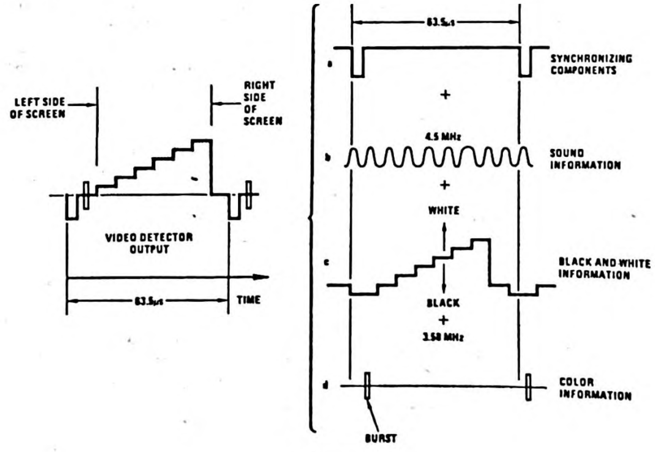

FIGURE 2

a) Synchronizing Components

The synchronizing information is a series of pulses which tell the horizontal section when to return to the left of the screen to start a new *line*, and the vertical section when to return to the top of the screen to start a new *frame*. In the NTSC system each frame contains 525 lines. This is done by scanning the horizontal at approximately 15,750 lines per second, and the vertical at 30 frames per second (the vertical scan rate is actually 60 Hz, but it takes two trips down the screen to complete one frame). The process of returning to start a new scan is called retrace or flyback.

b) Sound Information

The sound information is carried in the form of frequency-modulation (FM) of a 4.5 MHz carrier which in turn modulates the video carrier. (That makes the 4.5 MHz a "sub-carrier"). This sub-carrier is very similar to the IF signal in an FM radio. Although the sound sub-carrier is available at the video detector, a separate detector is often used to reduce crosstalk between signal components.

c) Black-and-White Information (called luminance)

This information determines the instantaneous brightness of the electron beams as they are scanned over the screen. In fact, it is all that is used for the single electron beam in a black-and-white TV set. A negative going video detector detects a luminance signal in which the negative signal extremes correspond to dark areas of the picture and positive signal extremes correspond to bright areas of the picture. Thus the waveform shown in *Figure 2(c)* would produce vertical bars of increasing brightness from left to right. Note that the output is at black during retrace so the electron beams will not be seen. The luminance signal is designated by the letter Y.

d) Color Information (called chrominance)

The color information (which is ignored in a black-and-white TV) is made up of the red, blue and green signals required to drive the picture tube, *minus* the luminance signal. These "color difference" signals, designated R-Y, B-Y and G-Y, modulate a second subcarrier which has a frequency of 3.58 MHz.

Although the type of modulation used on the sub-carrier is of a complex nature it boils down to a simple result:

1. The instantaneous *phase* of the 3.58 MHz signal determines *what* color will be displayed (called hue or tint).

2. The instantaneous *amplitude* of the 3.58 MHz signal determines *how much* color will be displayed (called saturation).

An obvious question is, the phase and amplitude of the 3.58 MHz signal relative to what? The answer is a short burst of 3.58 MHz (simply called the *burst*) which has constant phase and amplitude. The burst will be used to determine the tint and saturation of the color to be displayed. For the waveform shown in *Figure 2(d)* each bar would have a different saturation.

The four signal components are separated and sent to their respective sections in the TV according to the type of signal. Since the sync pulses are the negative peaks of the composite video signal, a peak-detector circuit called a *sync-separator* is used to separate them. The sound and chroma information is contained in sub-carriers which are separated with 4.5 MHz and 3.58 MHz tuned-circuits respectively. The luminance information combines frequency components from 0–4 MHz and therefore uses wideband dc-coupling.

SIGNAL PROCESSING

The remaining sections of the Receiver will now be covered.

Scanning and High Voltage

The sync section is shown in *Figure 3*.

The sync pulses separated in the sync-separator are divided into vertical and horizontal components according to their pulse widths, the vertical sync pulse being a string of wide horizontal sync pulses. When these wide pulses are fed through an integrator, they average to form the vertical sync pulse. The vertical oscillator is "injection-locked" by the vertical sync pulse to initiate vertical retrace at the correct time. The output stage then delivers a ramp of current to the vertical deflection coils to produce vertical scan.

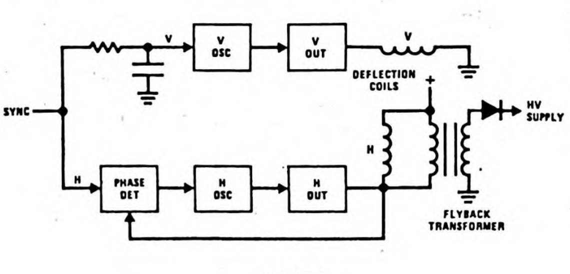

FIGURE 3

The horizontal section uses a different locking system, since horizontal retrace is started *before* the sync pulse is received in order to assure correct centering of the picture. This is done with a phase-locked loop (PLL) in which the oscillator is controlled by a phase detector to insure correct timing between the horizontal sync pulse and the flyback pulse produced by the output stage during horizontal retrace. The horizontal output stage does double duty — besides driving the horizontal deflection coils, it drives the flyback transformer for the picture tube anode high voltage supply. The 25–30 thousand volts dc required is generated either by directly rectifying or by tripling a hv flyback pulse derived from a large turns ratio on the flyback transformer.

The Sound Channel

The 4.5 MHz sound-subcarrier signal is amplified and limited in the sound IF to remove undesired amplitude information. The frequency modulation is then detected by an FM detector and applied to the audio amplifier.

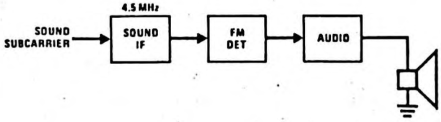

FIGURE 4

Limiting sensitivity for the sound section is typically 100μV and the output power requirement is from 1W to 4W depending on receiver size.

Luma Processing

The luminance signal Y must be amplified and delayed some 0.8μs on its way to the picture tube as shown in *Figure 5.* The delay is required to insure that the black and white information does not arrive at the picture tube before the color information, which is delayed by the comparatively narrow bandwidth of the 3.58 MHz chroma section.

The contrast and brightness controls are also located in the luminance amplifier. The *contrast* control changes the *peak-to-peak* amplitude of the signal, while the *brightness* control changes the *dc* level of the signal.

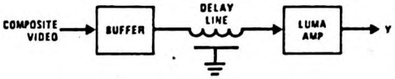

FIGURE 5

Chroma Processing

From the signal taken off the 3.58 MHz tuned circuit the chroma section must derive two signals:

1) The 3.58 MHz chroma sub-carrier signal of the correct amplitude and

2) A continuous 3.58 MHz chroma reference signal of the correct phase relative to the burst.

These two signals, when applied to the chroma demodulator, will produce the desired color difference signals R-Y, B-Y and G-Y. The chroma section is shown in *Figure 6.*

The first problem is that even though the AGC system holds the peak-to-peak video level constant, the chroma sub-carrier itself can vary in amplitude with transmission, antenna and fine-tuning changes, to name a few. Therefore, the chroma section requires an AGC loop of its own, which is called the Automatic Chroma Control stage, or ACC. This block compares the amplitude of the burst to a reference to keep the chroma output signal constant over a 20 dB input range.

The chroma signal is then gated into two components by a pulse derived from the horizontal section. The chroma sub-carrier (during horizontal scan) is sent to the chroma amplifier in which a gain control varies the saturation of the color picture. If *no* burst was present in the ACC stage, the output of the amplifier is "killed" completely for black and white reception.

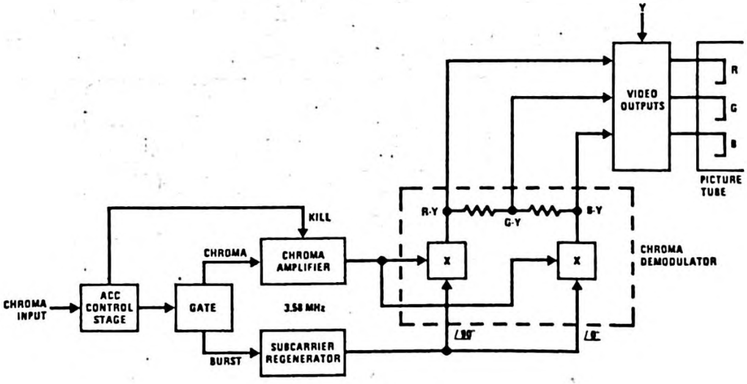

FIGURE 6

The burst (during horizontal retrace) is sent to the sub-carrier regenerator. This is actually a fancy name for a crystal-controlled 3.58 MHz oscillator which is locked to the frequency and phase of the incoming burst by either an injection-lock or phase-lock technique. This forms the reference output, which is passed through a variable phase-shift network to vary the tint of the color picture.

The outputs of the chroma amplifier and sub-carrier regenerator are the signals required by the chroma demodulator, which consists of two synchronous detectors operated in quadrature. What this means is that the reference phase applied to the B-Y detector makes it responsive only to chroma input phases corresponding to blue. The reference applied to the R-Y detector, which is 90° out of phase with the B-Y detector, makes it responsive only to red. The G-Y signal is derived by combining the R-Y and B-Y outputs in the correct ratios.

Finally, the luminance signal Y is added to the chroma difference signals R-Y, B-Y and G-Y to arrive at the desired red, blue and green signals. These signals are further amplified to 100 Vp-p in the video output stage and applied to the appropriate cathodes of the picture tube.

CONVERGENCE

One other messy, but needed, function remains in a color TV receiver — color convergence. The need for convergence results from the origination of the three electron beams in different locations and the fact that they are being scanned over a flat, instead of round, surface. Therefore, the deflection of each beam must be modified separately such that it lands in the same location as the other beams over the entire face of the picture tube.

A complete block diagram of the color TV receiver is shown for reference in *Figure 7.*

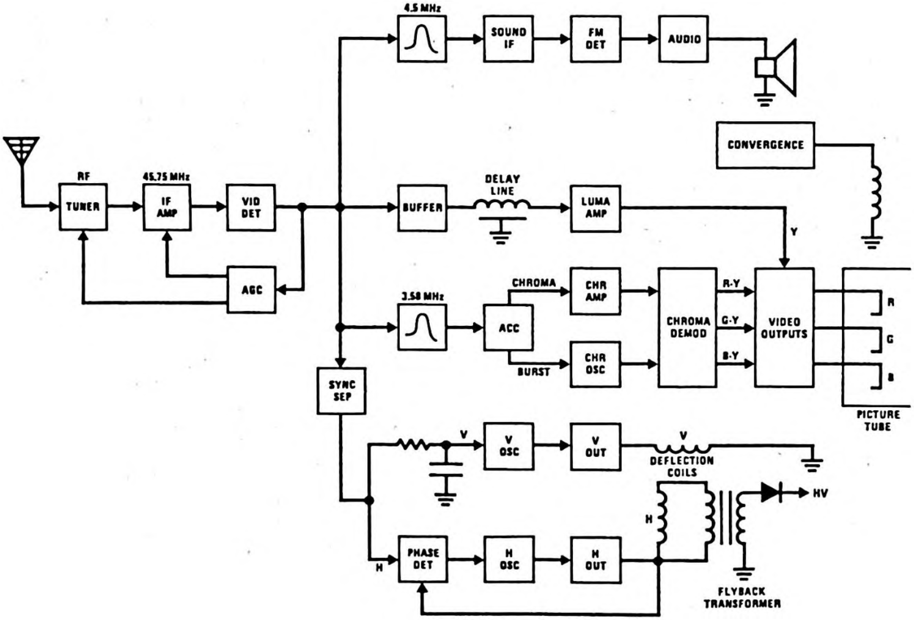
4.5 MHz
SOUND IF
FM DET
AUDIO
CONVERGENCE
RF
45.75 MHz
TUNER
IF AMP
VID DET
BUFFER
DELAY LINE
LUMA AMP
Y
AGC
CHROMA
CHR AMP
3.58 MHz
ACC
BURST
CHR OSC
CHROMA DEMOD
R-Y
G-Y
B-Y
VIDEO OUTPUTS
R
G
B
PICTURE TUBE
SYNC SEP
V
V OSC
V OUT
V
DEFLECTION COILS
H
HV
H
PHASE DET
H OSC
H OUT
FLYBACK TRANSFORMER

FIGURE 7

Section 2 — Integrated Circuits in Television

Here we will look at the integrated circuits used in television including a glimpse inside TV ICs.

Every area of the television which does not have too high a frequency or voltage requirement has been integrated at least once, and many are on second and third generation IC's. The only areas that have been "off-limits" to date are the tuner, video outputs, and horizontal/HV output sections.

RF AND IF SECTIONS

Monolithic circuits have been made to work very well at 45 MHz. The first IC IF systems used 2 chips: one for a 2-stage gain-controlled IF amplifier (Motorola MC1349, 52) and the second for a video detector with gain (Motorola MC1330). The major obstacle to combining these two chips into a single chip has been stability problems due to internal and/or external coupling output to input. However a one chip IF amplifier and video detector is now widely used in Europe (Telefunken TDA 440). The AGC system is also often included in these chips. Another IF function used in most color TV receivers today is automatic fine tuning (AFT) which keeps the tuner correctly tuned to the IF frequency (LM3064 type).

The first chip to incorporate all of the above functions into a single chip is the National LM1807. The chip uses a phase-locked loop to tune the tuner to the IF frequency set by a local oscillator on the chip. This concept is new to TV and is generating a lot of interest.

Rapid progress is also being made in periphery circuits to tuners. Present IC tuning systems control the voltage on a varactor in the tuner to tune the desired channel. However, new systems will actually "synthesize" the tuner local oscillator frequency for each channel.

SCANNING

The deflection area is one of the last to be integrated. While only low-level horizontal circuits have been integrated, vertical drivers and even output stages have been attempted. Current IC's include the Motorola MC1391 or Philips TBA 920 for horizontal and the SGS TDS 1270 for vertical.

In the standard U.S. television system, the vertical and horizontal scanning frequencies are related by the formula $f_v = 2f_H/525$. The National DM8890 makes use of this fact by dividing down a horizontal signal to generate vertical timing, thus eliminating the need for a vertical hold control. Although previous combined vertical/horizontal chips have been unsuccessful, the digital approach holds much promise and TI has announced a combined chip using I^2L.

THE SOUND CHANNEL

The LM3065 type sound IF/FM Detector is currently used in most TV receivers along with a class B discrete or IC audio amplifier. However, virtually every IC manufacturer has announced a one chip "sound system" combining the IF, detector, and audio amplifier. National's entry is the LM1808 which has been well received.

LUMA PROCESSING

Standard IC's have not been developed for the Luma area because of questionable economics. Instead, most of the efforts so far have been custom, with different IC's being used by Zenith, Sylvania and several European TV companies.

CHROMA PROCESSING

The first IC in TV was the chroma demodulator. Today every color TV has one, usually an LM746 or LM1828 type. In one variation the luminance signal is added to the color difference outputs on the chip (Motorola MC1324).

The chroma amplifier and subcarrier regenerator sections have been integrated using a phase-locked loop system with two chips (LM3070 and LM3071 types) and an injection-locked system with one chip (Motorola MC1398). Both of these systems are widely used. Second generation systems which do the phase-locked system with one chip (RCA CA3126 or Motorola MC1399) are gaining acceptance. All of these systems can be used with the above-mentioned demodulators.

Thus, so far the chroma section takes a minimum of two chips, including the demodulator. When will the demodulator be combined with the rest of the system for a true one-chip chroma? Hitachi has just introduced the first practical attempt and others are sure to follow.

WHAT'S A JUNGLE?

A "jungle" IC is a combination of miscellaneous TV functions on one chip. For example, the Zenith jungle (LM1845 type) does the sync-separator and AGC functions. The term is also sometimes applied to deflection IC's which include other functions.

INSIDE TV IC's

Next to the basic differential amplifier, the most widely used linear circuits in TV IC's are probably the current-sharing gain control stage and the linear multiplier.

Gain Control

The current-sharing gain control stage is so named because the input current is shared between two outputs depending on the dc control voltage V_C. For the circuit shown in *Figure 8*, the small signal gain at room temperature is given by:

$$A = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \cong \frac{R_L/R_e}{1 + \exp\left(\frac{V_C \text{ in mV}}{26}\right)}$$

As V_C is increased, the circuit acts as a logarithmic attenuator, yielding a gain reduction of approximately 20 dB for each 60 mV of applied voltage. This same basic gain control stage is used in IF AGC and chroma ACC circuits, as well as for volume, contrast, and chroma controls.

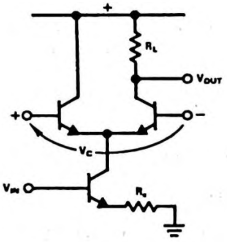

FIGURE 8

Multiplier

The multiplier is widely used in television IC's for amplitude, phase, and frequency detection. *Figure 9* shows a typical configuration in which the bottom pair is degenerated for linear operation while the top quad is switched. If $V_a(t)$ is an amplitude modulated carrier $F_m(t)\cos\omega t$ and $v_b(t)$ is a square wave of the same frequency ω and relative phase ϕ, then the filtered output is given by:

$$V_{OUT} \cong \frac{2}{\pi}\,\frac{R_L}{R_e}\,F_m(t)\cos\phi$$

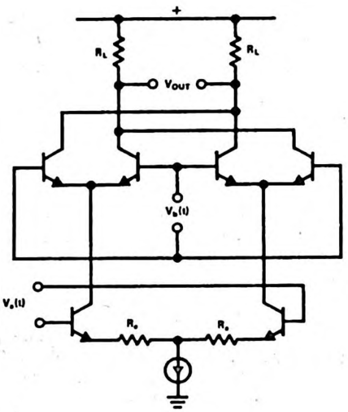

FIGURE 9

Thus the output depends on the amplitude of V_a and the relative phase ϕ between V_a and V_b.

If ϕ is made 0 degrees so COS ϕ is 1, then the multiplier acts as an amplitude detector and can be used to detect the video modulation on the IF carrier. Note that around 0 degrees COS ϕ changes very little with phase. To use the multiplier as a phase or frequency detector, $V_a(t)$ is limited to remove amplitude information and ϕ is centered at 90 degrees where COS ϕ produces the largest change in output for a given change in phase. This operation mode is used for chroma burst phase detectors and sound FM detectors. Both the amplitude and phase sensitive properties of the multiplier are used in chroma demodulators.

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